CONCORDIA UNIVERSITY
Department of Electrical and Computer Engineering
COEN 313 - Digital System Design II - Winter 2019
Lab 1

Objectives

- To become acquainted with the VHDL simulation software tool, logic synthesis tools, and FPGA implementation software tools.
- To learn the rudiments of Modelsim DO files.

Procedure

This lab will introduce the student to the various software tools used in the COEN 313 course. You are required to read Parts I, II, III, and IV of the tutorial "Digital Logic Simulation and Synthesis Using Modelsim, Precision RTL, and Xilinx ISE" and to **simulate**, **synthesize** and **download** to the Xilinx FPGA board the **full adder** example given in Part II of the tutorial.

Requirements

1. Modelsim simulation results of the full adder and the complete VHDL source code of the full adder together with DO file used to simulate the full adder.

2. RTL schematic diagram of synthesize circuit as produced by Precision RTL.

3. Xilinx UCF file used for implementation.

4. Demonstrate the downloaded design to the lab instructor.

Questions

1. What is the advantage of using the **-r** option in a force command within a DO file?

2. Briefly explain two methods of creating a repeating periodic signal using DO files.