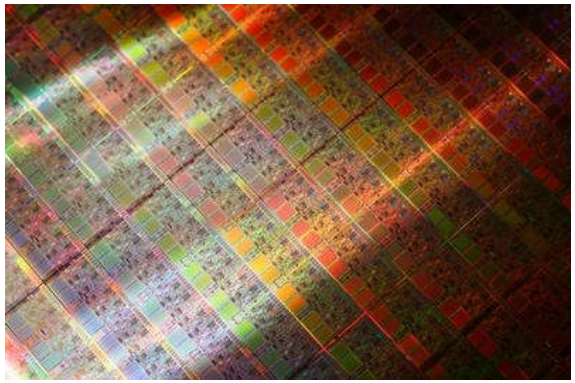
Computer Organization and Design
No.CST 31116 (Spring 2024)

Introduction



Prof. Jiang Zhong

Introduction

Three Key Questions

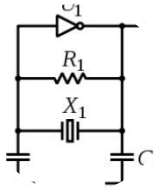
- **Why we learn this course?**
- What should we learn from this course?
- How to learn this course?

课程之间的关系

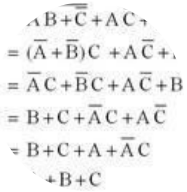
计算机组成与结构

数字逻辑

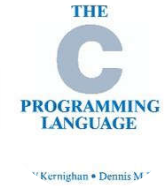
汇编语言



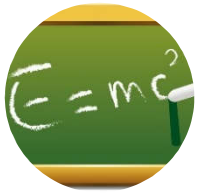
电路原理



离散数学



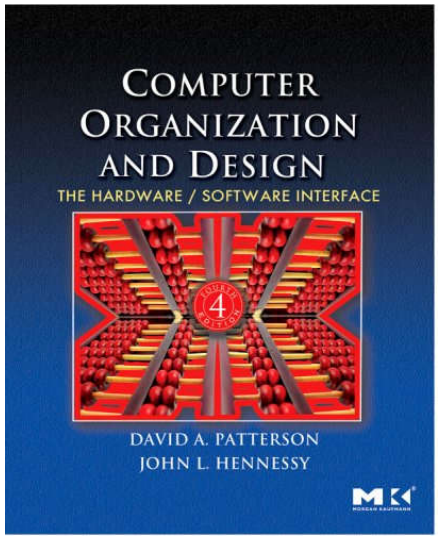
程序设计基础



大学物理

Scope of Course

- Lecture Topics:
  - Performance Metrics
  - Instruction Set Architectures (MIPS/ARM)
  - Computer Arithmetic
  - Memory Hierarchy, Storage and I/O
  - Datapath and Pipline
  - CPU与控制器设计与实现
  - 微程序控制器设计
  - 流水线控制器设计



What you will Learn

- How are programs written in high level languages (C or Java) translated into the language of the hardware, and how does hardware execute the resulting program?
- What is the interface between software and hardware, and how does software instruct hardware to perform needed functions? ISA (instruction set architecture)
- What determines the performance of a program, and how can software programmers and hardware designers improve performance?
- What are the reasons for and consequences of the recent switch from sequential to parallel processing?

What you will Learn

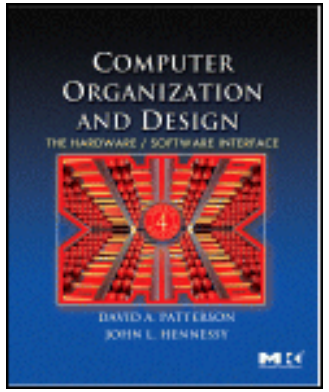
The implementation of a machine has two components: organization and hardware. The term organization includes the high-level aspects of a computer's design, such as the memory system, the bus structure, and the internal CPU (central processing unit—where arithmetic, logic, branching, and data transfer are implemented) design

Course Logistics

- Instructor
  - Jiang Zhong 钟 将 (zhongjiang@cqu.edu.cn, 13983650069)
  - Website: http://www.cs.cqu.edu.cn/info/1139/1783.htm
  - Office Hours: Wed.: 1:30-2:30 pm (Main Building 1709)
- TA

  戚舜恒
- Class Meets

  每周一下午**3:00** 信息大楼**B416**
- Textbook (Required)
  - David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, **5th Edition**, Morgan Kaufmann, October 2015



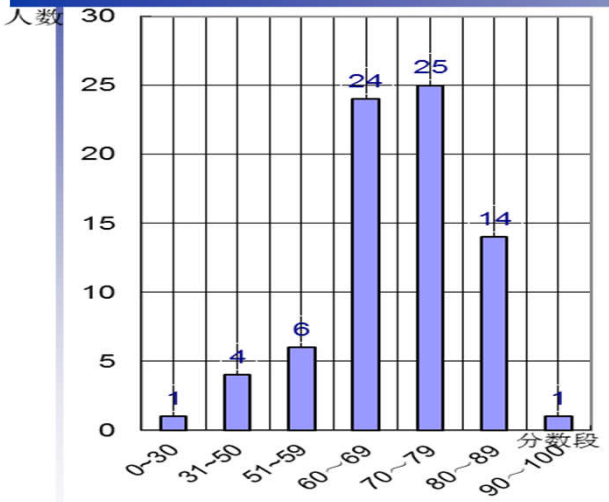
What You Should Know

- Prerequisite
  - Intro to Microprocessors
- Basic digital logic design
  - FSM, synchronous design
- Basic structure of a microprocessor
  - including memory subsystem, I/O
- Addressing modes
  - for operands in instructions
- Some experience with assembly language programming, debugging
- Verilog HDL

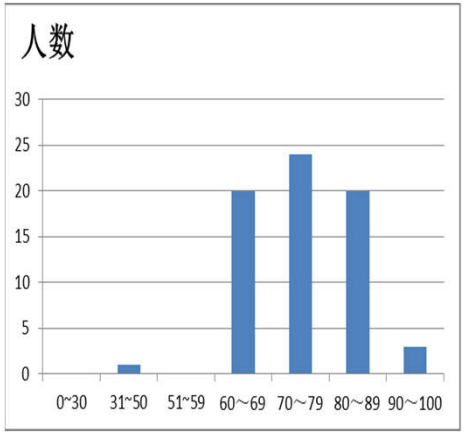
Evaluation and Grading

- Homework Assignments (5): 10%
- Class Participation: 10%
  - Quizzes (4-5): 10%
- Examinations (closed book/notes): 40%
  - Comprehensive Final: 40%
- Experiments: 20%
- Project: 20%

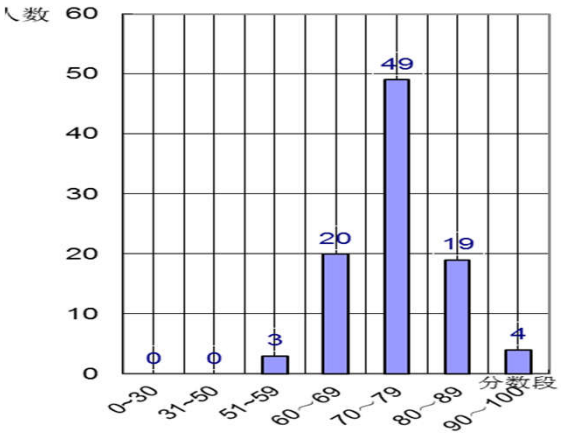
Grade Distributions in Recent Years



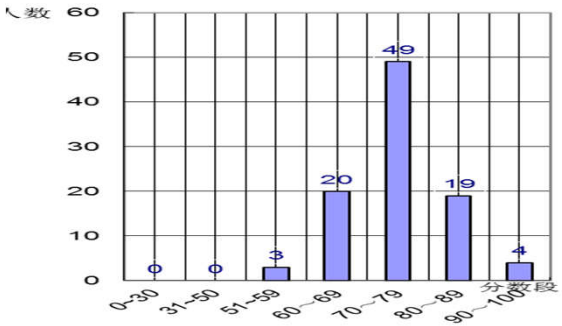
2009



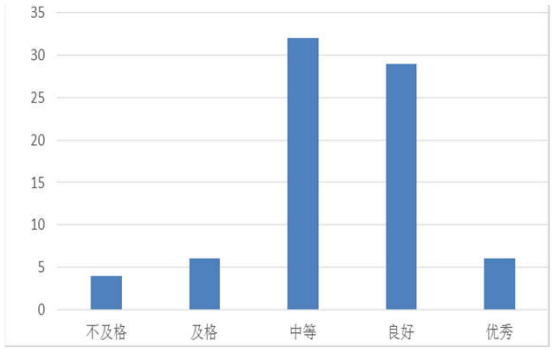
2010



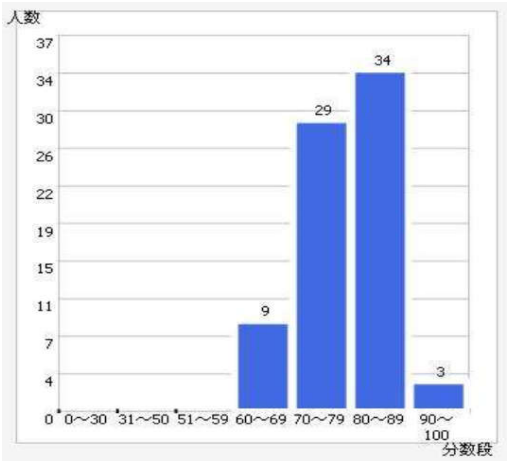
2011



2012



2013



2014

Evaluation and Grading

- **Homework Policy**
  - No late submissions accepted unless you have a valid excuse（through **sakai system**）
- **Attendance**
  - Your responsibility to keep track of what you missed if absent
  - Keep track of assignments and due dates
- **Academic Honesty**
  - All submitted work should be your own. Plagiarism/cheating will result in all students involved getting a zero on the assignment/exam and potentially a failing grade. Refer to the *CQU Academic Integrity Guidelines* for more information.
- **Appointment**
  - I encourage you to make at least one appointment with me during the semester for advice or to discuss research opportunities, research ideas, course suggestions, concerns etc.

Don’t Forget …

Ask Questions in class!