Hi3519 V100 Professional HD IP Camera SoC

Key Specifications

Processor Core

- 800 MHz A7 core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache
- 1.2 GHz A17 core, supporting 32 KB I-cache, 32 KB D-cache, and 256 KB L2 cache
- Neon acceleration, integrated FPU
- ARM@big-LITTLE architecture

Video Encoding

- H.264 BP/MP/HP
- H.265 Main Profile
- I/P frame H.264/H.265 encoding
- MJPEG/JPEG baseline encoding

Video Encoding Performance

- Maximum 16-megapixel resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capabilities
  - 4K x 2K@30 fps+720p@30 fps
  - 16 megapixels@2 fps
- JPEG snapshot at 8-megapixel@30 fps
- CBR/VBR control, ranging from 16 kbit/s to 100 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 60 fps
- Encoding of eight ROIs

Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- 3D denoising, image enhancement, and dynamic contrast improvement
- Anti-flicker for output videos and graphics
- 1/15.5x to 16x video scaling
- 1/2x to 2x graphics scaling
- OSD overlaying of eight regions before encoding
- Video graphics overlaying of two layers (video layer and graphics layer)

ISP

- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilization
- Anti-fog
- Lens distortion correction and fisheye correction
- Picture rotation by 90° or 270°
- Picture mirroring and flipping
- 4F/3F/2F frame-/line-based digital WDR and tone mapping
- ISP tuning tools for the PC

Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, ADPCM, and G.726 protocols
- Audio 3A functions (AEC, ANR, and ALC)

Security Engine

- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA1024/2048/4096 signature verification algorithm implemented by using hardware
- Hash-SHA1/256 and HMAC_SHA1/256 tamper proofing algorithms implemented by using hardware
- Integrated 512-bit OTP storage space and hardware random number generator

Video Interfaces

- VI Interfaces
  - 8-/10-/12-/14-bit RGB Bayer DC timing VI, at most 150 MHz clock frequency
  - BT.601, BT.656, or BT.1120 VI interface
  - 12-lane MIPI, LVDS/sub-LVDS interface, and HiSPI
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
- VO interfaces
  - One PAL/NTSC output for automatic load detection
  - One BT.1120/BT.656 VO interface for connecting to an external HDMI or SDI, supporting at most 1080p@60 fps LCD output

Audio Interfaces

- Integrated audio CODEC supporting 16-bit audio inputs and outputs
- I^{2}S interface for connecting to an external audio CODEC
- Dual-channel differential MIC inputs for reducing background noises

Peripheral Interfaces

- POR
- One integrated high-precision RTC
- Integrated 4-channel SAR ADC
- Five UART interfaces
- IR interface, I^{2}C interface, SSP master interface, and GPIO interface
- Eight PWM interfaces (four independent interfaces and four ones multiplexed with other pins)
- Two SD 3.0/SDIO 3.0 interfaces, supporting SDXC
- One USB 3.0/USB 2.0 host/device port
- One PCIe 2.0 interface in master/slave mode
- RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and 1000 Mbit/s full-duplex mode, and TSO network acceleration

External Memory Interfaces

- DDR4/DDR3/DDR3L interface
  - One 32-bit DDR4/3/3L interface with the maximum frequency of 800 MHz (1.6 Gbit/s)
  - Maximum capacity of 1024 MB for a 16-bit DDR SDRAM
  - Maximum total capacity of 2048 MB for two 16-bit DDR SDRAMs
- SPI NOR flash interface
  - 1-/2-/4-wire mode
  - 3-byte or 4-byte address mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface, supporting the maximum capacity of 512 MB
- eMMC 5.0 interface, supporting the maximum capacity of 64 GB
- NAND flash interface
  - 8-bit data width
  - SLC or MLC
  - 4-/8-/24-/40-/64-bit ECC
  - Components with 8 GB or larger capacity
- Booting from the SPI NOR flash, SPI NAND flash, or NAND flash
- Booting from an eMMC

SDK

- Linux-3.18-based SDK
- High-performance H.264/H.265 PC/iOS/Android decoding library
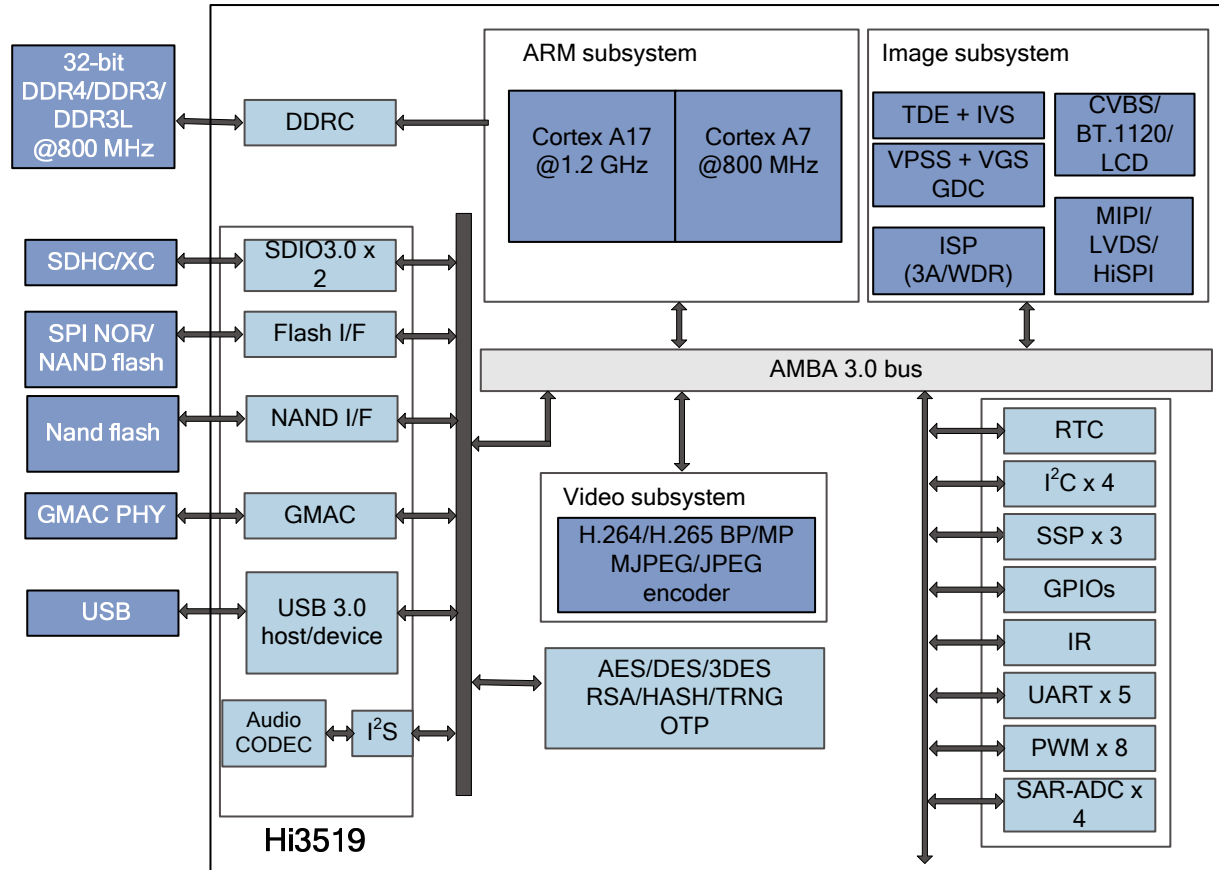
Physical Specifications

- Power consumption
  - 1.5 W typical power consumption in the 4K x 2K scenario
  - Multi-level power saving mode
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
  - 1.2 V, 1.35 V, or 1.5 V DDR4/3/3L SDRAM interface voltage
- Package
  - RoHS, TFBGA
  - Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.)
  - Ball pitch of 0.65 mm (0.026 in.)

Functional Block Diagram

As a new-generation industry-specific SoC designed for the HD IP camera, Hi3519 V100 integrates a new-generation ISP and uses the latest H.265 video compression encoder in the industry as well as advanced low-power technology and architecture design. These features enable Hi3519 V100 to continuously maintain the leading position in the aspects of low bit rate, high picture quality, and low power consumption. Hi3519 V100 supports 90° or 270° rotation and lens distortion correction by using hardware, which meet requirements in various surveillance application scenarios. It also supports 3A algorithms, which allow customers to design various models of IP cameras that contain integrated camera cores. Hi3519 V100 integrates the POR, RTC, and audio CODEC and supports various sensor levels and clock outputs, which significantly reduces the EBOM cost of the HD IP camera based on Hi3519 V100. The Hi3519 V100 HiSilicon SDK features high stability and ease of use, supports rapid mass production, and facilitates system layout of DVRs, NVRs, and IP cameras.

Hi3519 V100 HD IP Camera Solution