**Lab 2 Report**

**Group #: \_\_\_\_\_\_\_\_**

**Group Members: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**PART I: 2D IDCT Accelerator Design**

*Provide an overview of how you designed hw accelerator for the 2D IDCT. In particular, discuss:*

* *How inputs/outputs are passed between the 2D IDCT hardware accelerator and DMA cores (if you also implemented the color combiner in hardware, discuss how you connected the two accelerators with DMA cores);*
* *Hardware design for the 2D IDCT hardware accelerator, preferably including one or multiple state machines to describe the implemented logic.*
* *Software changes required to drive the DMA cores.*

*The overall length of the report (including all 3 parts) should not exceed 4 pages.*

**PART II: Profiling**

*Complete the tables below with your profiling information; use the v3\_300 file. You only need to include functional blocks whose timing changed compared to Lab 1 (i.e., at least idct). If you implemented any additional hw accelerator (ex: color combination), add the information to the tables.*

**Maximum execution time in ms**

|  |  |
| --- | --- |
|  | **Nios-II/f with HW Accelerator** |
| **idct, one frame** |  |

**Average application frame rate: \_\_\_\_\_\_\_\_**

**FPGA utilization**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Number of Logic Elements (ALM)** | **Number of 10Kbits RAM Blocks (M10K blocks)** | **Number of DPS units** |
| **Nios-II/f** |  |  |  |
| **DMA core** |  |  |  |
| **Idct2D custom instruction** |  |  |  |

**PART III: Period Optimization**

*Briefly discuss how you modified the code to optimize the application period for a sequence of I-frames and P-frames, and how you determined the minimum period. Specify the number of employed frame buffers, and any change required to the playback control logic.*

**PART IV: Group Members Contribution**

*Provide a short discussion of the contribution of each lab member.*