SACRAMENTO
STATE

Course: CSC/EEE 273 Hierarchical Digital Design

Term Project Report - Router

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Term Project Status Report

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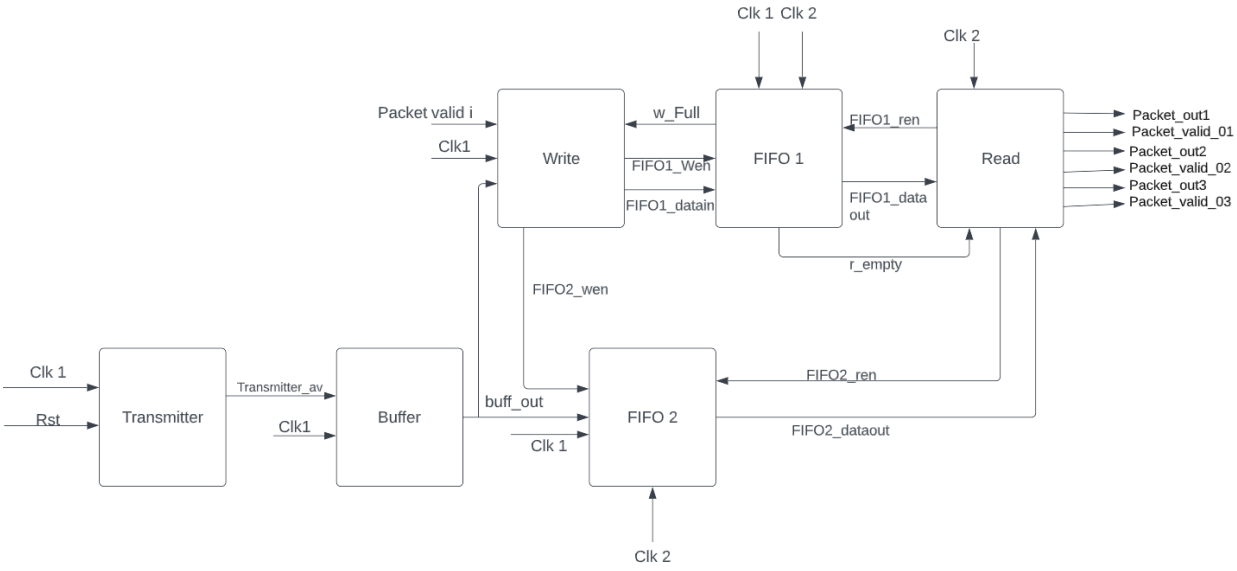
Write FSM	Sneha, Hazim, Ramya
Read FSM	Sneha, Hazim, Ramya
Main Router	Sneha, Hazim, Ramya
Main router testbench	Sneha, Hazim, Ramya

Overall Contribution

Name	Design	Testbench	Synthesis	Project report
Hazim Shaikh	33.33%	33.33%	33.33%	33.33%
Sneha Thatte	33.33%	33.33%	33.33%	33.33%
Ramya Ramani	33.33%	33.33%	33.33%	33.33%

Block Diagram of Router:



Main router source code:-

```
//Router code
//Authors:  Hazim, Sneha, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v

`include "read.v" // READ Control Unit Module
`include "write.v" // WRITE FSM Module
`include "fifo.v" //Asynchronous FIFO module
//`include "fifoo.v" //FIFO

module router (
input rst,
input clk1,
input clk2,
input [7:0] packet_in,
input packet_valid_i,
output packet_valid_o1,
output packet_valid_o2,
output packet_valid_o3,
output stop_packet_send,
output [7:0] packet_out1,
output [7:0] packet_out2,
output [7:0] packet_out3);

parameter [7:0] TS1 = 1;
parameter [7:0] TS2 = 2;
```

```
parameter [7:0] TS3 = 3;
parameter DATA_WIDTH = 8;

reg [7:0] buff_out;
wire fifo1_full, fifo1_wen, fifo1_ren, fifo1_empty;
wire [15:0] fifo1_datain, fifo1_dataout;
wire fifo2_full, fifo2_wen, fifo2_ren, fifo2_empty;
wire [7:0] fifo2_dataout;

always@(posedge clk1, posedge rst) begin
        if(rst == 1)
                buff_out <= 0;
        else if(packet_valid_i==1)
                buff_out <= packet_in;
        else
                buff_out <= buff_out;
end

write write_inst ( .rst(rst), .clk(clk1), .buff_out(buff_out), .src1(TS1), .src2(TS2), .src3(TS3),
.packet_valid(packet_valid_i), .fifo1_full(fifo1_full),
.fifo2_wen(fifo2_wen), .stop_packet(stop_packet_send), .fifo1_wen(fifo1_wen), .fifo1_datain(fifo1_datain));

read read_inst ( .rst(rst), .clk(clk2), .packet_valid_o1(packet_valid_o1), .packet_output_1(packet_out1),
.packet_valid_o2(packet_valid_o2), .packet_output_2(packet_out2), .packet_valid_o3(packet_valid_o3),
.packet_output_3(packet_out3), .fifo1_ren(fifo1_ren),  .fifo1_empty(fifo1_empty),
.fifo1_datain(fifo1_dataout), .fifo2_ren(fifo2_ren), .fifo2_empty(fifo2_empty), .fifo2_data(fifo2_dataout));

fifo#(.DATA_WIDTH(16), .DEPTH(32)) fifo1_inst(.data_output(fifo1_dataout), .write_inc(fifo1_wen),
.full(fifo1_full), .read_inc(fifo1_ren), .empty(fifo1_empty), .data_in(fifo1_datain), .read_clk(clk2),
.write_clk(clk1), .reset(rst));

//afifo#(.dsize(16), .asize(2)) fifo1_inst(.rdata(fifo1_dataout), .wren(fifo1_wen), .wfull(fifo1_full),
.rden(fifo1_ren), .rempty(fifo1_empty), .wdata(fifo1_datain), .rclk(clk1), .wclk(clk2), .wrstn(rst), .rrstn(rst));
```

```
fifo#(.DATA_WIDTH(DATA_WIDTH), .DEPTH(64)) fifo2_inst(.data_output(fifo2_dataout),
.write_inc(fifo2_wen), .full(fifo2_full), .read_inc(fifo2_ren), .empty(fifo2_empty), .data_in(buff_out),
.read_clk(clk2), .write_clk(clk1), .reset(rst));


//afifo#(.dsize(DATA_WIDTH), .asize(64)) fifo2_inst(.rdata(fifo2_dataout), .wren(fifo2_wen),
.wfull(fifo2_full), .rden(fifo2_ren), .rempty(fifo2_empty), .wdata(buff_out), .rclk(clk1), .wclk(clk2), .wrstn(rst),
.rrstn(rst));


endmodule
```

Router testbench:-

//Router testbench code

//Authors: Hazim, Sneha, Ramya

//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf

// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip

//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913

//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v

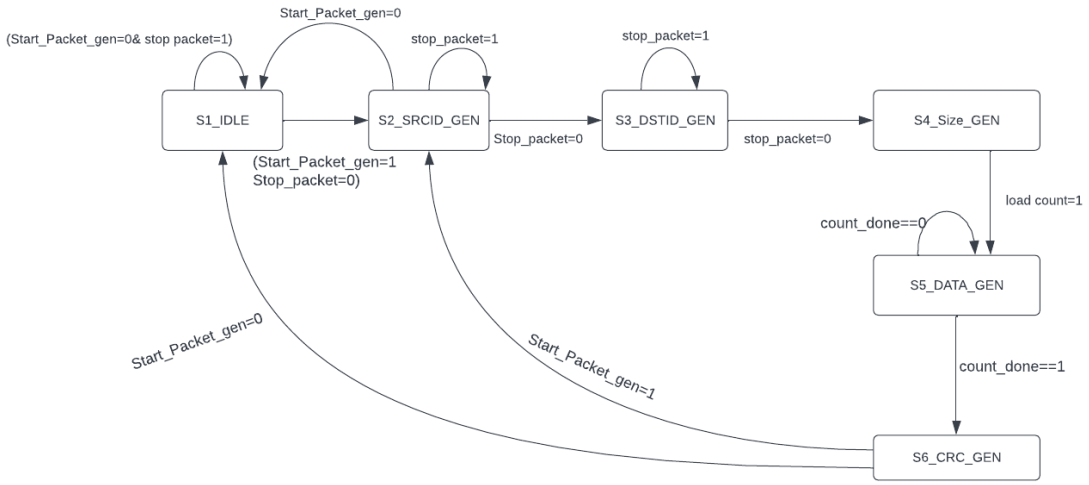
```
`timescale 1us/1us
`include "router.v"
`include "transmitter.v"
module router_tb;
// parameter DATA_WIDTH_TB = 8;
parameter [7:0] TS1_TB = 8'hA;
parameter [7:0] TS2_TB = 8'hB;
parameter [7:0] TS3_TB = 8'hC;
reg write_clk_tb, read_clk_tb, rst_tb;
wire [7:0] packet_out1_tb, packet_out2_tb, packet_out3_tb;
reg start_packet;
reg [7:0] srcid_tb, dstid_tb;
reg [2:0] data_size_tb, count_tb;
wire [7:0] packet_in_tb;
wire packet_valid_tb, start_of_packet_tb, end_of_packet_tb;
wire stop_packet_tb;
transmitter trans (.clk(write_clk_tb), .rst(rst_tb), .srcid(srcid_tb), .dstid(dstid_tb),
.packet_gen_output(packet_in_tb),
.packet_gen_valid(packet_valid_tb), .packet_starting(start_of_packet_tb), .packet_ending(end_of_packet_tb),
.actual_size(data_size_tb), .stop_packet(stop_packet_tb), .start_packet_gen(start_packet));
```

```
router #(.TS1(TS1_TB), .TS2(TS2_TB), .TS3(TS3_TB))

router_inst ( .rst(rst_tb), .clk1(write_clk_tb), .clk2(read_clk_tb), .packet_valid_i(packet_valid_tb),
.packet_in(packet_in_tb), .stop_packet_send(stop_packet_tb),

.packet_valid_o1(pktvalid_o1_tb), .packet_out1(packet_out1_tb), .packet_valid_o2(pktvalid_o2_tb),
.packet_out2(packet_out2_tb), .packet_valid_o3(pktvalid_o3_tb), .packet_out3(packet_out3_tb));


initial begin
        write_clk_tb = 1;
        forever begin
                #2 write_clk_tb = ~write_clk_tb;
        end
end


initial begin
        read_clk_tb =1;
        forever begin
                #5 read_clk_tb = ~read_clk_tb;
        end
end


initial begin
        rst_tb = 1;
        #10;
        rst_tb = 0;
end


always@(posedge write_clk_tb or posedge rst_tb) begin
        if(rst_tb == 1)
                count_tb <=0;
        else if(end_of_packet_tb == 1)
                count_tb <= count_tb+1;
```

```
        else
                count_tb <= count_tb;
end

initial begin
        start_packet = 0;
        srcid_tb = 0;
        dstid_tb = 0;
        data_size_tb = 0;
        #15;
        @(posedge write_clk_tb);
        start_packet = 1;
        srcid_tb = TS1_TB;
        dstid_tb = 8'hA;
        data_size_tb = 5;
        @(posedge write_clk_tb);
        @(end_of_packet_tb);
        @(posedge write_clk_tb);
        srcid_tb = TS2_TB;
        dstid_tb = 8'h82;
        data_size_tb = 7;
        @(posedge write_clk_tb);
        @(end_of_packet_tb);
        @(posedge write_clk_tb);
        srcid_tb = TS2_TB;
        dstid_tb = 8'hFF;
        data_size_tb = 3;
        @(posedge write_clk_tb);
        @(end_of_packet_tb);
        @(posedge write_clk_tb);
```

```
        srcid_tb = TS3_TB;
        dstid_tb = 8'h98;
        data_size_tb = 6;
        @(posedge write_clk_tb);
        @(end_of_packet_tb);
        @(posedge write_clk_tb);
        srcid_tb = 8'hF;
        dstid_tb = 8'hB;
        data_size_tb = 4;
        @(posedge write_clk_tb);
        @(end_of_packet_tb);
end
initial $vcdpluson;
initial begin
        forever begin
                @(count_tb);
        if(count_tb == 5) begin
                start_packet = 0;
                wait(!(pktvalid_o1_tb || pktvalid_o2_tb || pktvalid_o3_tb) );
                @(posedge write_clk_tb);
                @(posedge write_clk_tb);
                @(posedge write_clk_tb);
                @(posedge write_clk_tb);
                $finish;
        end
        end
end
endmodule
```

Transmitter State Diagram



Transmitter source code

```
//Packet Generator Source Code:
//Authors:  Sneha, Hazim, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v

//Transmitter Source Code:
//Authors: Sneha, Hazim, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
module transmitter (
input clk,
input rst,
input [7:0] srcid,
input [7:0] dstid,
output [7:0] transmitter_output,
output reg transmitter_valid,
output reg packet_starting,
output reg packet_ending,
input [2:0] actual_size,
input stop_packet,
input start_packet_gen);

parameter [2:0] S1_IDLE = 3'b000;
parameter [2:0] S2_SRCID_GEN = 3'b001;
parameter [2:0] S3_DSTID_GEN = 3'b010;
parameter [2:0] S4_SIZE_GEN = 3'b011;
parameter [2:0] S5_DATA_GEN = 3'b100;
```

```
parameter [2:0] S6_CRC_GEN = 3'b101;

//input [7:0] srcid, dstid;
//input clk, rst, stop_packet, start_packet_gen;
//input [2:0] actual_size;
//output [7:0] transmitter_output;
//output reg transmitter_valid, packet_starting, packet_ending;
reg [7:0] temp_packet, crc_gen, data;
reg [2:0] cs, ns;
reg gen_crc, clr_crc, load_data_count, clr_data_cnt;
reg [2:0] data_counter;
wire count_done;

assign transmitter_output = temp_packet;
assign count_done = (data_counter == 1)&& (cs == S5_DATA_GEN);

always@(posedge clk or posedge rst) begin
        if(rst)
                cs <= S1_IDLE;
        else
                cs <= ns;
end
always@(posedge clk or posedge rst) begin
        if(rst) begin
                data_counter <= 0;
                data <= 0;
        end

        else begin
                if(load_data_count) begin
```

```
                data_counter <= actual_size;
                data <=1;
            end
            else if(clr_data_cnt == 1) begin
                data_counter <=0;
                data <= 1;
            end
            else if (data_counter ==1) begin
                data_counter <= data_counter;
                data <= data;
            end
            else begin
                data_counter <= data_counter -1;
                data <= data+1;
            end
        end
end
always@(stop_packet, cs, srcid, dstid, start_packet_gen, data, actual_size) begin
        case(cs)
            S1_IDLE : begin
                transmitter_valid = 0;
                packet_ending = 0;
                packet_starting = 0;
                temp_packet = 0;
                clr_data_cnt = 0;
                load_data_count = 0;
                clr_crc = 0;
                if( start_packet_gen == 0 || stop_packet == 1)
                    ns <= S1_IDLE;
                else
```

```
                ns <= S2_SRCID_GEN;
end
S2_SRCID_GEN : begin
        packet_ending =0;
        clr_crc = 1;
        temp_packet = srcid;
        clr_data_cnt = 1;
        if(start_packet_gen ==0)
                ns <= S1_IDLE;
        else if(stop_packet == 1) begin
                ns <= S2_SRCID_GEN;
                transmitter_valid = 0;
        end
        else begin
                ns <= S3_DSTID_GEN;
                transmitter_valid = 1;
                packet_starting = 1;
        end
end
S3_DSTID_GEN : begin
        clr_crc = 0;
        clr_data_cnt = 0;
        temp_packet = dstid;
        packet_starting = 0;
        //if(start_packet_gen ==1)
        //ns <= S3_DSTID_GEN;
        //else
        ns <= S4_SIZE_GEN;
end
```

```
                S4_SIZE_GEN: begin
                        temp_packet = actual_size;
                        load_data_count = 1;
                        ns <= S5_DATA_GEN;
                end
                S5_DATA_GEN: begin
                        temp_packet = data;
                        gen_crc = 1;
                        load_data_count = 0;
                        if(count_done ==1) begin
                                ns <= S6_CRC_GEN;
                        end
                        else
                                ns <= S5_DATA_GEN;
                end
                S6_CRC_GEN: begin
                        packet_ending = 1;
                        gen_crc = 0;
                        temp_packet = crc_gen;
                        if(start_packet_gen == 1)
                                ns <= S2_SRCID_GEN;
                        else
                                ns <= S1_IDLE;
                end
                default: ns <= S1_IDLE;
        endcase
end
// CRC generator
always@(posedge clk or posedge rst) begin
        if(rst)
```

```
                crc_gen <= 0;
        else if(clr_crc == 1)
                crc_gen <= 0;
        else if(gen_crc)
                crc_gen <= temp_packet ^ crc_gen;
        else
                crc_gen <= crc_gen;
end
endmodule
```

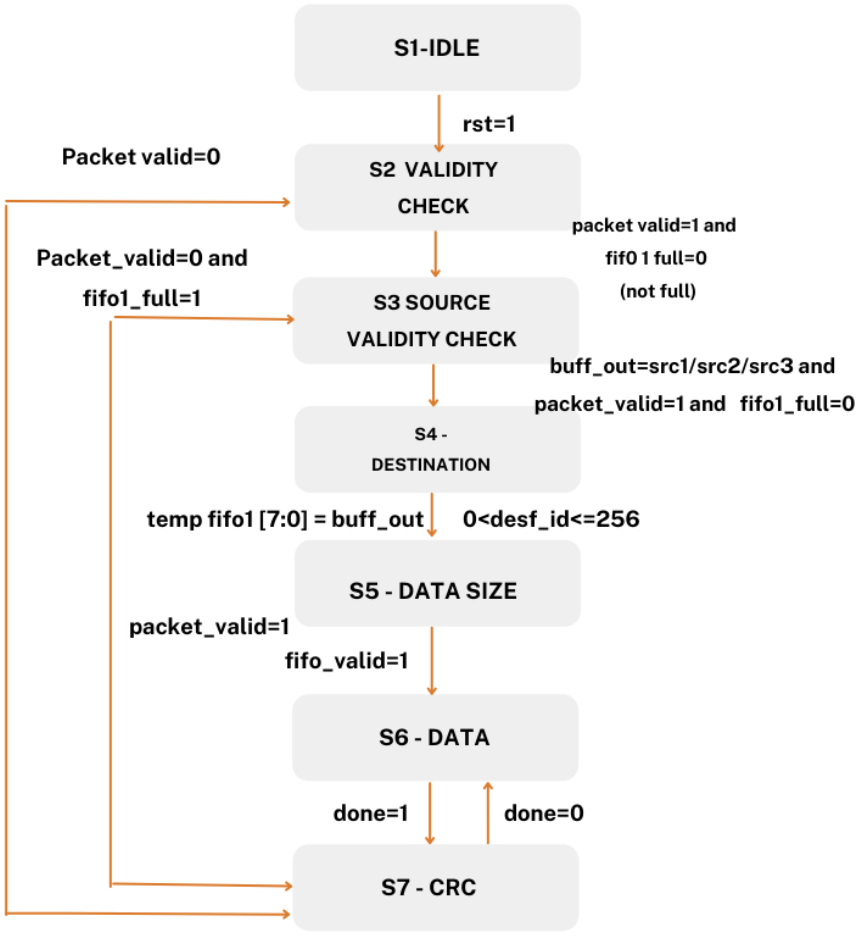
Transmitter testbench:-

```
//Data_Packet Generator Testbench:
//Authors: Sneha, Hazim, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v

`timescale 1us/1us
`include "transmitter.v"
module packet_gen_tb;
parameter TS1_TB = 5;
parameter TS2_TB = 6;
parameter TS3_TB = 7;
reg wr_clk_tb, rd_clk_tb, rst_tb, start_pkt, stop_packet_tb;
reg [7:0] srcid_tb, dstid_tb;
reg [2:0] num_data_tb, count_tb;
wire [7:0] packet_in;
wire packet_valid, sop_tb, eop_tb;
transmitter DUT (.clk(wr_clk_tb), .rst(rst_tb), .srcid(srcid_tb), .dstid(dstid_tb),
.packet_gen_output(packet_in),
.packet_gen_valid(packet_valid), .packet_starting(sop_tb), .packet_ending(eop_tb),
.actual_size(num_data_tb),
.stop_packet(stop_packet_tb), .start_packet_gen(start_pkt));
initial begin
        wr_clk_tb = 1;
        forever begin
                #2 wr_clk_tb = ~wr_clk_tb;
        end
end
```

```
initial begin
        rst_tb = 1;
        #10;
        rst_tb = 0;
end
always@(posedge wr_clk_tb or posedge rst_tb) begin
        if(rst_tb == 1)
                count_tb <=0;
        else if(eop_tb == 1)
                count_tb <= count_tb+1;
        else
                count_tb <= count_tb;
end
initial begin
        #20
        //randsel = $urandom_range(1, 4);
        stop_packet_tb =0;
        start_pkt = 0;
        srcid_tb = 0;
        dstid_tb = 0;
        num_data_tb = 0;
        #4;
        start_pkt = 1;
        srcid_tb = TS1_TB;
        dstid_tb = 8'hF8;
        num_data_tb = 4;
        @(eop_tb);
        @(posedge wr_clk_tb);
        stop_packet_tb = 1;
        @(posedge wr_clk_tb);
```

```
        @(posedge wr_clk_tb);
        @(posedge wr_clk_tb);
        stop_packet_tb = 0;
        srcid_tb = TS2_TB;
        dstid_tb = 8'h8;
        num_data_tb = 5;
        @(eop_tb);
        @(posedge wr_clk_tb);
        srcid_tb = TS2_TB;
        dstid_tb = 8'h45;
        num_data_tb = 7;
        @(posedge wr_clk_tb);
        @(eop_tb);
        // @(posedge wr_clk_tb);
        srcid_tb = TS3_TB;
        dstid_tb = 8'hF;
        num_data_tb = 4;
        @(eop_tb);
end
initial $vcdpluson;
initial begin
        forever begin
                @(count_tb);
                if(count_tb == 4)
                $finish;
        end
end
endmodule
```

Write FSM:


S1-IDLE
rst=1
Packet valid=0
S2 VALIDITY CHECK
packet valid=1 and
fif0 1 full=0
(not full)
Packet_valid=0 and
fifo1_full=1
S3 SOURCE VALIDITY CHECK
buff_out=src1/src2/src3 and
packet_valid=1 and fifo1_full=0
S4 - DESTINATION
temp fifo1 [7:0] = buff_out
0<desf_id<=256
S5 - DATA SIZE
packet_valid=1
fifo_valid=1
S6 - DATA
done=1
done=0
S7 - CRC

Write operation source code:-

```
//Write operation code
//Authors: Hazim, Sneha, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v


module write(
input rst,
input clk,
input [7:0] buff_out,
input [7:0] src1,
input [7:0] src2,
input [7:0] src3,
input packet_valid,
input fifo1_full,
output reg fifo2_wen,
output reg stop_packet,
output reg fifo1_wen,
output reg [15:0] fifo1_datain);

parameter [2:0] S1_IDLE = 3'b000;
parameter [2:0] S2_VALIDITY_CHECK = 3'b001;
parameter [2:0] S3_SOURCE_VALIDITY_CHECK = 3'b010;
parameter [2:0] S4_DESTINATION = 3'b011;
parameter [2:0] S5_DATA_SIZE = 3'b100;
parameter [2:0] S6_DATA = 3'b101;
```

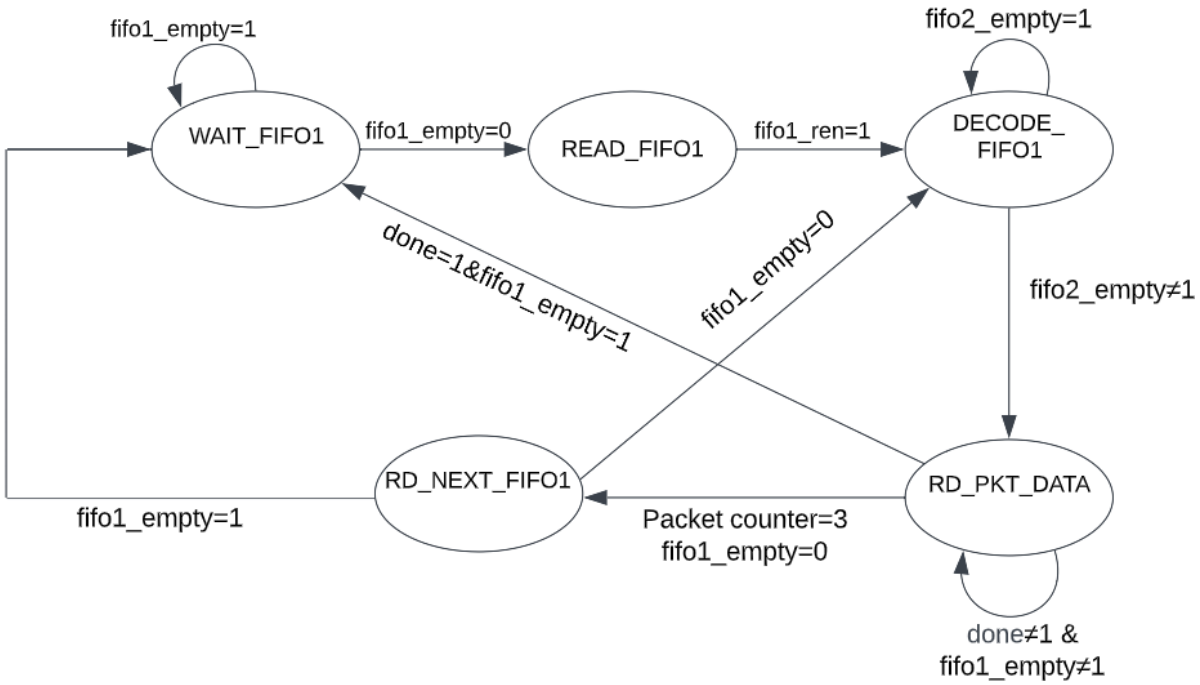
```
parameter [2:0] S7_CRC = 3'b110;

wire done;
reg load_data_count, clear_data_count, fifo1_valid;
reg [2:0] cs, ns, data_counter;
reg [15:0] temp_fifo1;

assign done = (data_counter == 1)&& (cs == S6_DATA);

always @ (posedge clk or posedge rst) begin
        if (rst == 1)
                cs <= S1_IDLE;
        else
                cs <= ns;
end
always@(posedge clk or posedge rst) begin
        if(rst) begin
                data_counter <= 0;
        end
        else begin
                if(load_data_count) begin
                        data_counter <= buff_out;
                end
                else if(clear_data_count == 1) begin
                        data_counter <=0;
                end
                else if (data_counter ==1) begin
                        data_counter <= data_counter;
                end
                else begin
```

```
                data_counter <= data_counter -1;
            end
        end
end
always @(packet_valid, src1, src2, src3, fifo1_full, done, cs) begin
        case(cs)
            S1_IDLE : begin
                fifo1_wen =0;
                stop_packet =0;
                fifo2_wen =0;
                fifo1_valid = 0;
                load_data_count =0;
                temp_fifo1 =0;
                fifo1_datain=0;
                clear_data_count =0;
                if (rst == 0)
                    ns <= S1_IDLE;
                else
                    ns <= S2_VALIDITY_CHECK;
            end
            S2_VALIDITY_CHECK: begin
                clear_data_count = 0;
                fifo2_wen = 0;
                if(packet_valid == 1 && fifo1_full == 0)
                    ns <= S3_SOURCE_VALIDITY_CHECK;
                else
                    ns <= S2_VALIDITY_CHECK;
                if(fifo1_full == 1)
                    stop_packet = 1;
                else
```

```
                stop_packet = 0;
end
S3_SOURCE_VALIDITY_CHECK : begin
        clear_data_count = 0;
        if((buff_out == src1 || buff_out == src2 || buff_out == src3) &&
        (packet_valid == 1 && fifo1_full == 0)) begin
                fifo1_valid = 1;
                fifo2_wen = 1;
        end
        else
                fifo2_wen = 0;
        if(fifo1_full == 1)
                stop_packet = 1;
        else
                stop_packet = 0;
        if(packet_valid == 1 && fifo1_full == 0)
                ns <= S4_DESTINATION;
        else
                ns <= S3_SOURCE_VALIDITY_CHECK;
end
S4_DESTINATION : begin
        temp_fifo1[7:0] = buff_out;
        ns <= S5_DATA_SIZE;
end
S5_DATA_SIZE : begin
        temp_fifo1[15:8] = buff_out + 4;
        fifo1_datain = temp_fifo1;
        load_data_count = 1;
        if(fifo1_valid == 1)
        fifo1_wen = 1;
```

```
                ns <= S6_DATA;
            end
            S6_DATA : begin
                fifo1_wen =0;
                fifo1_valid =0;
                load_data_count = 0;
                if(done == 1)
                    ns <= S7_CRC;
                else
                    ns <= S6_DATA;
            end
            S7_CRC : begin
                clear_data_count = 1;
                if(fifo1_full == 1)
                    stop_packet = 1;
                else
                    stop_packet = 0;
                if(packet_valid ==1)
                    ns <= S3_SOURCE_VALIDITY_CHECK;
                else
                    ns <= S2_VALIDITY_CHECK;
            end
            default : ns <= S1_IDLE;
        endcase
end
endmodule
```

Read Operation FSM



Read operation source code:-

```
//Read operation code
//Authors: Hazim, Sneha, Ramya
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v

module read(
input rst,
input clk,
input fifo1_empty,
input fifo2_empty,
input [15:0] fifo1_datain,
input [7:0] fifo2_data,
output packet_valid_o1,
output packet_valid_o2,
output packet_valid_o3,
output [7:0] packet_output_1,
output [7:0] packet_output_2,
output [7:0] packet_output_3,
output reg fifo1_ren,
output reg fifo2_ren);

parameter [2:0] WAIT_FIFO1 = 3'b000;
parameter [2:0] READ_FIFO1 = 3'b001;
parameter [2:0] DECODE_FIFO1 = 3'b010;
parameter [2:0] READ_PACKET_DATA = 3'b011;
parameter [2:0] READ_NEXT_FIFO1 = 3'b100;
```

```
wire done;
reg load_packet_count, clear_packet_count, packet_valid, packet_dec_en;
reg [1:0] select_output, select_output_reg;
reg[7:0] temp_packet_data;
reg [2:0] cs, ns;
reg [7:0] packet_counter;

assign done = (packet_counter == 1);
assign packet_output_1 = (select_output_reg == 1)? temp_packet_data : 0;
assign packet_output_2 = (select_output_reg == 2)? temp_packet_data : 0;
assign packet_output_3 = (select_output_reg == 3)? temp_packet_data : 0;
assign packet_valid_o1 = (select_output_reg == 1)? packet_valid : 0;
assign packet_valid_o2 = (select_output_reg == 2)? packet_valid : 0;
assign packet_valid_o3 = (select_output_reg == 3)? packet_valid : 0;

always @ (posedge clk or posedge rst) begin
        if (rst == 1)
                cs <= WAIT_FIFO1;
        else
                cs <= ns;
end
always @ (posedge clk or posedge rst) begin
        if (rst == 1)
                select_output_reg <= 0;
        else
                select_output_reg <= select_output;
end
always@(posedge clk or posedge rst) begin
        if(rst) begin
```

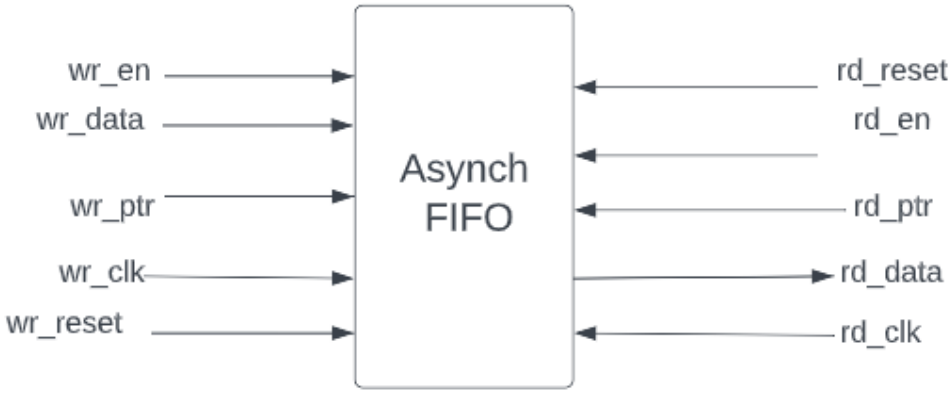
```
                packet_counter <= 0;
        end
        else begin
                if(load_packet_count) begin
                        packet_counter <= fifo1_datain[15:8];
                end
                else if(clear_packet_count == 1) begin
                        packet_counter <=0;
                end
                else if ((packet_counter ==1) || (fifo2_empty == 1) || (packet_dec_en == 0)) begin
                        packet_counter <= packet_counter;
                end
                else
                        packet_counter <= packet_counter -1;
        end
end
always @(fifo1_empty, fifo2_empty, done, cs, fifo1_datain, packet_counter,
fifo2_data) begin
        case(cs)
                WAIT_FIFO1 : begin
                        fifo1_ren =0;
                        load_packet_count =0;
                        packet_dec_en =0;
                        temp_packet_data =0;
                        select_output=0;
                        clear_packet_count =1;
                        packet_valid = 0;
                        fifo2_ren = 0;
                        if(fifo1_empty == 0)
                                ns <= READ_FIFO1;
```

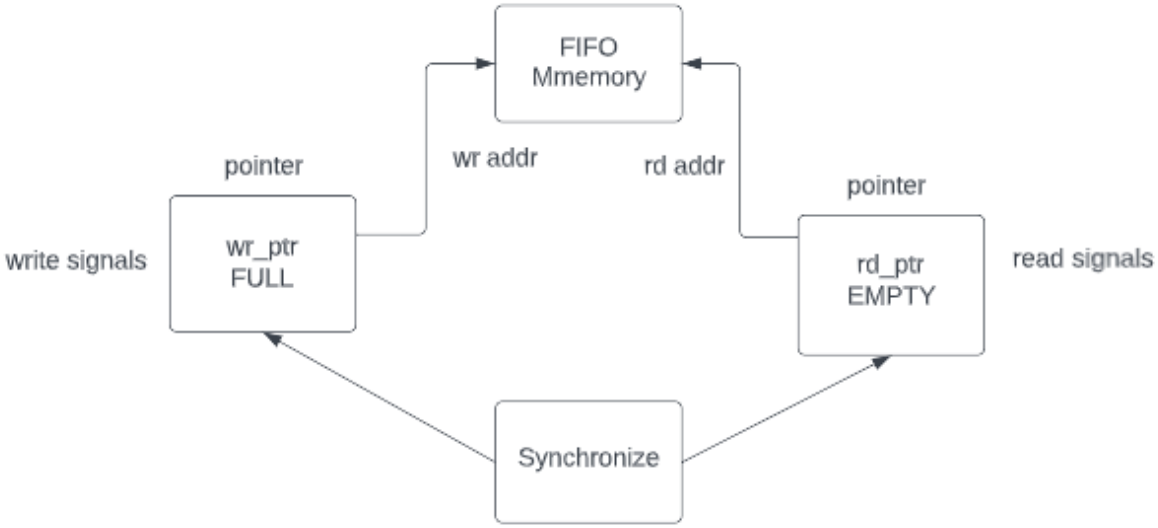
```
        else
                ns <= WAIT_FIFO1;
end
READ_FIFO1: begin
        clear_packet_count =0;
        packet_dec_en = 0;
        packet_valid = 0;
        fifo1_ren = 1;
        ns <= DECODE_FIFO1;
end
DECODE_FIFO1 : begin
        fifo1_ren = 0;
        fifo2_ren = 1;
        clear_packet_count =0;
        load_packet_count = 1;
        packet_dec_en =0;
        if(0 <= fifo1_datain[7:0] && fifo1_datain[7:0] <= 127)
                select_output = 1;
        else if( 128 <= fifo1_datain[7:0] && fifo1_datain[7:0] <= 195)
                select_output = 2;
        else if( 196 <= fifo1_datain[7:0] && fifo1_datain[7:0] <=255)
                select_output = 3;
        else
                select_output = 0;
        if(fifo2_empty == 1)
                ns <= DECODE_FIFO1;
        else
                ns <= READ_PACKET_DATA;
        if(packet_counter >= 1)
                temp_packet_data = fifo2_data;
```

```
                else
                        temp_packet_data = 0;
        end
        READ_PACKET_DATA : begin
                load_packet_count = 0;
                packet_dec_en = 1;
                packet_valid = 1;
                temp_packet_data = fifo2_data;
                if(packet_counter == 3 & fifo1_empty == 0)
                        ns <= READ_NEXT_FIFO1;
                else if(done == 1 && fifo1_empty == 1)
                        ns <= WAIT_FIFO1;
                else
                        ns <= READ_PACKET_DATA;
        end
        READ_NEXT_FIFO1: begin
                temp_packet_data = fifo2_data;
                if(fifo1_empty == 0)
                        fifo1_ren = 1;
                else
                        fifo1_ren = 0;
                if(fifo1_empty == 0)
                        ns <= DECODE_FIFO1;
                else
                        ns <= WAIT_FIFO1;
                end
        default : ns <= WAIT_FIFO1;
    endcase
end
endmodule
```

Asynchronous FIFO:

Asynchronous FIFO is used because here we are dealing with two different clock frequencies. To avoid the confusion for full and empty condition of FIFO binary code is converted into gray code and one extra bit is added to the MSB of actual data. The added MSB determines whether the write pointers and read pointers are full or empty. Async FIFO consists of write pointer, read pointer, FIFO memory along with synchronizer to compare the values of read and write pointers.





FIFO Source code:-

```
//FIFO code
//Authors:  Ramya, Hazim, Sneha
//References: 1. http://www.ijvdcs.org/uploads/625143IJVDCS4170-22.pdf
// Reference 2: https://www.ijert.org/design-and-implementation-of-four-port-router-for-network-on-chip
//Reference 3: https://ieeexplore.ieee.org/abstract/document/6949913
//Reference 4: https://github.com/vritrv/ROUTER-1X3-RTL-DESIGN/blob/master/RTL/router_top.v
module fifo( data_output, write_inc, full, read_inc, empty, data_in, read_clk,
write_clk, reset);

parameter DATA_WIDTH = 8;
parameter DEPTH = 8;

output reg [DATA_WIDTH - 1 : 0] data_output;
input [DATA_WIDTH - 1 : 0] data_in;
output full;
output empty;
input write_inc, read_inc;
input read_clk, write_clk;
input reset;
reg [$clog2(DEPTH) : 0] read_ptr, read_sync_1, read_sync_2;
reg [$clog2(DEPTH) : 0] write_ptr, wr_sync_1, wr_sync_2;
reg [DATA_WIDTH-1 : 0] mem [DEPTH-1 : 0];
wire [$clog2(DEPTH) : 0] read_ptr_b, read_ptr_g;
wire [$clog2(DEPTH) : 0] write_ptr_b, write_ptr_g;
wire [$clog2(DEPTH)-1 : 0] read_mem_ptr;
wire [$clog2(DEPTH)-1 : 0] write_mem_ptr;
assign write_mem_ptr = write_ptr[$clog2(DEPTH)-1:0];
assign read_mem_ptr = read_ptr[$clog2(DEPTH)-1:0];
//Write pointer increment and write logic//
```

```
always @(posedge write_clk or posedge reset) begin
        if (reset)
                write_ptr <= 0;
        else if (write_inc == 1 && full == 0) begin
                write_ptr <= write_ptr + 1;
                mem[write_mem_ptr] <= data_in;
        end
        else
                write_ptr <= write_ptr;
end
//Read Pointer Increment
always @(posedge read_clk or posedge reset) begin
        if (reset) begin
                read_ptr <= 0;
        end
        else if (read_inc == 1 && empty == 0) begin
                read_ptr <= read_ptr + 1;
                data_output <= mem[read_mem_ptr];
        end
        else
                read_ptr <= read_ptr;
end
// Synchronizing Grey code converted Read Pointer to Write clock Domain
always @(posedge write_clk or posedge reset) begin
        if(reset == 1) begin
                read_sync_1 <= 0;
                read_sync_2 <= 0;
        end
        else begin
                read_sync_1 <= read_ptr_g;
```

```
                read_sync_2 <= read_sync_1;
        end
end
//Synchronizig Grey code converted Write pointer to Read clock domain
always @(posedge read_clk or posedge reset) begin
        if(reset == 1) begin
                wr_sync_1 <= 0;
                wr_sync_2 <= 0;
        end
        else begin
                wr_sync_1 <= write_ptr_g;
                wr_sync_2 <= wr_sync_1;
        end
end
// Memory Data Read
//assign data_output = mem[read_mem_ptr];
//return Full
assign full = returnFull(read_ptr_b, write_ptr);
// return Empty
assign empty = returnEmpty(read_ptr, write_ptr_b);
// Write pointer Binary2Gray
assign write_ptr_g = write_ptr ^ (write_ptr>>1);
//Read Pointer Binary2Gray
assign read_ptr_g = read_ptr ^ (read_ptr>>1);
// Write Pointer Gray2Binary
genvar i;
generate
        assign write_ptr_b[$clog2(DEPTH)] = wr_sync_2[$clog2(DEPTH)];
        for(i=$clog2(DEPTH)-1; i>=0; i=i-1) begin : WrGtoB
                assign write_ptr_b[i] = wr_sync_2[i] ^ write_ptr_b[i+1];
```

```
        end
endgenerate
//Read Pointer Gray2Binary
genvar j;
generate
        assign read_ptr_b[$clog2(DEPTH)] = read_sync_2[$clog2(DEPTH)];
        for(j=$clog2(DEPTH)-1; j>=0; j=j-1) begin : RdGtoB
                assign read_ptr_b[j] = read_sync_2[j] ^ read_ptr_b[j+1];
        end
endgenerate
// Function to calculate Empty Condition
function returnEmpty(input [$clog2(DEPTH):0] rdptr, input [$clog2(DEPTH):0] wrptr);
begin
        if(rdptr == wrptr)
                returnEmpty = 1'b1;
        else
                returnEmpty = 1'b0;
        end
endfunction
// Function to calculate Full condition
function returnFull(input [$clog2(DEPTH):0]rdptr, input [$clog2(DEPTH):0]wrptr);
begin
        if(wrptr[$clog2(DEPTH)-1:0] == rdptr[$clog2(DEPTH)-1:0] &&
        write_ptr[$clog2(DEPTH)] != read_ptr[$clog2(DEPTH)])
                returnFull = 1;
        else
                returnFull = 0;
end
endfunction
endmodule
```

Compilation and simv results :-

1. Transmitter:-

```
[hkshaikh@ecs-pa-coding1 ExpProject]$ vcs -debug_access+all trans_testbench.v
                         Chronologic VCS (TM)
        Version S-2021.09_Full64 -- Wed May 11 19:57:35 2022

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Parsing design file 'trans_testbench.v'
Parsing included file 'transmitter.v'.
Back to file 'trans_testbench.v'.
Top Level Modules:
       packet_gen_tb
TimeScale is 1 us / 1 us
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module packet_gen_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic   -o .//../simv.daidir//_cuarc0.so objs/amcQw_d.o
rm -f _cuarc0.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/opt/synopsys/vcs/S-2021.09/linux64/lib -L/opt/synopsys/vcs/S-2021.09/linux64/lib  -Wl,-rpath-link=./ -Wl
,--no-as-needed  /usr/lib64/libnuma.so.1     _25756_archive_1.so _cuarc0.so  SIM_l.o      rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o           -lvirsim -lerrorinf -lsnpsmalloc
 -lvfs    -lvcsnew -lsimprofile -luclinative /opt/synopsys/vcs/S-2021.09/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive          /opt/synopsys/vcs/S-2021.09/linux64/lib/vcs_s
ave_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .228 seconds to compile + .238 seconds to elab + .146 seconds to link
[hkshaikh@ecs-pa-coding1 ExpProject]$ ./simv
Chronologic VCS simulator copyright 1991-2021
Contains Synopsys proprietary information.
Compiler version S-2021.09_Full64; Runtime version S-2021.09_Full64;  May 11 19:59 2022
VCD+ Writer S-2021.09-Full64 Copyright (c) 1991-2021 by Synopsys Inc.
$finish called from file "trans_testbench.v", line 79.
$finish at simulation time                168
           V C S   S i m u l a t i o n   R e p o r t
Time: 168 us
CPU Time:      0.240 seconds;       Data structure size:   0.0Mb
Wed May 11 19:59:17 2022
[hkshaikh@ecs-pa-coding1 ExpProject]$
```

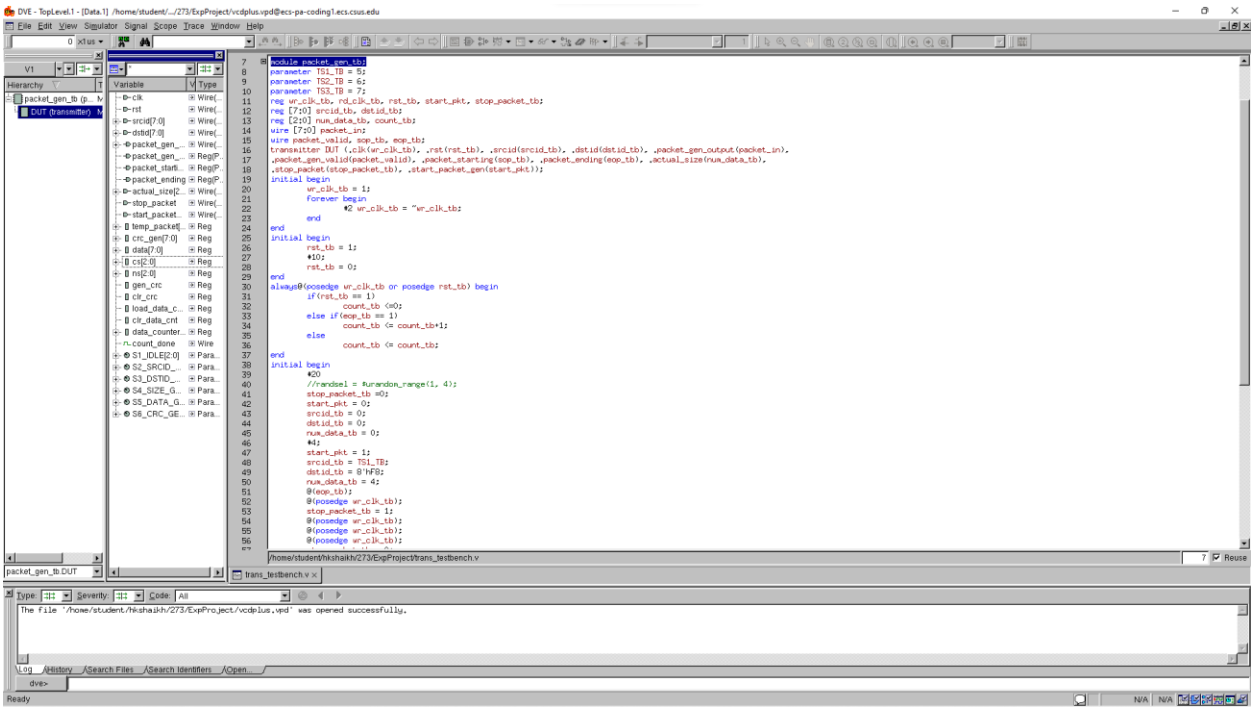

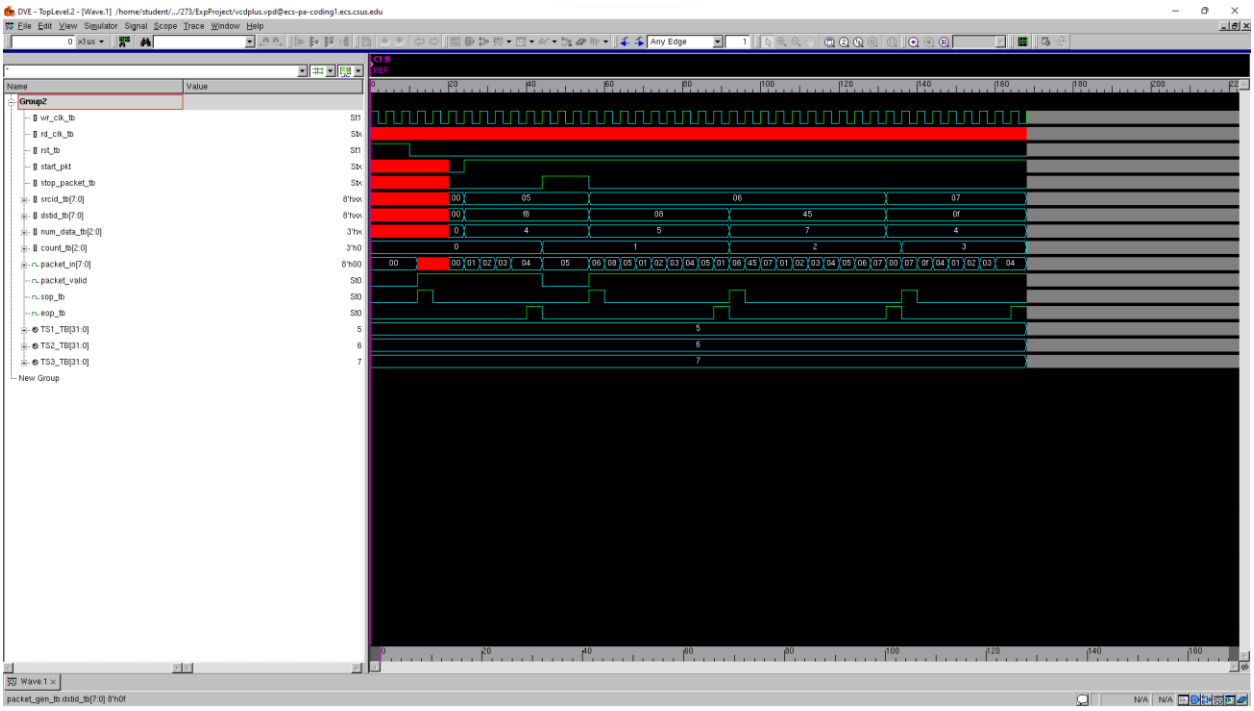
DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group2
wr_clk_tb
rd_clk_tb
rst_tb
start_pkt
stop_packet_tb
srcid_tb[7:0]
dstid_tb[7:0]
num_data_tb[2:0]
count_tb[2:0]
rx_packet_in[7:0]
rx_packet_valid
rx_sop_tb
rx_eop_tb
TS1_TB[31:0]
TS2_TB[31:0]
TS3_TB[31:0]
New Group
Wave.1
packet_gen_tb.dstid_tb[7:0] 8'h0f

2. Router:-

```
[hkshaikh@ecs-pa-coding1 ExpProject]$ vcs -debug_access+all testbench.v
                         Chronologic VCS (TM)
        Version S-2021.09_Full64 -- Wed May 11 20:03:59 2022

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Parsing design file 'testbench.v'
Parsing included file 'router.v'.
Parsing included file 'read.v'.
Back to file 'router.v'.
Parsing included file 'write.v'.
Back to file 'router.v'.
Parsing included file 'fifo.v'.
Back to file 'router.v'.
Back to file 'testbench.v'.
Parsing included file 'transmitter.v'.
Back to file 'testbench.v'.
Top Level Modules:
       router_tb
TimeScale is 1 us / 1 us
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module router_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/opt/synopsys/vcs/S-2021.09/linux64/lib -L/opt/synopsys/vcs/S-2021.09/linux64/lib  -Wl,-rpath-link=./ -Wl
,--no-as-needed  /usr/lib64/libnuma.so.1   objs/amcQw_d.o   _27947_archive_1.so  SIM_l.o      rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lvirsim -lerrorinf -lsnpsma
lloc -lvfs    -lvcsnew -lsimprofile -luclinative /opt/synopsys/vcs/S-2021.09/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive          /opt/synopsys/vcs/S-2021.09/linux64/lib/v
cs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .304 seconds to compile + .252 seconds to elab + .144 seconds to link
[1]-  Done                    dve -full64
[2]+  Done                    dve -full64
[hkshaikh@ecs-pa-coding1 ExpProject]$ ./simv
Chronologic VCS simulator copyright 1991-2021
Contains Synopsys proprietary information.
Compiler version S-2021.09_Full64; Runtime version S-2021.09_Full64;  May 11 20:04 2022
VCD+ Writer S-2021.09_Full64 Copyright (c) 1991-2021 by Synopsys Inc.
$finish called from file "testbench.v", line 102.
$finish at simulation time                464
           V C S   S i m u l a t i o n   R e p o r t
Time: 464 us
CPU Time:      0.230 seconds;       Data structure size:   0.0Mb
Wed May 11 20:04:07 2022
[hkshaikh@ecs-pa-coding1 ExpProject]$
```
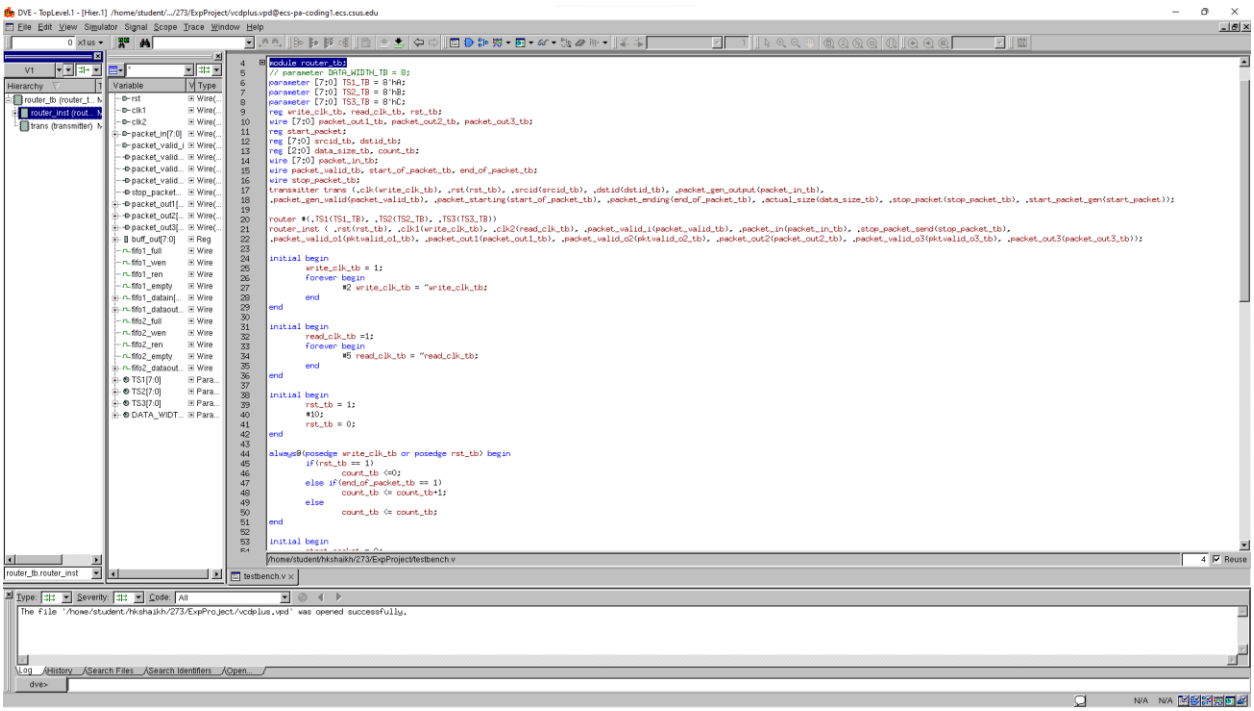
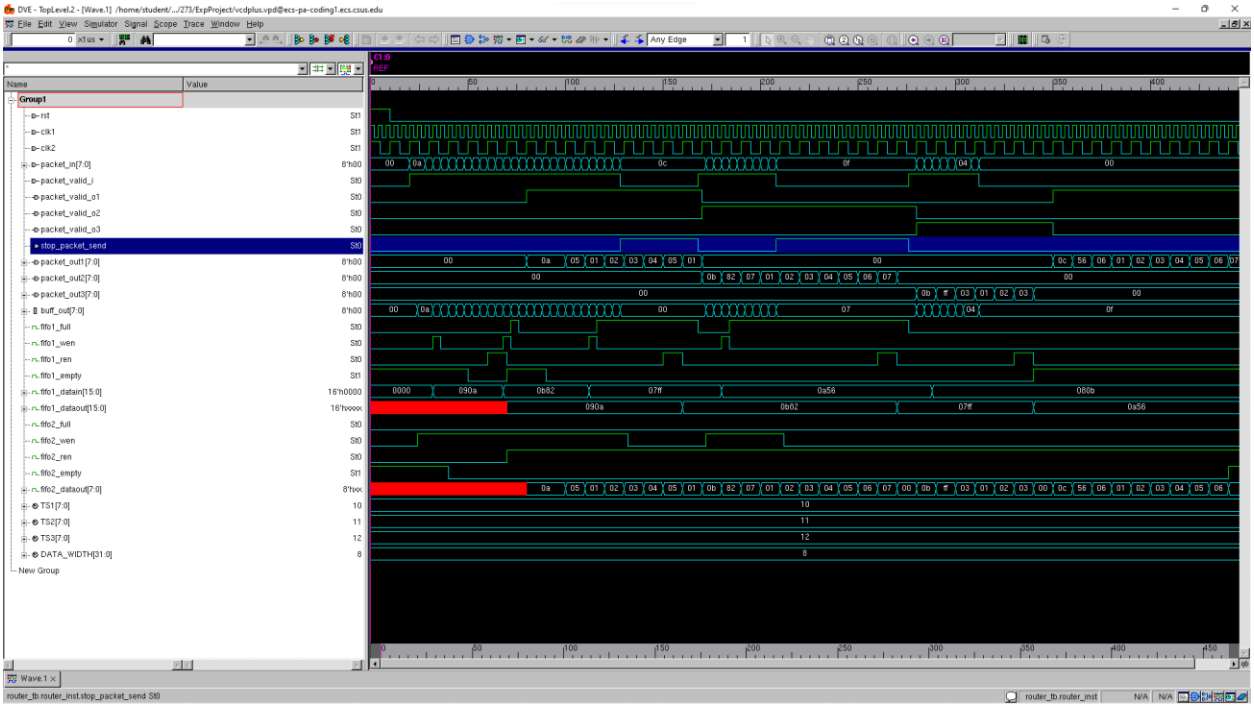
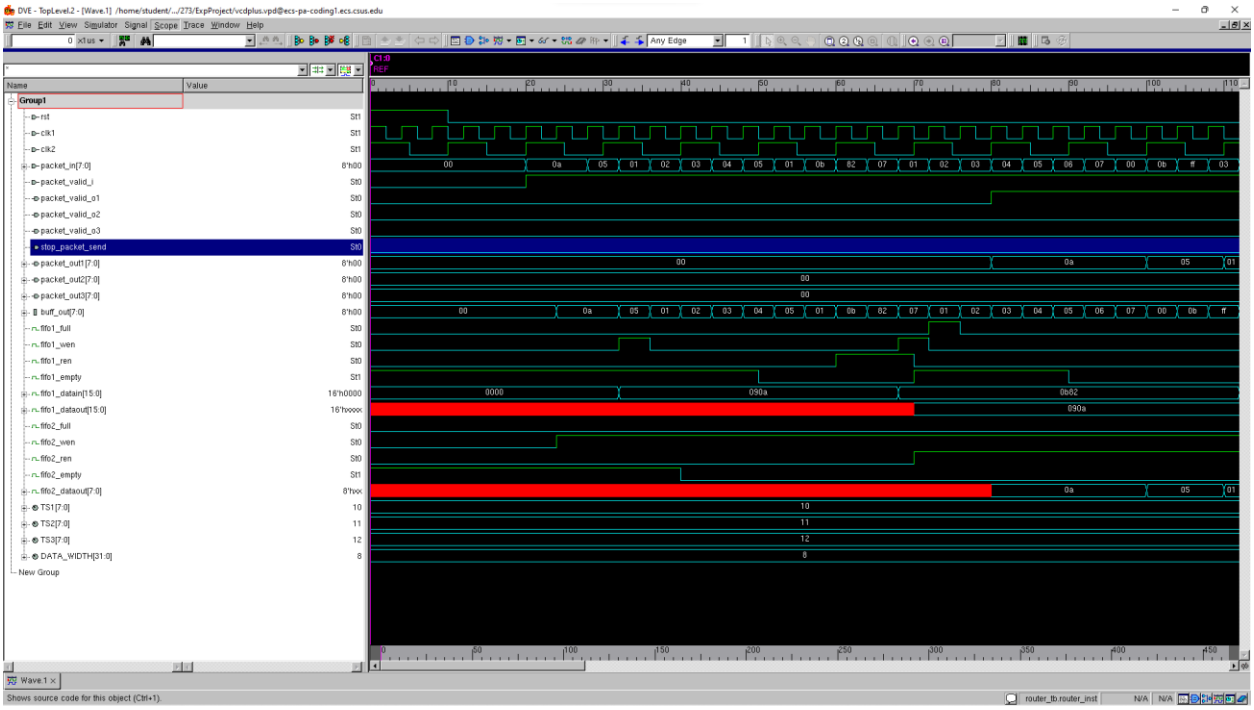
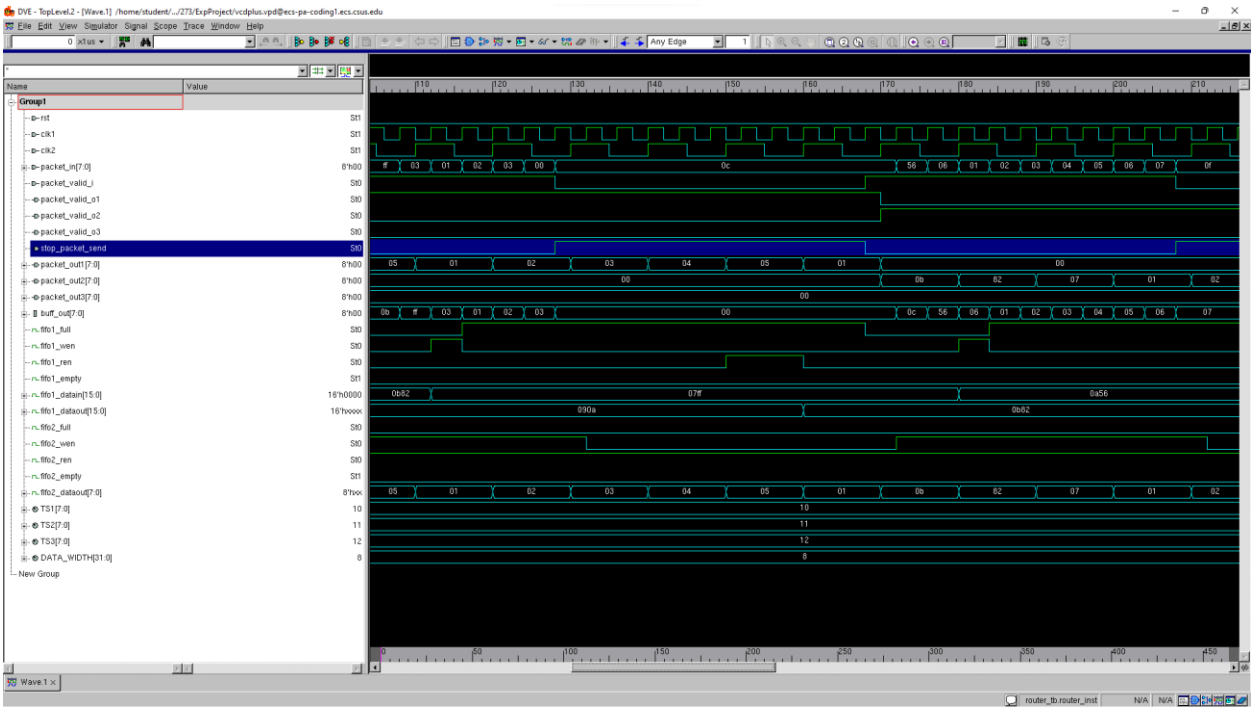
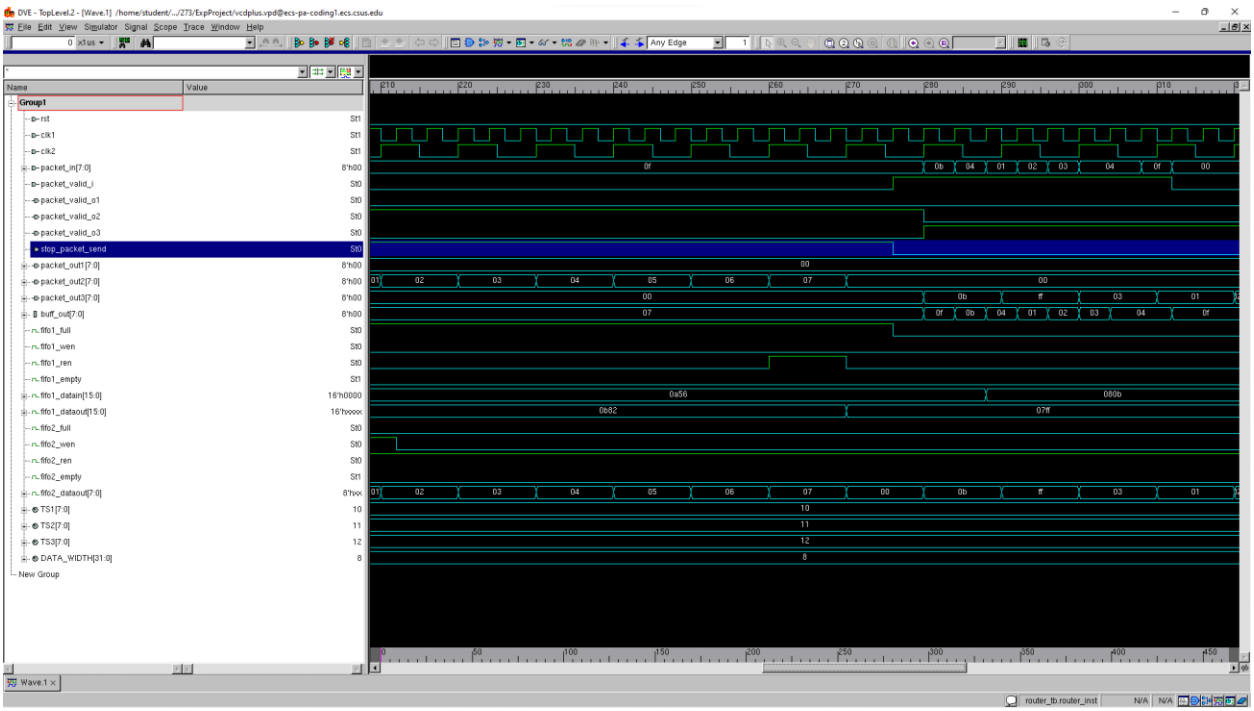
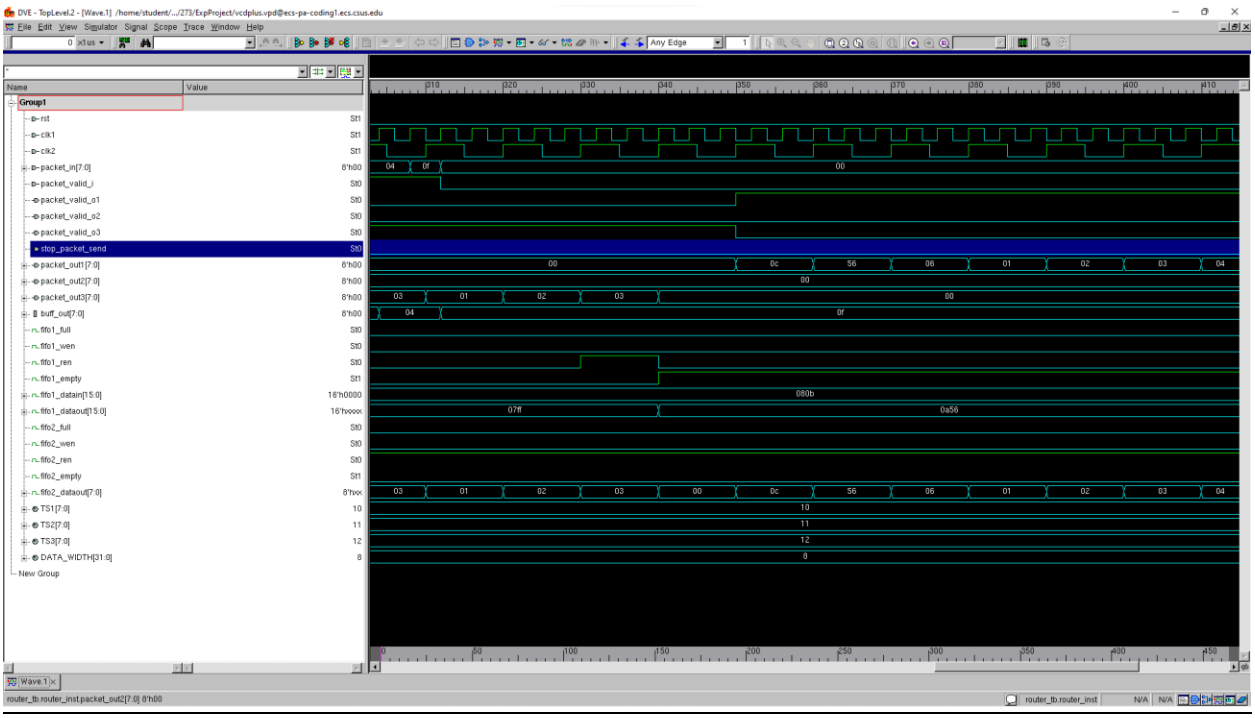



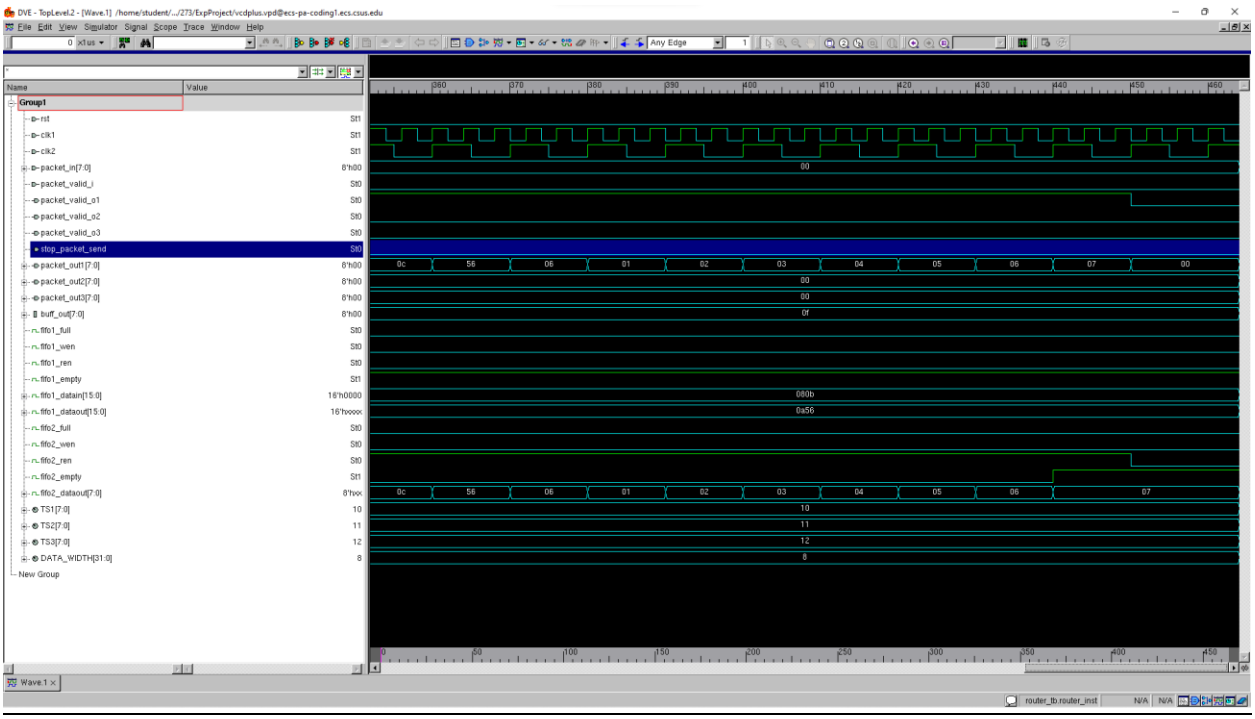

DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
router_tb.router_inst.stop_packet_send St0
router_tb.router_inst


DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
Shows source code for this object (Ctrl+1).
router_tb.router_inst

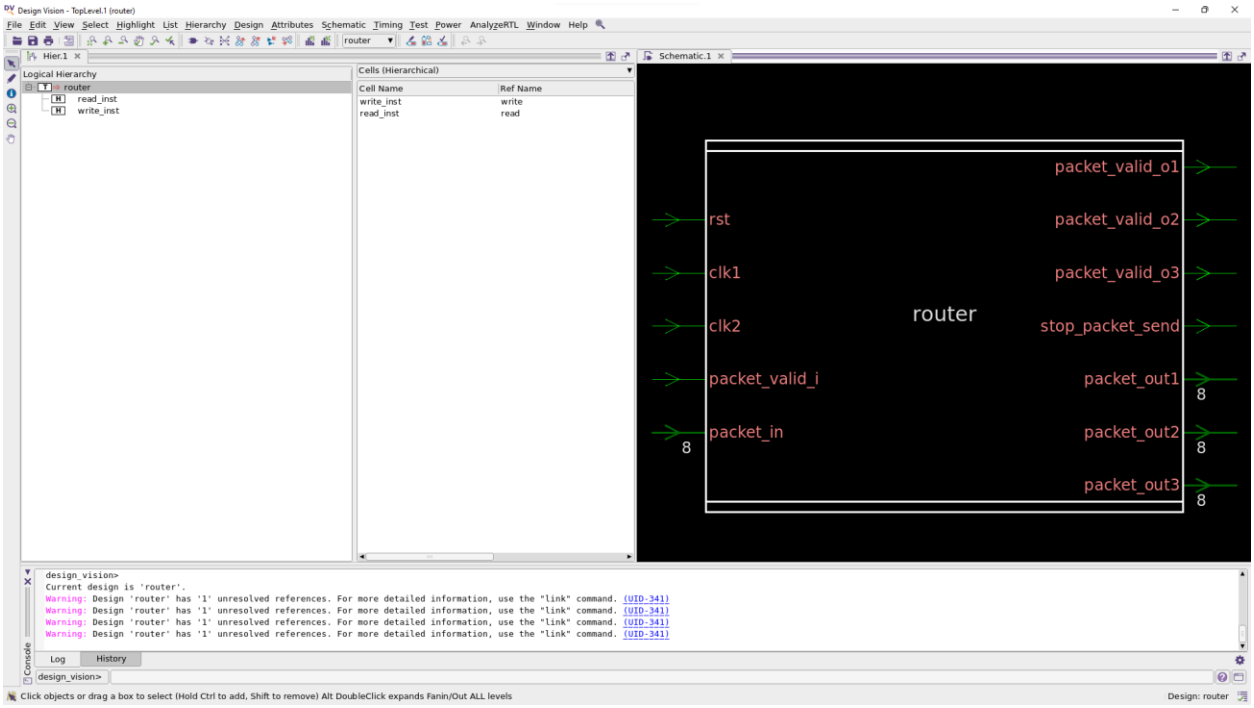

DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
router_tb.router_inst


DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
router_tb.router_inst

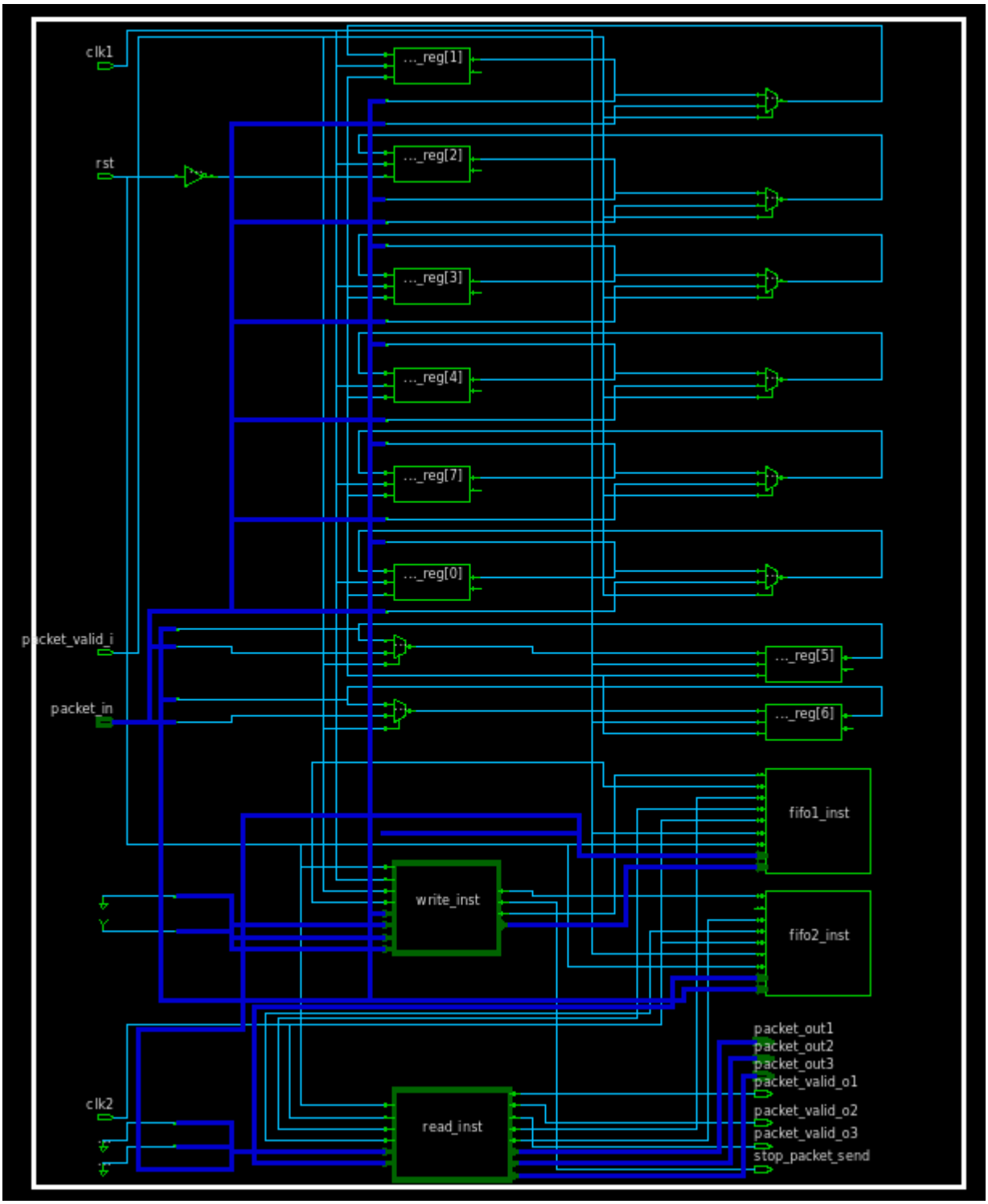

DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
router_tb.router_inst.packet_out2[7:0] 8'h00
router_tb.router_inst


DVE - TopLevel.2 - [Wave.1] /home/student/.../273/ExpProject/vcdplus.vpd@ecs-pa-coding1.ecs.csus.edu
File Edit View Simulator Signal Scope Trace Window Help
Name
Value
Group1
rst
clk1
clk2
packet_in[7:0]
packet_valid_i
packet_valid_o1
packet_valid_o2
packet_valid_o3
stop_packet_send
packet_out1[7:0]
packet_out2[7:0]
packet_out3[7:0]
buff_out[7:0]
fifo1_full
fifo1_wen
fifo1_ren
fifo1_empty
fifo1_datain[15:0]
fifo1_dataout[15:0]
fifo2_full
fifo2_wen
fifo2_ren
fifo2_empty
fifo2_dataout[7:0]
TS1[7:0]
TS2[7:0]
TS3[7:0]
DATA_WIDTH[31:0]
New Group
Wave.1
router_tb.router_inst

Router Synthesis (Schematic):-



Zoom-in View of Detailed Router Synthesis Diagram:-



Synthesis Script (with High Map Effort):

Synthesis Script/Log

```
#Read the design in
read_file -format verilog {"fifo.v"}
read_file -format verilog {"write.v"}
read_file -format verilog {"read.v"}
read_file -format verilog {"router.v"}
#set the current design
set current_design router
#link the design to the libraries
link
#create clock
create_clock "clk1" -period 4 -name "clk1"
set_dont_touch_network "clk1"
create_clock "clk2" -period 10 -name "clk2"
set_dont_touch_network "clk2"
#false path
set_false_path -from clk1 -to clk2
#specify max/min delays for input/output ports
set_input_delay -clock clk1 -max -rise 2 "packet_valid_i"
set_input_delay -clock clk1 -min -rise 1 "packet_valid_i"
set_input_delay -clock clk1 -max -rise 2 "packet_in"
set_input_delay -clock clk1 -min -rise 1 "packet_in"
set_input_delay -clock clk1 -max -rise 2 "rst"
set_input_delay -clock clk1 -min -rise 1 "rst"
set_input_delay -clock clk1 -max -rise 2 "clk1"
set_input_delay -clock clk1 -min -rise 1 "clk1"
set_input_delay -clock clk2 -max -rise 2 "clk2"
set_input_delay -clock clk2 -min -rise 1 "clk2"
set_output_delay -clock clk1 -max -rise 2 "stop_packet_send"
```

```
set_output_delay -clock clk1 -min -rise 1 "stop_packet_send"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o1"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o1"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o2"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o2"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o3"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o3"
set_output_delay -clock clk2 -max -rise 2 "packet_out1"
set_output_delay -clock clk2 -min -rise 1 "packet_out1"
set_output_delay -clock clk2 -max -rise 2 "packet_out2"
set_output_delay -clock clk2 -min -rise 1 "packet_out2"
set_output_delay -clock clk2 -max -rise 2 "packet_out3"
set_output_delay -clock clk2 -min -rise 1 "packet_out3"
#set area constraint to 0 for optimum area
set_max_area 0
#set operating conditions
set_operating_conditions -library "lsi_10k" "BCCOM"
#synthesize
compile -map_effort high -boundary_optimization
#generate reports
report_attribute > report_attribute.txt
report_area > report_area.txt
report_constraints -all_violators > report_constraints.txt
#report_timing -path full -delay max -max_paths 1 -nworst 1 > report_timing.txt
report_timing > report_timing.txt
```

Area Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : area

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 00:55:42 2022

****

Information: Updating design information... (UID-85)

Library(s) Used:

lsi_10k (File: /opt/synopsys/syn/S-2021.06-SP1/libraries/syn/lsi_10k.db)

Number of ports: 152

Number of nets: 441

Number of cells: 306

Number of combinational cells: 225

Number of sequential cells: 75

Number of macros/black boxes: 0

Number of buf/inv: 37

Number of references: 7

Combinational area: 337.000000

Buf/Inv area: 38.000000

Noncombinational area: 473.000000

Macro/Black Box area: 0.000000

Net Interconnect area: undefined (No wire load specified)

Total cell area: 810.000000

Total area: undefined

Information: This design contains black box (unknown) components. (RPT-8)

Timing Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : router
Version: S-2021.06-SP1
Date   : Mon May  2 00:55:42 2022
****************************************

Operating Conditions: BCCOM   Library: lsi_10k
Wire Load Model Mode: top

  Startpoint: packet_valid_i
              (input port clocked by clk1)
  Endpoint: write_inst/cs_reg[1]
            (rising edge-triggered flip-flop clocked by clk1)
  Path Group: clk1
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk1 (rise edge)                   0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     2.00       2.00 r
  packet_valid_i (in)                      0.00       2.00 r
```

write_inst/packet_valid (write) 0.00 2.00 r

write_inst/U21/Z (B4I) 0.08 2.08 f

write_inst/U28/Z (AO4) 0.73 2.81 r

write_inst/U29/Z (AO1P) 0.18 2.99 f

write_inst/U30/Z (IVA) 0.16 3.15 r

write_inst/cs_reg[1]/D (FD2) 0.00 3.15 r

data arrival time 3.15

clock clk1 (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

write_inst/cs_reg[1]/CP (FD2) 0.00 4.00 r

library setup time -0.85 3.15

data required time 3.15

---

data required time 3.15

data arrival time -3.15

---

slack (MET) 0.00

Startpoint: read_inst/packet_counter_reg[5]

(rising edge-triggered flip-flop clocked by clk2)

Endpoint: read_inst/packet_counter_reg[0]

(rising edge-triggered flip-flop clocked by clk2)

Path Group: clk2

Path Type: max

Point Incr Path

---

clock clk2 (rise edge) 0.00 0.00

clock network delay (ideal)	0.00	0.00	
read_inst/packet_counter_reg[5]/CP (FD2)		0.00	0.00 r
read_inst/packet_counter_reg[5]/QN (FD2)		0.96	0.96 f
read_inst/U107/Z (ND4)	0.47	1.43 r	
read_inst/U84/Z (NR4)	0.19	1.62 f	
read_inst/U83/Z (ND2)	0.39	2.01 r	
read_inst/U81/Z (ND2)	0.11	2.12 f	
read_inst/U8/Z (AO3)	1.46	3.58 r	
read_inst/U80/Z (AN3)	0.95	4.53 r	
read_inst/U61/Z (ND2)	0.11	4.64 f	
read_inst/U59/Z (AO3)	0.40	5.04 r	
read_inst/packet_counter_reg[0]/D (FD2)		0.00	5.04 r
data arrival time	5.04		

clock clk2 (rise edge)	10.00	10.00	
clock network delay (ideal)	0.00	10.00	
read_inst/packet_counter_reg[0]/CP (FD2)		0.00	10.00 r
library setup time	-0.85	9.15	
data required time	9.15		

---

data required time	9.15		
data arrival time	-5.04		

---

slack (MET)	4.11		

Constraints Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : constraint

-all_violators

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 00:55:42 2022

****

max_area

Design	Required Area	Actual Area	Slack	
router	0.00	810.00	-810.00	(VIOLATED)

Attributes Report:-

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=16,DEPTH=2". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=8,DEPTH=64". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Warning: Unable to resolve reference 'fifo' in 'router'. (LINK-5)

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : Attribute

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 00:55:42 2022

****

Design	Object	Type	Attribute Name	Value
router	router	design	design_voltage_unit	1000.000000
router	router	design	design_current_unit	0.001000
router	router	design	design_resistance_unit	10000.000000
router	router	design	design_cap_unit	0.000100
router	router	design	design_time_unit	1.000000
router	router	design	compile_cpu_hostname	ecs-pa-coding1.ecs.csus.edu
router	router	design	ice_canonical_xor2_delay	0.537872
router	router	design	ice_canonical_nand2_delay	0.219973
router	router	design	testdb_meth_sig_usage_option	

98307

router router design testdb_meth_sig_usage 106499
router router design testdb_meth_name multiplexed_flip_flop
router router design map_effort_option 3
router router design map true
router router design exact_sequential_map false
router router design pads_thru_hier false
router router design pads_respect_hier false
router router design redundancy_removal true
router router design instance_name_suffix
router router design multibit_mode non_timing_driven
router router design compile_tdrs_cpu_time 0.345882
router router design compile_lib_cpu_time 0.164389
router router design compile_tot_cpu_time 1.638793
router router design compile_rbo_cpu_time 0.502469
router router design compile_abo_cpu_time 0.554005
router router design compile_tot_wall_time 1.903931
router router design temperature_from_min_lib 0.000000
router router design temperature_from_max_lib 0.000000
router router design max_area 0.000000
router router design ungroup_all_option false
router router design scan_state_route_serial false
router router design scan_state_route_clocks false
router router design scan_state_route_enables false
router router design scan_state_type 1
router router design min_wire_load_selection_type
0
router router design wire_load_selection_type 0
router router design hdl_library WORK
router router design hdl_template router
router router design hdl_canonical_default_params

DATA_WIDTH=32'h00000008,TS1=8'h01,TS2=8'h02,TS3=8'h03

router router design hdl_default_parameters TS1 => 8'h01, TS2 => 8'h02, TS3 => 8'h03, DATA_WIDTH => 8

router router design hdl_canonical_params

router router design hdl_parameters

router router design link_design_libraries WORK

router router design presto_gtech_count 12

router buff_out_reg[0] cell ff_edge_sense 1

router buff_out_reg[0] cell hdl_instance_name buff_out_reg[0]

router buff_out_reg[1] cell ff_edge_sense 1

router buff_out_reg[1] cell hdl_instance_name buff_out_reg[1]

router buff_out_reg[2] cell ff_edge_sense 1

router buff_out_reg[2] cell hdl_instance_name buff_out_reg[2]

router buff_out_reg[3] cell ff_edge_sense 1

router buff_out_reg[3] cell hdl_instance_name buff_out_reg[3]

router buff_out_reg[4] cell ff_edge_sense 1

router buff_out_reg[4] cell hdl_instance_name buff_out_reg[4]

router buff_out_reg[5] cell ff_edge_sense 1

router buff_out_reg[5] cell hdl_instance_name buff_out_reg[5]

router buff_out_reg[6] cell ff_edge_sense 1

router buff_out_reg[6] cell hdl_instance_name buff_out_reg[6]

router buff_out_reg[7] cell ff_edge_sense 1

router buff_out_reg[7] cell hdl_instance_name buff_out_reg[7]

router fifo1_inst cell hdl_instance_name fifo1_inst

router fifo1_inst cell array_ref 0

router fifo2_inst cell hdl_instance_name fifo2_inst

router fifo2_inst cell array_ref 0

router read_inst cell hdl_instance_name read_inst

router read_inst cell array_ref 0

router write_inst cell hdl_instance_name write_inst

router write_inst cell array_ref 0
router buff_out[0] net net_original_name buff_out[0]
router buff_out[0] net three_state true
router buff_out[1] net net_original_name buff_out[1]
router buff_out[1] net three_state true
router buff_out[2] net net_original_name buff_out[2]
router buff_out[2] net three_state true
router buff_out[3] net net_original_name buff_out[3]
router buff_out[3] net three_state true
router buff_out[4] net net_original_name buff_out[4]
router buff_out[4] net three_state true
router buff_out[5] net net_original_name buff_out[5]
router buff_out[5] net three_state true
router buff_out[6] net net_original_name buff_out[6]
router buff_out[6] net three_state true
router buff_out[7] net net_original_name buff_out[7]
router buff_out[7] net three_state true
router clk1 net net_original_name clk1
router clk1 net three_state true
router clk2 net net_original_name clk2
router clk2 net three_state true
router fifo1_datain[0] net net_original_name fifo1_datain[0]
router fifo1_datain[0] net three_state true
router fifo1_datain[1] net net_original_name fifo1_datain[1]
router fifo1_datain[1] net three_state true
router fifo1_datain[2] net net_original_name fifo1_datain[2]
router fifo1_datain[2] net three_state true
router fifo1_datain[3] net net_original_name fifo1_datain[3]
router fifo1_datain[3] net three_state true
router fifo1_datain[4] net net_original_name fifo1_datain[4]

router	fifo1_datain[4]	net	three_state	true
router	fifo1_datain[5]	net	net_original_name	fifo1_datain[5]
router	fifo1_datain[5]	net	three_state	true
router	fifo1_datain[6]	net	net_original_name	fifo1_datain[6]
router	fifo1_datain[6]	net	three_state	true
router	fifo1_datain[7]	net	net_original_name	fifo1_datain[7]
router	fifo1_datain[7]	net	three_state	true
router	fifo1_datain[8]	net	net_original_name	fifo1_datain[8]
router	fifo1_datain[8]	net	three_state	true
router	fifo1_datain[9]	net	net_original_name	fifo1_datain[9]
router	fifo1_datain[9]	net	three_state	true
router	fifo1_datain[10]	net	net_original_name	fifo1_datain[10]
router	fifo1_datain[10]	net	three_state	true
router	fifo1_datain[11]	net	net_original_name	fifo1_datain[11]
router	fifo1_datain[11]	net	three_state	true
router	fifo1_datain[12]	net	net_original_name	fifo1_datain[12]
router	fifo1_datain[12]	net	three_state	true
router	fifo1_datain[13]	net	net_original_name	fifo1_datain[13]
router	fifo1_datain[13]	net	three_state	true
router	fifo1_datain[14]	net	net_original_name	fifo1_datain[14]
router	fifo1_datain[14]	net	three_state	true
router	fifo1_datain[15]	net	net_original_name	fifo1_datain[15]
router	fifo1_datain[15]	net	three_state	true
router	fifo1_dataout[0]	net	net_original_name	fifo1_dataout[0]
router	fifo1_dataout[0]	net	three_state	true
router	fifo1_dataout[1]	net	net_original_name	fifo1_dataout[1]
router	fifo1_dataout[1]	net	three_state	true
router	fifo1_dataout[2]	net	net_original_name	fifo1_dataout[2]
router	fifo1_dataout[2]	net	three_state	true
router	fifo1_dataout[3]	net	net_original_name	fifo1_dataout[3]

router fifo1_dataout[3] net three_state true
router fifo1_dataout[4] net net_original_name fifo1_dataout[4]
router fifo1_dataout[4] net three_state true
router fifo1_dataout[5] net net_original_name fifo1_dataout[5]
router fifo1_dataout[5] net three_state true
router fifo1_dataout[6] net net_original_name fifo1_dataout[6]
router fifo1_dataout[6] net three_state true
router fifo1_dataout[7] net net_original_name fifo1_dataout[7]
router fifo1_dataout[7] net three_state true
router fifo1_dataout[8] net net_original_name fifo1_dataout[8]
router fifo1_dataout[8] net three_state true
router fifo1_dataout[9] net net_original_name fifo1_dataout[9]
router fifo1_dataout[9] net three_state true
router fifo1_dataout[10] net net_original_name fifo1_dataout[10]
router fifo1_dataout[10] net three_state true
router fifo1_dataout[11] net net_original_name fifo1_dataout[11]
router fifo1_dataout[11] net three_state true
router fifo1_dataout[12] net net_original_name fifo1_dataout[12]
router fifo1_dataout[12] net three_state true
router fifo1_dataout[13] net net_original_name fifo1_dataout[13]
router fifo1_dataout[13] net three_state true
router fifo1_dataout[14] net net_original_name fifo1_dataout[14]
router fifo1_dataout[14] net three_state true
router fifo1_dataout[15] net net_original_name fifo1_dataout[15]
router fifo1_dataout[15] net three_state true
router fifo1_empty net net_original_name fifo1_empty
router fifo1_empty net three_state true
router fifo1_full net net_original_name fifo1_full
router fifo1_full net three_state true
router fifo1_ren net net_original_name fifo1_ren

router fifo1_ren net three_state true

router fifo1_wen net net_original_name fifo1_wen

router fifo1_wen net three_state true

router fifo2_dataout[0] net net_original_name fifo2_dataout[0]

router fifo2_dataout[0] net three_state true

router fifo2_dataout[1] net net_original_name fifo2_dataout[1]

router fifo2_dataout[1] net three_state true

router fifo2_dataout[2] net net_original_name fifo2_dataout[2]

router fifo2_dataout[2] net three_state true

router fifo2_dataout[3] net net_original_name fifo2_dataout[3]

router fifo2_dataout[3] net three_state true

router fifo2_dataout[4] net net_original_name fifo2_dataout[4]

router fifo2_dataout[4] net three_state true

router fifo2_dataout[5] net net_original_name fifo2_dataout[5]

router fifo2_dataout[5] net three_state true

router fifo2_dataout[6] net net_original_name fifo2_dataout[6]

router fifo2_dataout[6] net three_state true

router fifo2_dataout[7] net net_original_name fifo2_dataout[7]

router fifo2_dataout[7] net three_state true

router fifo2_empty net net_original_name fifo2_empty

router fifo2_empty net three_state true

router fifo2_ren net net_original_name fifo2_ren

router fifo2_ren net three_state true

router fifo2_wen net net_original_name fifo2_wen

router fifo2_wen net three_state true

router packet_in[0] net net_original_name packet_in[0]

router packet_in[1] net net_original_name packet_in[1]

router packet_in[2] net net_original_name packet_in[2]

router packet_in[3] net net_original_name packet_in[3]

router packet_in[4] net net_original_name packet_in[4]

router packet_in[5] net net_original_name packet_in[5]

router packet_in[6] net net_original_name packet_in[6]

router packet_in[7] net net_original_name packet_in[7]

router packet_out1[0] net net_original_name packet_out1[0]

router packet_out1[1] net net_original_name packet_out1[1]

router packet_out1[2] net net_original_name packet_out1[2]

router packet_out1[3] net net_original_name packet_out1[3]

router packet_out1[4] net net_original_name packet_out1[4]

router packet_out1[5] net net_original_name packet_out1[5]

router packet_out1[6] net net_original_name packet_out1[6]

router packet_out1[7] net net_original_name packet_out1[7]

router packet_out2[0] net net_original_name packet_out2[0]

router packet_out2[1] net net_original_name packet_out2[1]

router packet_out2[2] net net_original_name packet_out2[2]

router packet_out2[3] net net_original_name packet_out2[3]

router packet_out2[4] net net_original_name packet_out2[4]

router packet_out2[5] net net_original_name packet_out2[5]

router packet_out2[6] net net_original_name packet_out2[6]

router packet_out2[7] net net_original_name packet_out2[7]

router packet_out3[0] net net_original_name packet_out3[0]

router packet_out3[1] net net_original_name packet_out3[1]

router packet_out3[2] net net_original_name packet_out3[2]

router packet_out3[3] net net_original_name packet_out3[3]

router packet_out3[4] net net_original_name packet_out3[4]

router packet_out3[5] net net_original_name packet_out3[5]

router packet_out3[6] net net_original_name packet_out3[6]

router packet_out3[7] net net_original_name packet_out3[7]

router packet_valid_i net net_original_name packet_valid_i

router packet_valid_o1 net net_original_name packet_valid_o1

router packet_valid_o2 net net_original_name packet_valid_o2

router packet_valid_o3 net net_original_name packet_valid_o3

router rst net net_original_name rst

router rst net three_state true

router stop_packet_send net net_original_name stop_packet_send

router read_inst/clk net three_state true

router read_inst/fifo1_datain[2]
net three_state true

router read_inst/fifo1_datain[3]
net three_state true

router read_inst/fifo1_datain[4]
net three_state true

router read_inst/fifo1_datain[5]
net three_state true

router read_inst/fifo1_datain[6]
net three_state true

router read_inst/fifo1_datain[7]
net three_state true

router read_inst/fifo1_datain[8]
net three_state true

router read_inst/fifo1_datain[9]
net three_state true

router read_inst/fifo1_datain[10]
net three_state true

router read_inst/fifo1_datain[11]
net three_state true

router read_inst/fifo1_datain[12]
net three_state true

router read_inst/fifo1_datain[13]
net three_state true

router read_inst/fifo1_datain[14]

net three_state true

router read_inst/fifo1_datain[15]

net three_state true

router read_inst/fifo1_empty

net three_state true

router read_inst/fifo1_ren

net three_state true

router read_inst/packet_datain[0]

net three_state true

router read_inst/packet_datain[1]

net three_state true

router read_inst/packet_datain[2]

net three_state true

router read_inst/packet_datain[3]

net three_state true

router read_inst/packet_datain[4]

net three_state true

router read_inst/packet_datain[5]

net three_state true

router read_inst/packet_datain[6]

net three_state true

router read_inst/packet_datain[7]

net three_state true

router read_inst/packet_empty

net three_state true

router read_inst/packet_ren

net three_state true

router read_inst/rst net three_state true

router write_inst/N54 net three_state true

router write_inst/N55 net three_state true

router write_inst/add_97/carry[3]
net three_state true
router write_inst/buff_out[3]
net three_state true
router write_inst/buff_out[4]
net three_state true
router write_inst/buff_out[5]
net three_state true
router write_inst/buff_out[6]
net three_state true
router write_inst/buff_out[7]
net three_state true
router write_inst/clk net three_state true
router write_inst/fifo1_datain[0]
net three_state true
router write_inst/fifo1_datain[1]
net three_state true
router write_inst/fifo1_datain[2]
net three_state true
router write_inst/fifo1_datain[3]
net three_state true
router write_inst/fifo1_datain[4]
net three_state true
router write_inst/fifo1_datain[5]
net three_state true
router write_inst/fifo1_datain[6]
net three_state true
router write_inst/fifo1_datain[7]
net three_state true
router write_inst/fifo1_datain[8]

net three_state true

router write_inst/fifo1_datain[9]

net three_state true

router write_inst/fifo1_datain[10]

net three_state true

router write_inst/fifo1_datain[11]

net three_state true

router write_inst/fifo1_datain[12]

net three_state true

router write_inst/fifo1_datain[13]

net three_state true

router write_inst/fifo1_datain[14]

net three_state true

router write_inst/fifo1_datain[15]

net three_state true

router write_inst/fifo1_full

net three_state true

router write_inst/fifo1_wen

net three_state true

router write_inst/fifo2_wen

net three_state true

router write_inst/rst net three_state true

router buff_out_reg[2]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[1]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[3]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[4]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[5]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[0]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[6]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[7]/CP pin pin_on_clock_network_per_scn
true
router read_inst/clk pin pin_on_clock_network_per_scn
true
router write_inst/clk pin pin_on_clock_network_per_scn
true
router fifo2_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo2_inst/write_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/write_clk
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[0]/CP
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[1]/CP
pin pin_on_clock_network_per_scn
true

router read_inst/packet_counter_reg[2]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[3]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[4]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[5]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[6]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/select_output_reg_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/select_output_reg_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router write_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

```
router      write_inst/cs_reg[1]/CP
                pin     pin_on_clock_network_per_scn
                                true
router      write_inst/data_counter_reg[2]/CP
                pin     pin_on_clock_network_per_scn
                                true
router      write_inst/data_counter_reg[1]/CP
                pin     pin_on_clock_network_per_scn
                                true
router      write_inst/data_counter_reg[0]/CP
                pin     pin_on_clock_network_per_scn
                                true
router      read_inst/clear_packet_count_reg
                cell    hdl_instance_name       clear_packet_count_reg
router      read_inst/cs_reg[0]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[0]
                cell    hdl_instance_name       cs_reg[0]
router      read_inst/cs_reg[1]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[1]
                cell    hdl_instance_name       cs_reg[1]
router      read_inst/cs_reg[2]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[2]
                cell    hdl_instance_name       cs_reg[2]
router      read_inst/fifo1_ren_reg
                cell    hdl_instance_name       fifo1_ren_reg
router      read_inst/load_packet_count_reg
                cell    hdl_instance_name       load_packet_count_reg
```

```
router      read_inst/packet_counter_reg[0]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[0]
                cell    hdl_instance_name   packet_counter_reg[0]
router      read_inst/packet_counter_reg[1]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[1]
                cell    hdl_instance_name   packet_counter_reg[1]
router      read_inst/packet_counter_reg[2]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[2]
                cell    hdl_instance_name   packet_counter_reg[2]
router      read_inst/packet_counter_reg[3]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[3]
                cell    hdl_instance_name   packet_counter_reg[3]
router      read_inst/packet_counter_reg[4]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[4]
                cell    hdl_instance_name   packet_counter_reg[4]
router      read_inst/packet_counter_reg[5]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[5]
                cell    hdl_instance_name   packet_counter_reg[5]
router      read_inst/packet_counter_reg[6]
                cell    ff_edge_sense       1
router      read_inst/packet_counter_reg[6]
                cell    hdl_instance_name   packet_counter_reg[6]
router      read_inst/packet_counter_reg[7]
                cell    ff_edge_sense       1
```

```
router      read_inst/packet_counter_reg[7]
                cell    hdl_instance_name       packet_counter_reg[7]
router      read_inst/packet_dec_en_reg
                cell    hdl_instance_name       packet_dec_en_reg
router      read_inst/packet_ren_reg
                cell    hdl_instance_name       packet_ren_reg
router      read_inst/packet_valid_reg
                cell    hdl_instance_name       packet_valid_reg
router      read_inst/select_output_reg[0]
                cell    hdl_instance_name       select_output_reg[0]
router      read_inst/select_output_reg[1]
                cell    hdl_instance_name       select_output_reg[1]
router      read_inst/select_output_reg_reg[0]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[0]
                cell    hdl_instance_name       select_output_reg_reg[0]
router      read_inst/select_output_reg_reg[1]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[1]
                cell    hdl_instance_name       select_output_reg_reg[1]
router      read_inst/temp_packet_data_reg[0]
                cell    hdl_instance_name       temp_packet_data_reg[0]
router      read_inst/temp_packet_data_reg[1]
                cell    hdl_instance_name       temp_packet_data_reg[1]
router      read_inst/temp_packet_data_reg[2]
                cell    hdl_instance_name       temp_packet_data_reg[2]
router      read_inst/temp_packet_data_reg[3]
                cell    hdl_instance_name       temp_packet_data_reg[3]
router      read_inst/temp_packet_data_reg[4]
                cell    hdl_instance_name       temp_packet_data_reg[4]
```

```
router      read_inst/temp_packet_data_reg[5]
                cell    hdl_instance_name       temp_packet_data_reg[5]
router      read_inst/temp_packet_data_reg[6]
                cell    hdl_instance_name       temp_packet_data_reg[6]
router      read_inst/temp_packet_data_reg[7]
                cell    hdl_instance_name       temp_packet_data_reg[7]
router      write_inst/clear_data_count_reg
                cell    hdl_instance_name       clear_data_count_reg
router      write_inst/cs_reg[0]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[0]
                cell    hdl_instance_name       cs_reg[0]
router      write_inst/cs_reg[1]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[1]
                cell    hdl_instance_name       cs_reg[1]
router      write_inst/cs_reg[2]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[2]
                cell    hdl_instance_name       cs_reg[2]
router      write_inst/data_counter_reg[0]
                cell    ff_edge_sense           1
router      write_inst/data_counter_reg[0]
                cell    hdl_instance_name       data_counter_reg[0]
router      write_inst/data_counter_reg[1]
                cell    ff_edge_sense           1
router      write_inst/data_counter_reg[1]
                cell    hdl_instance_name       data_counter_reg[1]
router      write_inst/data_counter_reg[2]
                cell    ff_edge_sense           1
```

```
router      write_inst/data_counter_reg[2]
                cell    hdl_instance_name       data_counter_reg[2]
router      write_inst/fifo1_datain_reg[0]
                cell    hdl_instance_name       fifo1_datain_reg[0]
router      write_inst/fifo1_datain_reg[1]
                cell    hdl_instance_name       fifo1_datain_reg[1]
router      write_inst/fifo1_datain_reg[2]
                cell    hdl_instance_name       fifo1_datain_reg[2]
router      write_inst/fifo1_datain_reg[3]
                cell    hdl_instance_name       fifo1_datain_reg[3]
router      write_inst/fifo1_datain_reg[4]
                cell    hdl_instance_name       fifo1_datain_reg[4]
router      write_inst/fifo1_datain_reg[5]
                cell    hdl_instance_name       fifo1_datain_reg[5]
router      write_inst/fifo1_datain_reg[6]
                cell    hdl_instance_name       fifo1_datain_reg[6]
router      write_inst/fifo1_datain_reg[7]
                cell    hdl_instance_name       fifo1_datain_reg[7]
router      write_inst/fifo1_datain_reg[8]
                cell    hdl_instance_name       fifo1_datain_reg[8]
router      write_inst/fifo1_datain_reg[9]
                cell    hdl_instance_name       fifo1_datain_reg[9]
router      write_inst/fifo1_datain_reg[10]
                cell    hdl_instance_name       fifo1_datain_reg[10]
router      write_inst/fifo1_datain_reg[11]
                cell    hdl_instance_name       fifo1_datain_reg[11]
router      write_inst/fifo1_datain_reg[12]
                cell    hdl_instance_name       fifo1_datain_reg[12]
router      write_inst/fifo1_datain_reg[13]
                cell    hdl_instance_name       fifo1_datain_reg[13]
```

router write_inst/fifo1_datain_reg[14]

cell hdl_instance_name fifo1_datain_reg[14]

router write_inst/fifo1_datain_reg[15]

cell hdl_instance_name fifo1_datain_reg[15]

router write_inst/fifo1_valid_reg

cell hdl_instance_name fifo1_valid_reg

router write_inst/fifo1_wen_reg

cell hdl_instance_name fifo1_wen_reg

router write_inst/fifo2_wen_reg

cell hdl_instance_name fifo2_wen_reg

router write_inst/load_data_count_reg

cell hdl_instance_name load_data_count_reg

router write_inst/stop_packet_reg

cell hdl_instance_name stop_packet_reg

router write_inst/temp_fifo1_reg[0]

cell hdl_instance_name temp_fifo1_reg[0]

router write_inst/temp_fifo1_reg[1]

cell hdl_instance_name temp_fifo1_reg[1]

router write_inst/temp_fifo1_reg[2]

cell hdl_instance_name temp_fifo1_reg[2]

router write_inst/temp_fifo1_reg[3]

cell hdl_instance_name temp_fifo1_reg[3]

router write_inst/temp_fifo1_reg[4]

cell hdl_instance_name temp_fifo1_reg[4]

router write_inst/temp_fifo1_reg[5]

cell hdl_instance_name temp_fifo1_reg[5]

router write_inst/temp_fifo1_reg[6]

cell hdl_instance_name temp_fifo1_reg[6]

router write_inst/temp_fifo1_reg[7]

cell hdl_instance_name temp_fifo1_reg[7]

router read_inst/N30 net net_original_name SUM(1)

router read_inst/N32 net net_original_name SUM(3)

router read_inst/N34 net net_original_name SUM(5)

router read_inst/N35 net net_original_name SUM(6)

router read_inst/N36 net net_original_name SUM(7)

router read_inst/clk net net_original_name clk

router read_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router read_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router read_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router read_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router read_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router read_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router read_inst/fifo1_datain[8]

net net_original_name fifo1_datain[8]

router read_inst/fifo1_datain[9]

net net_original_name fifo1_datain[9]

router read_inst/fifo1_datain[10]

net net_original_name fifo1_datain[10]

router read_inst/fifo1_datain[11]

net net_original_name fifo1_datain[11]

router read_inst/fifo1_datain[12]

net net_original_name fifo1_datain[12]

router read_inst/fifo1_datain[13]

net net_original_name fifo1_datain[13]

router read_inst/fifo1_datain[14]
net net_original_name fifo1_datain[14]
router read_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router read_inst/fifo1_empty
net net_original_name fifo1_empty
router read_inst/fifo1_ren
net net_original_name fifo1_ren
router read_inst/ns[0] net net_original_name ns[0]
router read_inst/ns[1] net net_original_name ns[1]
router read_inst/ns[2] net net_original_name ns[2]
router read_inst/packet_counter[1]
net net_original_name packet_counter[1]
router read_inst/packet_counter[2]
net net_original_name packet_counter[2]
router read_inst/packet_counter[3]
net net_original_name packet_counter[3]
router read_inst/packet_counter[4]
net net_original_name packet_counter[4]
router read_inst/packet_counter[6]
net net_original_name packet_counter[6]
router read_inst/packet_counter[7]
net net_original_name packet_counter[7]
router read_inst/packet_datain[0]
net net_original_name packet_datain[0]
router read_inst/packet_datain[1]
net net_original_name packet_datain[1]
router read_inst/packet_datain[2]
net net_original_name packet_datain[2]
router read_inst/packet_datain[3]

net net_original_name packet_datain[3]

router read_inst/packet_datain[4]

net net_original_name packet_datain[4]

router read_inst/packet_datain[5]

net net_original_name packet_datain[5]

router read_inst/packet_datain[6]

net net_original_name packet_datain[6]

router read_inst/packet_datain[7]

net net_original_name packet_datain[7]

router read_inst/packet_empty

net net_original_name packet_empty

router read_inst/packet_output_1[0]

net net_original_name packet_output_1[0]

router read_inst/packet_output_1[1]

net net_original_name packet_output_1[1]

router read_inst/packet_output_1[2]

net net_original_name packet_output_1[2]

router read_inst/packet_output_1[3]

net net_original_name packet_output_1[3]

router read_inst/packet_output_1[4]

net net_original_name packet_output_1[4]

router read_inst/packet_output_1[5]

net net_original_name packet_output_1[5]

router read_inst/packet_output_1[6]

net net_original_name packet_output_1[6]

router read_inst/packet_output_1[7]

net net_original_name packet_output_1[7]

router read_inst/packet_output_2[0]

net net_original_name packet_output_2[0]

router read_inst/packet_output_2[1]

net net_original_name packet_output_2[1]
router read_inst/packet_output_2[2]
net net_original_name packet_output_2[2]
router read_inst/packet_output_2[3]
net net_original_name packet_output_2[3]
router read_inst/packet_output_2[4]
net net_original_name packet_output_2[4]
router read_inst/packet_output_2[5]
net net_original_name packet_output_2[5]
router read_inst/packet_output_2[6]
net net_original_name packet_output_2[6]
router read_inst/packet_output_2[7]
net net_original_name packet_output_2[7]
router read_inst/packet_output_3[0]
net net_original_name packet_output_3[0]
router read_inst/packet_output_3[1]
net net_original_name packet_output_3[1]
router read_inst/packet_output_3[2]
net net_original_name packet_output_3[2]
router read_inst/packet_output_3[3]
net net_original_name packet_output_3[3]
router read_inst/packet_output_3[4]
net net_original_name packet_output_3[4]
router read_inst/packet_output_3[5]
net net_original_name packet_output_3[5]
router read_inst/packet_output_3[6]
net net_original_name packet_output_3[6]
router read_inst/packet_output_3[7]
net net_original_name packet_output_3[7]
router read_inst/packet_ren

net net_original_name packet_ren

router read_inst/packet_valid_o1

net net_original_name packet_valid_o1

router read_inst/packet_valid_o2

net net_original_name packet_valid_o2

router read_inst/packet_valid_o3

net net_original_name packet_valid_o3

router read_inst/rst net net_original_name rst

router read_inst/select_output[0]

net net_original_name select_output[0]

router read_inst/select_output[1]

net net_original_name select_output[1]

router read_inst/select_output_reg[0]

net net_original_name select_output_reg[0]

router read_inst/select_output_reg[1]

net net_original_name select_output_reg[1]

router write_inst/N54 net net_original_name SUM(0)

router write_inst/N55 net net_original_name SUM(1)

router write_inst/N57 net net_original_name SUM(3)

router write_inst/N58 net net_original_name SUM(4)

router write_inst/N59 net net_original_name SUM(5)

router write_inst/N60 net net_original_name SUM(6)

router write_inst/N61 net net_original_name SUM(7)

router write_inst/add_97/carry[3]

net net_original_name carry(3)

router write_inst/add_97/carry[4]

net net_original_name carry(4)

router write_inst/add_97/carry[5]

net net_original_name carry(5)

router write_inst/add_97/carry[6]

net net_original_name carry(6)

router write_inst/add_97/carry[7]

net net_original_name carry(7)

router write_inst/buff_out[3]

net net_original_name buff_out[3]

router write_inst/buff_out[4]

net net_original_name buff_out[4]

router write_inst/buff_out[5]

net net_original_name buff_out[5]

router write_inst/buff_out[6]

net net_original_name buff_out[6]

router write_inst/buff_out[7]

net net_original_name buff_out[7]

router write_inst/clk net net_original_name clk

router write_inst/fifo1_datain[0]

net net_original_name fifo1_datain[0]

router write_inst/fifo1_datain[1]

net net_original_name fifo1_datain[1]

router write_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router write_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router write_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router write_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router write_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router write_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router write_inst/fifo1_datain[8]
net net_original_name fifo1_datain[8]
router write_inst/fifo1_datain[9]
net net_original_name fifo1_datain[9]
router write_inst/fifo1_datain[10]
net net_original_name fifo1_datain[10]
router write_inst/fifo1_datain[11]
net net_original_name fifo1_datain[11]
router write_inst/fifo1_datain[12]
net net_original_name fifo1_datain[12]
router write_inst/fifo1_datain[13]
net net_original_name fifo1_datain[13]
router write_inst/fifo1_datain[14]
net net_original_name fifo1_datain[14]
router write_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router write_inst/fifo1_full
net net_original_name fifo1_full
router write_inst/fifo1_wen
net net_original_name fifo1_wen
router write_inst/fifo2_wen
net net_original_name fifo2_wen
router write_inst/ns[0] net net_original_name ns[0]
router write_inst/ns[1] net net_original_name ns[1]
router write_inst/ns[2] net net_original_name ns[2]
router write_inst/packet_valid
net net_original_name packet_valid
router write_inst/rst net net_original_name rst
router write_inst/stop_packet
net net_original_name stop_packet

```
router    clk1          port    pin_on_clock_network_per_scn
                                        true
router    clk1          port    hdl_instance_name       clk1
router    clk2          port    pin_on_clock_network_per_scn
                                        true
router    clk2          port    hdl_instance_name       clk2
router    packet_in[0]    port    hdl_instance_name     packet_in[0]
router    packet_in[1]    port    hdl_instance_name     packet_in[1]
router    packet_in[2]    port    hdl_instance_name     packet_in[2]
router    packet_in[3]    port    hdl_instance_name     packet_in[3]
router    packet_in[4]    port    hdl_instance_name     packet_in[4]
router    packet_in[5]    port    hdl_instance_name     packet_in[5]
router    packet_in[6]    port    hdl_instance_name     packet_in[6]
router    packet_in[7]    port    hdl_instance_name     packet_in[7]
router    packet_out1[0]  port    hdl_instance_name     packet_out1[0]
router    packet_out1[1]  port    hdl_instance_name     packet_out1[1]
router    packet_out1[2]  port    hdl_instance_name     packet_out1[2]
router    packet_out1[3]  port    hdl_instance_name     packet_out1[3]
router    packet_out1[4]  port    hdl_instance_name     packet_out1[4]
router    packet_out1[5]  port    hdl_instance_name     packet_out1[5]
router    packet_out1[6]  port    hdl_instance_name     packet_out1[6]
router    packet_out1[7]  port    hdl_instance_name     packet_out1[7]
router    packet_out2[0]  port    hdl_instance_name     packet_out2[0]
router    packet_out2[1]  port    hdl_instance_name     packet_out2[1]
router    packet_out2[2]  port    hdl_instance_name     packet_out2[2]
router    packet_out2[3]  port    hdl_instance_name     packet_out2[3]
router    packet_out2[4]  port    hdl_instance_name     packet_out2[4]
router    packet_out2[5]  port    hdl_instance_name     packet_out2[5]
router    packet_out2[6]  port    hdl_instance_name     packet_out2[6]
router    packet_out2[7]  port    hdl_instance_name     packet_out2[7]
```

router packet_out3[0] port hdl_instance_name packet_out3[0]

router packet_out3[1] port hdl_instance_name packet_out3[1]

router packet_out3[2] port hdl_instance_name packet_out3[2]

router packet_out3[3] port hdl_instance_name packet_out3[3]

router packet_out3[4] port hdl_instance_name packet_out3[4]

router packet_out3[5] port hdl_instance_name packet_out3[5]

router packet_out3[6] port hdl_instance_name packet_out3[6]

router packet_out3[7] port hdl_instance_name packet_out3[7]

router packet_valid_i port hdl_instance_name packet_valid_i

router packet_valid_o1 port hdl_instance_name packet_valid_o1

router packet_valid_o2 port hdl_instance_name packet_valid_o2

router packet_valid_o3 port hdl_instance_name packet_valid_o3

router rst port hdl_instance_name rst

router stop_packet_send port hdl_instance_name stop_packet_send

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000010,DEPTH=32'h00000002

router fifo reference hdl_parameters DATA_WIDTH=16,DEPTH=2

router fifo reference hdl_template fifo

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000008,DEPTH=32'h00000040

router fifo reference hdl_parameters DATA_WIDTH=8,DEPTH=64

router fifo reference hdl_template fifo

Synthesis Script (with Medium Map Effort):

Synthesis Script/Log

```
#Read the design in
read_file -format verilog {"fifo.v"}
read_file -format verilog {"write.v"}
read_file -format verilog {"read.v"}
read_file -format verilog {"router.v"}
#set the current design
set current_design router
#link the design to the libraries
link
#create clock
create_clock "clk1" -period 4 -name "clk1"
set_dont_touch_network "clk1"
create_clock "clk2" -period 10 -name "clk2"
set_dont_touch_network "clk2"
#false path
set_false_path -from clk1 -to clk2
#specify max/min delays for input/output ports
set_input_delay -clock clk1 -max -rise 2 "packet_valid_i"
set_input_delay -clock clk1 -min -rise 1 "packet_valid_i"
set_input_delay -clock clk1 -max -rise 2 "packet_in"
set_input_delay -clock clk1 -min -rise 1 "packet_in"
set_input_delay -clock clk1 -max -rise 2 "rst"
set_input_delay -clock clk1 -min -rise 1 "rst"
set_input_delay -clock clk1 -max -rise 2 "clk1"
set_input_delay -clock clk1 -min -rise 1 "clk1"
set_input_delay -clock clk2 -max -rise 2 "clk2"
set_input_delay -clock clk2 -min -rise 1 "clk2"
set_output_delay -clock clk1 -max -rise 2 "stop_packet_send"
```

```
set_output_delay -clock clk1 -min -rise 1 "stop_packet_send"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o1"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o1"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o2"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o2"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o3"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o3"
set_output_delay -clock clk2 -max -rise 2 "packet_out1"
set_output_delay -clock clk2 -min -rise 1 "packet_out1"
set_output_delay -clock clk2 -max -rise 2 "packet_out2"
set_output_delay -clock clk2 -min -rise 1 "packet_out2"
set_output_delay -clock clk2 -max -rise 2 "packet_out3"
set_output_delay -clock clk2 -min -rise 1 "packet_out3"
#set area constraint to 0 for optimum area
set_max_area 0
#set operating conditions
set_operating_conditions -library "lsi_10k" "BCCOM"
#synthesize
compile -map_effort medium -boundary_optimization
#generate reports
report_attribute > report_attribute.txt
report_area > report_area.txt
report_constraints -all_violators > report_constraints.txt
#report_timing -path full -delay max -max_paths 1 -nworst 1 > report_timing.txt
report_timing > report_timing.txt
```

Area Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

```
****************************************
Report : area
Design : router
Version: S-2021.06-SP1
Date   : Mon May  2 01:09:47 2022
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    lsi_10k (File: /opt/synopsys/syn/S-2021.06-SP1/libraries/syn/lsi_10k.db)

Number of ports:                  152
Number of nets:                   449
Number of cells:                  314
Number of combinational cells:    233
Number of sequential cells:        75
Number of macros/black boxes:       0
Number of buf/inv:                 44
Number of references:               7

Combinational area:        342.000000
Buf/Inv area:               45.000000
Noncombinational area:     473.000000
Macro/Black Box area:        0.000000
Net Interconnect area:      undefined  (No wire load specified)
```

Total cell area: 815.000000

Total area: undefined

Information: This design contains black box (unknown) components. (RPT-8)

Timing Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : timing

-path full

-delay max

-max_paths 1

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:09:47 2022

****

Operating Conditions: BCCOM Library: lsi_10k

Wire Load Model Mode: top

Startpoint: packet_valid_i

(input port clocked by clk1)

Endpoint: write_inst/cs_reg[1]

(rising edge-triggered flip-flop clocked by clk1)

Path Group: clk1

Path Type: max

Point	Incr	Path
clock clk1 (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	2.00	2.00 r
packet_valid_i (in)	0.00	2.00 r
write_inst/packet_valid (write)	0.00	2.00 r

write_inst/U19/Z (B4I) 0.08 2.08 f

write_inst/U32/Z (AO4) 0.73 2.81 r

write_inst/U33/Z (AO1P) 0.18 2.99 f

write_inst/U34/Z (IVA) 0.16 3.15 r

write_inst/cs_reg[1]/D (FD2) 0.00 3.15 r

data arrival time 3.15

clock clk1 (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

write_inst/cs_reg[1]/CP (FD2) 0.00 4.00 r

library setup time -0.85 3.15

data required time 3.15

---

data required time 3.15

data arrival time -3.15

---

slack (MET) 0.00

Startpoint: read_inst/packet_counter_reg[5]

(rising edge-triggered flip-flop clocked by clk2)

Endpoint: read_inst/packet_counter_reg[0]

(rising edge-triggered flip-flop clocked by clk2)

Path Group: clk2

Path Type: max

Point Incr Path

---

clock clk2 (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

read_inst/packet_counter_reg[5]/CP (FD2)	0.00	0.00	r
read_inst/packet_counter_reg[5]/QN (FD2)	0.96	0.96	f
read_inst/U110/Z (ND4)	0.47	1.43	r
read_inst/U85/Z (NR4)	0.19	1.62	f
read_inst/U84/Z (ND2)	0.39	2.01	r
read_inst/U82/Z (ND2)	0.11	2.12	f
read_inst/U4/Z (AO3)	1.46	3.58	r
read_inst/U81/Z (AN3)	0.95	4.53	r
read_inst/U62/Z (ND2)	0.11	4.64	f
read_inst/U60/Z (AO3)	0.40	5.04	r
read_inst/packet_counter_reg[0]/D (FD2)	0.00	5.04	r
data arrival time	5.04		

clock clk2 (rise edge)	10.00	10.00	
clock network delay (ideal)	0.00	10.00	
read_inst/packet_counter_reg[0]/CP (FD2)	0.00	10.00	r
library setup time	-0.85	9.15	
data required time	9.15		

---

data required time	9.15		
data arrival time	-5.04		

---

slack (MET)	4.11		

Constraints Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : constraint

-all_violators

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:09:47 2022

****

max_area

Design	Required Area	Actual Area	Slack	
router	0.00	815.00	-815.00	(VIOLATED)

Attribute Report:

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=16,DEPTH=2". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=8,DEPTH=64". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Warning: Unable to resolve reference 'fifo' in 'router'. (LINK-5)

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : Attribute

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:09:47 2022

****

Design	Object	Type	Attribute Name	Value
router	router	design	design_voltage_unit	1000.000000
router	router	design	design_current_unit	0.001000
router	router	design	design_resistance_unit	10000.000000
router	router	design	design_cap_unit	0.000100
router	router	design	design_time_unit	1.000000
router	router	design	compile_cpu_hostname	ecs-pa-coding1.ecs.csus.edu
router	router	design	ice_canonical_xor2_delay	0.537872
router	router	design	ice_canonical_nand2_delay	0.219973
router	router	design	testdb_meth_sig_usage_option	98307
router	router	design	testdb_meth_sig_usage	106499

router router design testdb_meth_name multiplexed_flip_flop

router router design map_effort_option 2

router router design map true

router router design exact_sequential_map false

router router design pads_thru_hier false

router router design pads_respect_hier false

router router design redundancy_removal true

router router design instance_name_suffix

router router design multibit_mode non_timing_driven

router router design compile_tdrs_cpu_time 0.338829

router router design compile_lib_cpu_time 0.154404

router router design compile_tot_cpu_time 1.315130

router router design compile_rbo_cpu_time 0.206198

router router design compile_abo_cpu_time 0.540298

router router design compile_tot_wall_time 1.562788

router router design temperature_from_min_lib 0.000000

router router design temperature_from_max_lib 0.000000

router router design max_area 0.000000

router router design ungroup_all_option false

router router design scan_state_route_serial false

router router design scan_state_route_clocks false

router router design scan_state_route_enables false

router router design scan_state_type 1

router router design min_wire_load_selection_type

0

router router design wire_load_selection_type 0

router router design hdl_library WORK

router router design hdl_template router

router router design hdl_canonical_default_params

DATA_WIDTH=32'h00000008,TS1=8'h01,TS2=8'h02,TS3=8'h03

router router design hdl_default_parameters TS1 => 8'h01, TS2 => 8'h02, TS3 => 8'h03, DATA_WIDTH => 8

router router design hdl_canonical_params

router router design hdl_parameters

router router design link_design_libraries WORK

router router design presto_gtech_count 12

router buff_out_reg[0] cell ff_edge_sense 1

router buff_out_reg[0] cell hdl_instance_name buff_out_reg[0]

router buff_out_reg[1] cell ff_edge_sense 1

router buff_out_reg[1] cell hdl_instance_name buff_out_reg[1]

router buff_out_reg[2] cell ff_edge_sense 1

router buff_out_reg[2] cell hdl_instance_name buff_out_reg[2]

router buff_out_reg[3] cell ff_edge_sense 1

router buff_out_reg[3] cell hdl_instance_name buff_out_reg[3]

router buff_out_reg[4] cell ff_edge_sense 1

router buff_out_reg[4] cell hdl_instance_name buff_out_reg[4]

router buff_out_reg[5] cell ff_edge_sense 1

router buff_out_reg[5] cell hdl_instance_name buff_out_reg[5]

router buff_out_reg[6] cell ff_edge_sense 1

router buff_out_reg[6] cell hdl_instance_name buff_out_reg[6]

router buff_out_reg[7] cell ff_edge_sense 1

router buff_out_reg[7] cell hdl_instance_name buff_out_reg[7]

router fifo1_inst cell hdl_instance_name fifo1_inst

router fifo1_inst cell array_ref 0

router fifo2_inst cell hdl_instance_name fifo2_inst

router fifo2_inst cell array_ref 0

router read_inst cell hdl_instance_name read_inst

router read_inst cell array_ref 0

router write_inst cell hdl_instance_name write_inst

router write_inst cell array_ref 0

router buff_out[0] net net_original_name buff_out[0]

router buff_out[0] net three_state true
router buff_out[1] net net_original_name buff_out[1]
router buff_out[1] net three_state true
router buff_out[2] net net_original_name buff_out[2]
router buff_out[2] net three_state true
router buff_out[3] net net_original_name buff_out[3]
router buff_out[3] net three_state true
router buff_out[4] net net_original_name buff_out[4]
router buff_out[4] net three_state true
router buff_out[5] net net_original_name buff_out[5]
router buff_out[5] net three_state true
router buff_out[6] net net_original_name buff_out[6]
router buff_out[6] net three_state true
router buff_out[7] net net_original_name buff_out[7]
router buff_out[7] net three_state true
router clk1 net net_original_name clk1
router clk1 net three_state true
router clk2 net net_original_name clk2
router clk2 net three_state true
router fifo1_datain[0] net net_original_name fifo1_datain[0]
router fifo1_datain[0] net three_state true
router fifo1_datain[1] net net_original_name fifo1_datain[1]
router fifo1_datain[1] net three_state true
router fifo1_datain[2] net net_original_name fifo1_datain[2]
router fifo1_datain[2] net three_state true
router fifo1_datain[3] net net_original_name fifo1_datain[3]
router fifo1_datain[3] net three_state true
router fifo1_datain[4] net net_original_name fifo1_datain[4]
router fifo1_datain[4] net three_state true
router fifo1_datain[5] net net_original_name fifo1_datain[5]

router	fifo1_datain[5]	net	three_state	true
router	fifo1_datain[6]	net	net_original_name	fifo1_datain[6]
router	fifo1_datain[6]	net	three_state	true
router	fifo1_datain[7]	net	net_original_name	fifo1_datain[7]
router	fifo1_datain[7]	net	three_state	true
router	fifo1_datain[8]	net	net_original_name	fifo1_datain[8]
router	fifo1_datain[8]	net	three_state	true
router	fifo1_datain[9]	net	net_original_name	fifo1_datain[9]
router	fifo1_datain[9]	net	three_state	true
router	fifo1_datain[10]	net	net_original_name	fifo1_datain[10]
router	fifo1_datain[10]	net	three_state	true
router	fifo1_datain[11]	net	net_original_name	fifo1_datain[11]
router	fifo1_datain[11]	net	three_state	true
router	fifo1_datain[12]	net	net_original_name	fifo1_datain[12]
router	fifo1_datain[12]	net	three_state	true
router	fifo1_datain[13]	net	net_original_name	fifo1_datain[13]
router	fifo1_datain[13]	net	three_state	true
router	fifo1_datain[14]	net	net_original_name	fifo1_datain[14]
router	fifo1_datain[14]	net	three_state	true
router	fifo1_datain[15]	net	net_original_name	fifo1_datain[15]
router	fifo1_datain[15]	net	three_state	true
router	fifo1_dataout[0]	net	net_original_name	fifo1_dataout[0]
router	fifo1_dataout[0]	net	three_state	true
router	fifo1_dataout[1]	net	net_original_name	fifo1_dataout[1]
router	fifo1_dataout[1]	net	three_state	true
router	fifo1_dataout[2]	net	net_original_name	fifo1_dataout[2]
router	fifo1_dataout[2]	net	three_state	true
router	fifo1_dataout[3]	net	net_original_name	fifo1_dataout[3]
router	fifo1_dataout[3]	net	three_state	true
router	fifo1_dataout[4]	net	net_original_name	fifo1_dataout[4]

router fifo1_dataout[4] net three_state true
router fifo1_dataout[5] net net_original_name fifo1_dataout[5]
router fifo1_dataout[5] net three_state true
router fifo1_dataout[6] net net_original_name fifo1_dataout[6]
router fifo1_dataout[6] net three_state true
router fifo1_dataout[7] net net_original_name fifo1_dataout[7]
router fifo1_dataout[7] net three_state true
router fifo1_dataout[8] net net_original_name fifo1_dataout[8]
router fifo1_dataout[8] net three_state true
router fifo1_dataout[9] net net_original_name fifo1_dataout[9]
router fifo1_dataout[9] net three_state true
router fifo1_dataout[10] net net_original_name fifo1_dataout[10]
router fifo1_dataout[10] net three_state true
router fifo1_dataout[11] net net_original_name fifo1_dataout[11]
router fifo1_dataout[11] net three_state true
router fifo1_dataout[12] net net_original_name fifo1_dataout[12]
router fifo1_dataout[12] net three_state true
router fifo1_dataout[13] net net_original_name fifo1_dataout[13]
router fifo1_dataout[13] net three_state true
router fifo1_dataout[14] net net_original_name fifo1_dataout[14]
router fifo1_dataout[14] net three_state true
router fifo1_dataout[15] net net_original_name fifo1_dataout[15]
router fifo1_dataout[15] net three_state true
router fifo1_empty net net_original_name fifo1_empty
router fifo1_empty net three_state true
router fifo1_full net net_original_name fifo1_full
router fifo1_full net three_state true
router fifo1_ren net net_original_name fifo1_ren
router fifo1_ren net three_state true
router fifo1_wen net net_original_name fifo1_wen

router fifo1_wen net three_state true
router fifo2_dataout[0] net net_original_name fifo2_dataout[0]
router fifo2_dataout[0] net three_state true
router fifo2_dataout[1] net net_original_name fifo2_dataout[1]
router fifo2_dataout[1] net three_state true
router fifo2_dataout[2] net net_original_name fifo2_dataout[2]
router fifo2_dataout[2] net three_state true
router fifo2_dataout[3] net net_original_name fifo2_dataout[3]
router fifo2_dataout[3] net three_state true
router fifo2_dataout[4] net net_original_name fifo2_dataout[4]
router fifo2_dataout[4] net three_state true
router fifo2_dataout[5] net net_original_name fifo2_dataout[5]
router fifo2_dataout[5] net three_state true
router fifo2_dataout[6] net net_original_name fifo2_dataout[6]
router fifo2_dataout[6] net three_state true
router fifo2_dataout[7] net net_original_name fifo2_dataout[7]
router fifo2_dataout[7] net three_state true
router fifo2_empty net net_original_name fifo2_empty
router fifo2_empty net three_state true
router fifo2_ren net net_original_name fifo2_ren
router fifo2_ren net three_state true
router fifo2_wen net net_original_name fifo2_wen
router fifo2_wen net three_state true
router packet_in[0] net net_original_name packet_in[0]
router packet_in[1] net net_original_name packet_in[1]
router packet_in[2] net net_original_name packet_in[2]
router packet_in[3] net net_original_name packet_in[3]
router packet_in[4] net net_original_name packet_in[4]
router packet_in[5] net net_original_name packet_in[5]
router packet_in[6] net net_original_name packet_in[6]

router	packet_in[7]	net	net_original_name	packet_in[7]
router	packet_out1[0]	net	net_original_name	packet_out1[0]
router	packet_out1[1]	net	net_original_name	packet_out1[1]
router	packet_out1[2]	net	net_original_name	packet_out1[2]
router	packet_out1[3]	net	net_original_name	packet_out1[3]
router	packet_out1[4]	net	net_original_name	packet_out1[4]
router	packet_out1[5]	net	net_original_name	packet_out1[5]
router	packet_out1[6]	net	net_original_name	packet_out1[6]
router	packet_out1[7]	net	net_original_name	packet_out1[7]
router	packet_out2[0]	net	net_original_name	packet_out2[0]
router	packet_out2[1]	net	net_original_name	packet_out2[1]
router	packet_out2[2]	net	net_original_name	packet_out2[2]
router	packet_out2[3]	net	net_original_name	packet_out2[3]
router	packet_out2[4]	net	net_original_name	packet_out2[4]
router	packet_out2[5]	net	net_original_name	packet_out2[5]
router	packet_out2[6]	net	net_original_name	packet_out2[6]
router	packet_out2[7]	net	net_original_name	packet_out2[7]
router	packet_out3[0]	net	net_original_name	packet_out3[0]
router	packet_out3[1]	net	net_original_name	packet_out3[1]
router	packet_out3[2]	net	net_original_name	packet_out3[2]
router	packet_out3[3]	net	net_original_name	packet_out3[3]
router	packet_out3[4]	net	net_original_name	packet_out3[4]
router	packet_out3[5]	net	net_original_name	packet_out3[5]
router	packet_out3[6]	net	net_original_name	packet_out3[6]
router	packet_out3[7]	net	net_original_name	packet_out3[7]
router	packet_valid_i	net	net_original_name	packet_valid_i
router	packet_valid_o1	net	net_original_name	packet_valid_o1
router	packet_valid_o2	net	net_original_name	packet_valid_o2
router	packet_valid_o3	net	net_original_name	packet_valid_o3
router	rst	net	net_original_name	rst

router rst net three_state true

router stop_packet_send net net_original_name stop_packet_send

router read_inst/clk net three_state true

router read_inst/fifo1_datain[2]
net three_state true

router read_inst/fifo1_datain[3]
net three_state true

router read_inst/fifo1_datain[4]
net three_state true

router read_inst/fifo1_datain[5]
net three_state true

router read_inst/fifo1_datain[6]
net three_state true

router read_inst/fifo1_datain[7]
net three_state true

router read_inst/fifo1_datain[8]
net three_state true

router read_inst/fifo1_datain[9]
net three_state true

router read_inst/fifo1_datain[10]
net three_state true

router read_inst/fifo1_datain[11]
net three_state true

router read_inst/fifo1_datain[12]
net three_state true

router read_inst/fifo1_datain[13]
net three_state true

router read_inst/fifo1_datain[14]
net three_state true

router read_inst/fifo1_datain[15]

net three_state true

router read_inst/fifo1_empty

net three_state true

router read_inst/fifo1_ren

net three_state true

router read_inst/packet_datain[0]

net three_state true

router read_inst/packet_datain[1]

net three_state true

router read_inst/packet_datain[2]

net three_state true

router read_inst/packet_datain[3]

net three_state true

router read_inst/packet_datain[4]

net three_state true

router read_inst/packet_datain[5]

net three_state true

router read_inst/packet_datain[6]

net three_state true

router read_inst/packet_datain[7]

net three_state true

router read_inst/packet_empty

net three_state true

router read_inst/packet_ren

net three_state true

router read_inst/rst net three_state true

router write_inst/N54 net three_state true

router write_inst/N55 net three_state true

router write_inst/add_97/carry[3]

net three_state true

router write_inst/buff_out[3]
net three_state true
router write_inst/buff_out[4]
net three_state true
router write_inst/buff_out[5]
net three_state true
router write_inst/buff_out[6]
net three_state true
router write_inst/buff_out[7]
net three_state true
router write_inst/clk net three_state true
router write_inst/fifo1_datain[0]
net three_state true
router write_inst/fifo1_datain[1]
net three_state true
router write_inst/fifo1_datain[2]
net three_state true
router write_inst/fifo1_datain[3]
net three_state true
router write_inst/fifo1_datain[4]
net three_state true
router write_inst/fifo1_datain[5]
net three_state true
router write_inst/fifo1_datain[6]
net three_state true
router write_inst/fifo1_datain[7]
net three_state true
router write_inst/fifo1_datain[8]
net three_state true
router write_inst/fifo1_datain[9]

net three_state true

router write_inst/fifo1_datain[10]

net three_state true

router write_inst/fifo1_datain[11]

net three_state true

router write_inst/fifo1_datain[12]

net three_state true

router write_inst/fifo1_datain[13]

net three_state true

router write_inst/fifo1_datain[14]

net three_state true

router write_inst/fifo1_datain[15]

net three_state true

router write_inst/fifo1_full

net three_state true

router write_inst/fifo1_wen

net three_state true

router write_inst/fifo2_wen

net three_state true

router write_inst/rst net three_state true

router buff_out_reg[2]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[1]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[3]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[4]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[5]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[0]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[6]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[7]/CP pin pin_on_clock_network_per_scn
true
router read_inst/clk pin pin_on_clock_network_per_scn
true
router write_inst/clk pin pin_on_clock_network_per_scn
true
router fifo2_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo2_inst/write_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/write_clk
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[0]/CP
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[1]/CP
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[2]/CP
pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[3]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[4]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[5]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[6]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/select_output_reg_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/select_output_reg_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router write_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router write_inst/cs_reg[1]/CP

pin pin_on_clock_network_per_scn

```
                                        true
router      write_inst/data_counter_reg[2]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      write_inst/data_counter_reg[1]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      write_inst/data_counter_reg[0]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      read_inst/clear_packet_count_reg
                cell    hdl_instance_name       clear_packet_count_reg
router      read_inst/cs_reg[0]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[0]
                cell    hdl_instance_name       cs_reg[0]
router      read_inst/cs_reg[1]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[1]
                cell    hdl_instance_name       cs_reg[1]
router      read_inst/cs_reg[2]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[2]
                cell    hdl_instance_name       cs_reg[2]
router      read_inst/fifo1_ren_reg
                cell    hdl_instance_name       fifo1_ren_reg
router      read_inst/load_packet_count_reg
                cell    hdl_instance_name       load_packet_count_reg
router      read_inst/packet_counter_reg[0]
                cell    ff_edge_sense           1
```

```
router      read_inst/packet_counter_reg[0]
                cell    hdl_instance_name       packet_counter_reg[0]
router      read_inst/packet_counter_reg[1]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[1]
                cell    hdl_instance_name       packet_counter_reg[1]
router      read_inst/packet_counter_reg[2]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[2]
                cell    hdl_instance_name       packet_counter_reg[2]
router      read_inst/packet_counter_reg[3]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[3]
                cell    hdl_instance_name       packet_counter_reg[3]
router      read_inst/packet_counter_reg[4]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[4]
                cell    hdl_instance_name       packet_counter_reg[4]
router      read_inst/packet_counter_reg[5]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[5]
                cell    hdl_instance_name       packet_counter_reg[5]
router      read_inst/packet_counter_reg[6]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[6]
                cell    hdl_instance_name       packet_counter_reg[6]
router      read_inst/packet_counter_reg[7]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[7]
                cell    hdl_instance_name       packet_counter_reg[7]
```

```
router      read_inst/packet_dec_en_reg
                cell    hdl_instance_name       packet_dec_en_reg
router      read_inst/packet_ren_reg
                cell    hdl_instance_name       packet_ren_reg
router      read_inst/packet_valid_reg
                cell    hdl_instance_name       packet_valid_reg
router      read_inst/select_output_reg[0]
                cell    hdl_instance_name       select_output_reg[0]
router      read_inst/select_output_reg[1]
                cell    hdl_instance_name       select_output_reg[1]
router      read_inst/select_output_reg_reg[0]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[0]
                cell    hdl_instance_name       select_output_reg_reg[0]
router      read_inst/select_output_reg_reg[1]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[1]
                cell    hdl_instance_name       select_output_reg_reg[1]
router      read_inst/temp_packet_data_reg[0]
                cell    hdl_instance_name       temp_packet_data_reg[0]
router      read_inst/temp_packet_data_reg[1]
                cell    hdl_instance_name       temp_packet_data_reg[1]
router      read_inst/temp_packet_data_reg[2]
                cell    hdl_instance_name       temp_packet_data_reg[2]
router      read_inst/temp_packet_data_reg[3]
                cell    hdl_instance_name       temp_packet_data_reg[3]
router      read_inst/temp_packet_data_reg[4]
                cell    hdl_instance_name       temp_packet_data_reg[4]
router      read_inst/temp_packet_data_reg[5]
                cell    hdl_instance_name       temp_packet_data_reg[5]
```

router read_inst/temp_packet_data_reg[6]
cell hdl_instance_name temp_packet_data_reg[6]
router read_inst/temp_packet_data_reg[7]
cell hdl_instance_name temp_packet_data_reg[7]
router write_inst/clear_data_count_reg
cell hdl_instance_name clear_data_count_reg
router write_inst/cs_reg[0]
cell ff_edge_sense 1
router write_inst/cs_reg[0]
cell hdl_instance_name cs_reg[0]
router write_inst/cs_reg[1]
cell ff_edge_sense 1
router write_inst/cs_reg[1]
cell hdl_instance_name cs_reg[1]
router write_inst/cs_reg[2]
cell ff_edge_sense 1
router write_inst/cs_reg[2]
cell hdl_instance_name cs_reg[2]
router write_inst/data_counter_reg[0]
cell ff_edge_sense 1
router write_inst/data_counter_reg[0]
cell hdl_instance_name data_counter_reg[0]
router write_inst/data_counter_reg[1]
cell ff_edge_sense 1
router write_inst/data_counter_reg[1]
cell hdl_instance_name data_counter_reg[1]
router write_inst/data_counter_reg[2]
cell ff_edge_sense 1
router write_inst/data_counter_reg[2]
cell hdl_instance_name data_counter_reg[2]

router write_inst/fifo1_datain_reg[0]

cell hdl_instance_name fifo1_datain_reg[0]

router write_inst/fifo1_datain_reg[1]

cell hdl_instance_name fifo1_datain_reg[1]

router write_inst/fifo1_datain_reg[2]

cell hdl_instance_name fifo1_datain_reg[2]

router write_inst/fifo1_datain_reg[3]

cell hdl_instance_name fifo1_datain_reg[3]

router write_inst/fifo1_datain_reg[4]

cell hdl_instance_name fifo1_datain_reg[4]

router write_inst/fifo1_datain_reg[5]

cell hdl_instance_name fifo1_datain_reg[5]

router write_inst/fifo1_datain_reg[6]

cell hdl_instance_name fifo1_datain_reg[6]

router write_inst/fifo1_datain_reg[7]

cell hdl_instance_name fifo1_datain_reg[7]

router write_inst/fifo1_datain_reg[8]

cell hdl_instance_name fifo1_datain_reg[8]

router write_inst/fifo1_datain_reg[9]

cell hdl_instance_name fifo1_datain_reg[9]

router write_inst/fifo1_datain_reg[10]

cell hdl_instance_name fifo1_datain_reg[10]

router write_inst/fifo1_datain_reg[11]

cell hdl_instance_name fifo1_datain_reg[11]

router write_inst/fifo1_datain_reg[12]

cell hdl_instance_name fifo1_datain_reg[12]

router write_inst/fifo1_datain_reg[13]

cell hdl_instance_name fifo1_datain_reg[13]

router write_inst/fifo1_datain_reg[14]

cell hdl_instance_name fifo1_datain_reg[14]

router write_inst/fifo1_datain_reg[15]
cell hdl_instance_name fifo1_datain_reg[15]
router write_inst/fifo1_valid_reg
cell hdl_instance_name fifo1_valid_reg
router write_inst/fifo1_wen_reg
cell hdl_instance_name fifo1_wen_reg
router write_inst/fifo2_wen_reg
cell hdl_instance_name fifo2_wen_reg
router write_inst/load_data_count_reg
cell hdl_instance_name load_data_count_reg
router write_inst/stop_packet_reg
cell hdl_instance_name stop_packet_reg
router write_inst/temp_fifo1_reg[0]
cell hdl_instance_name temp_fifo1_reg[0]
router write_inst/temp_fifo1_reg[1]
cell hdl_instance_name temp_fifo1_reg[1]
router write_inst/temp_fifo1_reg[2]
cell hdl_instance_name temp_fifo1_reg[2]
router write_inst/temp_fifo1_reg[3]
cell hdl_instance_name temp_fifo1_reg[3]
router write_inst/temp_fifo1_reg[4]
cell hdl_instance_name temp_fifo1_reg[4]
router write_inst/temp_fifo1_reg[5]
cell hdl_instance_name temp_fifo1_reg[5]
router write_inst/temp_fifo1_reg[6]
cell hdl_instance_name temp_fifo1_reg[6]
router write_inst/temp_fifo1_reg[7]
cell hdl_instance_name temp_fifo1_reg[7]
router read_inst/N30 net net_original_name SUM(1)
router read_inst/N32 net net_original_name SUM(3)

router read_inst/N34 net net_original_name SUM(5)

router read_inst/N35 net net_original_name SUM(6)

router read_inst/N36 net net_original_name SUM(7)

router read_inst/clk net net_original_name clk

router read_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router read_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router read_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router read_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router read_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router read_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router read_inst/fifo1_datain[8]

net net_original_name fifo1_datain[8]

router read_inst/fifo1_datain[9]

net net_original_name fifo1_datain[9]

router read_inst/fifo1_datain[10]

net net_original_name fifo1_datain[10]

router read_inst/fifo1_datain[11]

net net_original_name fifo1_datain[11]

router read_inst/fifo1_datain[12]

net net_original_name fifo1_datain[12]

router read_inst/fifo1_datain[13]

net net_original_name fifo1_datain[13]

router read_inst/fifo1_datain[14]

net net_original_name fifo1_datain[14]

router read_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router read_inst/fifo1_empty
net net_original_name fifo1_empty
router read_inst/fifo1_ren
net net_original_name fifo1_ren
router read_inst/ns[0] net net_original_name ns[0]
router read_inst/ns[1] net net_original_name ns[1]
router read_inst/ns[2] net net_original_name ns[2]
router read_inst/packet_counter[0]
net net_original_name packet_counter[0]
router read_inst/packet_counter[1]
net net_original_name packet_counter[1]
router read_inst/packet_counter[2]
net net_original_name packet_counter[2]
router read_inst/packet_counter[3]
net net_original_name packet_counter[3]
router read_inst/packet_counter[4]
net net_original_name packet_counter[4]
router read_inst/packet_counter[6]
net net_original_name packet_counter[6]
router read_inst/packet_counter[7]
net net_original_name packet_counter[7]
router read_inst/packet_datain[0]
net net_original_name packet_datain[0]
router read_inst/packet_datain[1]
net net_original_name packet_datain[1]
router read_inst/packet_datain[2]
net net_original_name packet_datain[2]
router read_inst/packet_datain[3]

net net_original_name packet_datain[3]

router read_inst/packet_datain[4]

net net_original_name packet_datain[4]

router read_inst/packet_datain[5]

net net_original_name packet_datain[5]

router read_inst/packet_datain[6]

net net_original_name packet_datain[6]

router read_inst/packet_datain[7]

net net_original_name packet_datain[7]

router read_inst/packet_empty

net net_original_name packet_empty

router read_inst/packet_output_1[0]

net net_original_name packet_output_1[0]

router read_inst/packet_output_1[1]

net net_original_name packet_output_1[1]

router read_inst/packet_output_1[2]

net net_original_name packet_output_1[2]

router read_inst/packet_output_1[3]

net net_original_name packet_output_1[3]

router read_inst/packet_output_1[4]

net net_original_name packet_output_1[4]

router read_inst/packet_output_1[5]

net net_original_name packet_output_1[5]

router read_inst/packet_output_1[6]

net net_original_name packet_output_1[6]

router read_inst/packet_output_1[7]

net net_original_name packet_output_1[7]

router read_inst/packet_output_2[0]

net net_original_name packet_output_2[0]

router read_inst/packet_output_2[1]

net net_original_name packet_output_2[1]
router read_inst/packet_output_2[2]
net net_original_name packet_output_2[2]
router read_inst/packet_output_2[3]
net net_original_name packet_output_2[3]
router read_inst/packet_output_2[4]
net net_original_name packet_output_2[4]
router read_inst/packet_output_2[5]
net net_original_name packet_output_2[5]
router read_inst/packet_output_2[6]
net net_original_name packet_output_2[6]
router read_inst/packet_output_2[7]
net net_original_name packet_output_2[7]
router read_inst/packet_output_3[0]
net net_original_name packet_output_3[0]
router read_inst/packet_output_3[1]
net net_original_name packet_output_3[1]
router read_inst/packet_output_3[2]
net net_original_name packet_output_3[2]
router read_inst/packet_output_3[3]
net net_original_name packet_output_3[3]
router read_inst/packet_output_3[4]
net net_original_name packet_output_3[4]
router read_inst/packet_output_3[5]
net net_original_name packet_output_3[5]
router read_inst/packet_output_3[6]
net net_original_name packet_output_3[6]
router read_inst/packet_output_3[7]
net net_original_name packet_output_3[7]
router read_inst/packet_ren

net net_original_name packet_ren

router read_inst/packet_valid_o1

net net_original_name packet_valid_o1

router read_inst/packet_valid_o2

net net_original_name packet_valid_o2

router read_inst/packet_valid_o3

net net_original_name packet_valid_o3

router read_inst/rst net net_original_name rst

router read_inst/select_output[0]

net net_original_name select_output[0]

router read_inst/select_output[1]

net net_original_name select_output[1]

router read_inst/select_output_reg[0]

net net_original_name select_output_reg[0]

router read_inst/select_output_reg[1]

net net_original_name select_output_reg[1]

router write_inst/N54 net net_original_name SUM(0)

router write_inst/N55 net net_original_name SUM(1)

router write_inst/N57 net net_original_name SUM(3)

router write_inst/N58 net net_original_name SUM(4)

router write_inst/N59 net net_original_name SUM(5)

router write_inst/N60 net net_original_name SUM(6)

router write_inst/N61 net net_original_name SUM(7)

router write_inst/add_97/carry[3]

net net_original_name carry(3)

router write_inst/add_97/carry[4]

net net_original_name carry(4)

router write_inst/add_97/carry[5]

net net_original_name carry(5)

router write_inst/add_97/carry[6]

net net_original_name carry(6)

router write_inst/add_97/carry[7]

net net_original_name carry(7)

router write_inst/buff_out[3]

net net_original_name buff_out[3]

router write_inst/buff_out[4]

net net_original_name buff_out[4]

router write_inst/buff_out[5]

net net_original_name buff_out[5]

router write_inst/buff_out[6]

net net_original_name buff_out[6]

router write_inst/buff_out[7]

net net_original_name buff_out[7]

router write_inst/clk net net_original_name clk

router write_inst/fifo1_datain[0]

net net_original_name fifo1_datain[0]

router write_inst/fifo1_datain[1]

net net_original_name fifo1_datain[1]

router write_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router write_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router write_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router write_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router write_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router write_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router write_inst/fifo1_datain[8]
net net_original_name fifo1_datain[8]
router write_inst/fifo1_datain[9]
net net_original_name fifo1_datain[9]
router write_inst/fifo1_datain[10]
net net_original_name fifo1_datain[10]
router write_inst/fifo1_datain[11]
net net_original_name fifo1_datain[11]
router write_inst/fifo1_datain[12]
net net_original_name fifo1_datain[12]
router write_inst/fifo1_datain[13]
net net_original_name fifo1_datain[13]
router write_inst/fifo1_datain[14]
net net_original_name fifo1_datain[14]
router write_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router write_inst/fifo1_full
net net_original_name fifo1_full
router write_inst/fifo1_wen
net net_original_name fifo1_wen
router write_inst/fifo2_wen
net net_original_name fifo2_wen
router write_inst/ns[0] net net_original_name ns[0]
router write_inst/ns[1] net net_original_name ns[1]
router write_inst/ns[2] net net_original_name ns[2]
router write_inst/packet_valid
net net_original_name packet_valid
router write_inst/rst net net_original_name rst
router write_inst/stop_packet
net net_original_name stop_packet

```
router    clk1          port    pin_on_clock_network_per_scn
                                        true
router    clk1          port    hdl_instance_name       clk1
router    clk2          port    pin_on_clock_network_per_scn
                                        true
router    clk2          port    hdl_instance_name       clk2
router    packet_in[0]      port    hdl_instance_name       packet_in[0]
router    packet_in[1]      port    hdl_instance_name       packet_in[1]
router    packet_in[2]      port    hdl_instance_name       packet_in[2]
router    packet_in[3]      port    hdl_instance_name       packet_in[3]
router    packet_in[4]      port    hdl_instance_name       packet_in[4]
router    packet_in[5]      port    hdl_instance_name       packet_in[5]
router    packet_in[6]      port    hdl_instance_name       packet_in[6]
router    packet_in[7]      port    hdl_instance_name       packet_in[7]
router    packet_out1[0]    port    hdl_instance_name       packet_out1[0]
router    packet_out1[1]    port    hdl_instance_name       packet_out1[1]
router    packet_out1[2]    port    hdl_instance_name       packet_out1[2]
router    packet_out1[3]    port    hdl_instance_name       packet_out1[3]
router    packet_out1[4]    port    hdl_instance_name       packet_out1[4]
router    packet_out1[5]    port    hdl_instance_name       packet_out1[5]
router    packet_out1[6]    port    hdl_instance_name       packet_out1[6]
router    packet_out1[7]    port    hdl_instance_name       packet_out1[7]
router    packet_out2[0]    port    hdl_instance_name       packet_out2[0]
router    packet_out2[1]    port    hdl_instance_name       packet_out2[1]
router    packet_out2[2]    port    hdl_instance_name       packet_out2[2]
router    packet_out2[3]    port    hdl_instance_name       packet_out2[3]
router    packet_out2[4]    port    hdl_instance_name       packet_out2[4]
router    packet_out2[5]    port    hdl_instance_name       packet_out2[5]
router    packet_out2[6]    port    hdl_instance_name       packet_out2[6]
router    packet_out2[7]    port    hdl_instance_name       packet_out2[7]
```

router packet_out3[0] port hdl_instance_name packet_out3[0]

router packet_out3[1] port hdl_instance_name packet_out3[1]

router packet_out3[2] port hdl_instance_name packet_out3[2]

router packet_out3[3] port hdl_instance_name packet_out3[3]

router packet_out3[4] port hdl_instance_name packet_out3[4]

router packet_out3[5] port hdl_instance_name packet_out3[5]

router packet_out3[6] port hdl_instance_name packet_out3[6]

router packet_out3[7] port hdl_instance_name packet_out3[7]

router packet_valid_i port hdl_instance_name packet_valid_i

router packet_valid_o1 port hdl_instance_name packet_valid_o1

router packet_valid_o2 port hdl_instance_name packet_valid_o2

router packet_valid_o3 port hdl_instance_name packet_valid_o3

router rst port hdl_instance_name rst

router stop_packet_send port hdl_instance_name stop_packet_send

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000010,DEPTH=32'h00000002

router fifo reference hdl_parameters DATA_WIDTH=16,DEPTH=2

router fifo reference hdl_template fifo

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000008,DEPTH=32'h00000040

router fifo reference hdl_parameters DATA_WIDTH=8,DEPTH=64

router fifo reference hdl_template fifo

Synthesis (with Low Map Effort):

Synthesis Script/Log

```
#Read the design in
read_file -format verilog {"fifo.v"}
read_file -format verilog {"write.v"}
read_file -format verilog {"read.v"}
read_file -format verilog {"router.v"}
#set the current design
set current_design router
#link the design to the libraries
link
#create clock
create_clock "clk1" -period 4 -name "clk1"
set_dont_touch_network "clk1"
create_clock "clk2" -period 10 -name "clk2"
set_dont_touch_network "clk2"
#false path
set_false_path -from clk1 -to clk2
#specify max/min delays for input/output ports
set_input_delay -clock clk1 -max -rise 2 "packet_valid_i"
set_input_delay -clock clk1 -min -rise 1 "packet_valid_i"
set_input_delay -clock clk1 -max -rise 2 "packet_in"
set_input_delay -clock clk1 -min -rise 1 "packet_in"
set_input_delay -clock clk1 -max -rise 2 "rst"
set_input_delay -clock clk1 -min -rise 1 "rst"
set_input_delay -clock clk1 -max -rise 2 "clk1"
set_input_delay -clock clk1 -min -rise 1 "clk1"
set_input_delay -clock clk2 -max -rise 2 "clk2"
set_input_delay -clock clk2 -min -rise 1 "clk2"
set_output_delay -clock clk1 -max -rise 2 "stop_packet_send"
```

```
set_output_delay -clock clk1 -min -rise 1 "stop_packet_send"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o1"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o1"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o2"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o2"
set_output_delay -clock clk2 -max -rise 2 "packet_valid_o3"
set_output_delay -clock clk2 -min -rise 1 "packet_valid_o3"
set_output_delay -clock clk2 -max -rise 2 "packet_out1"
set_output_delay -clock clk2 -min -rise 1 "packet_out1"
set_output_delay -clock clk2 -max -rise 2 "packet_out2"
set_output_delay -clock clk2 -min -rise 1 "packet_out2"
set_output_delay -clock clk2 -max -rise 2 "packet_out3"
set_output_delay -clock clk2 -min -rise 1 "packet_out3"
#set area constraint to 0 for optimum area
set_max_area 0
#set operating conditions
set_operating_conditions -library "lsi_10k" "BCCOM"
#synthesize
compile -map_effort low -boundary_optimization
#generate reports
report_attribute > report_attribute.txt
report_area > report_area.txt
report_constraints -all_violators > report_constraints.txt
#report_timing -path full -delay max -max_paths 1 -nworst 1 > report_timing.txt
report_timing > report_timing.txt
```

Area Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : area

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:14:10 2022

****

Information: Updating design information... (UID-85)

Library(s) Used:

lsi_10k (File: /opt/synopsys/syn/S-2021.06-SP1/libraries/syn/lsi_10k.db)

Number of ports: 152

Number of nets: 449

Number of cells: 313

Number of combinational cells: 232

Number of sequential cells: 75

Number of macros/black boxes: 0

Number of buf/inv: 43

Number of references: 7

Combinational area: 340.000000

Buf/Inv area: 43.000000

Noncombinational area: 473.000000

Macro/Black Box area: 0.000000

Net Interconnect area: undefined (No wire load specified)

Total cell area: 813.000000

Total area: undefined

Information: This design contains black box (unknown) components. (RPT-8)

Timing Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : timing

-path full

-delay max

-max_paths 1

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:14:10 2022

****

Operating Conditions: BCCOM Library: lsi_10k

Wire Load Model Mode: top

Startpoint: packet_valid_i

(input port clocked by clk1)

Endpoint: write_inst/cs_reg[0]

(rising edge-triggered flip-flop clocked by clk1)

Path Group: clk1

Path Type: max

Point	Incr	Path
clock clk1 (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	2.00	2.00 r
packet_valid_i (in)	0.00	2.00 r
write_inst/packet_valid (write)	0.00	2.00 r

write_inst/U3/Z (AN2P) 0.42 2.42 r

write_inst/U20/Z (MUX21L) 0.42 2.84 r

write_inst/U12/Z (ND4) 0.30 3.14 f

write_inst/cs_reg[0]/D (FD2) 0.00 3.14 f

data arrival time 3.14

clock clk1 (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

write_inst/cs_reg[0]/CP (FD2) 0.00 4.00 r

library setup time -0.85 3.15

data required time 3.15

---

data required time 3.15

data arrival time -3.14

---

slack (MET) 0.01

Startpoint: read_inst/packet_counter_reg[5]

(rising edge-triggered flip-flop clocked by clk2)

Endpoint: read_inst/packet_counter_reg[0]

(rising edge-triggered flip-flop clocked by clk2)

Path Group: clk2

Path Type: max

Point Incr Path

---

clock clk2 (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

read_inst/packet_counter_reg[5]/CP (FD2) 0.00 0.00 r

read_inst/packet_counter_reg[5]/QN (FD2)	0.96	0.96 f
read_inst/U110/Z (ND4)	0.47	1.43 r
read_inst/U85/Z (NR4)	0.19	1.62 f
read_inst/U84/Z (ND2)	0.39	2.01 r
read_inst/U82/Z (ND2)	0.11	2.12 f
read_inst/U3/Z (AO3)	1.46	3.58 r
read_inst/U81/Z (AN3)	0.95	4.53 r
read_inst/U62/Z (ND2)	0.11	4.64 f
read_inst/U60/Z (AO3)	0.40	5.04 r
read_inst/packet_counter_reg[0]/D (FD2)	0.00	5.04 r
data arrival time	5.04	

clock clk2 (rise edge)	10.00	10.00
clock network delay (ideal)	0.00	10.00
read_inst/packet_counter_reg[0]/CP (FD2)	0.00	10.00 r
library setup time	-0.85	9.15
data required time		9.15

---

data required time	9.15
data arrival time	-5.04

---

slack (MET)	4.11

Constraints Report:

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : constraint

-all_violators

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:14:10 2022

****

max_area

Design	Required Area	Actual Area	Slack	
router	0.00	813.00	-813.00	(VIOLATED)

1

Attribute Report:

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=16,DEPTH=2". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Information: Building the design 'fifo' instantiated from design 'router' with
the parameters "DATA_WIDTH=8,DEPTH=64". (HDL-193)

Warning: Cannot find the design 'fifo' in the library 'WORK'. (LBR-1)

Warning: Unable to resolve reference 'fifo' in 'router'. (LINK-5)

Warning: Design 'router' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)

****

Report : Attribute

Design : router

Version: S-2021.06-SP1

Date : Mon May 2 01:14:09 2022

****

Design	Object	Type	Attribute Name	Value
router	router	design	design_voltage_unit	1000.000000
router	router	design	design_current_unit	0.001000
router	router	design	design_resistance_unit	10000.000000
router	router	design	design_cap_unit	0.000100
router	router	design	design_time_unit	1.000000
router	router	design	compile_cpu_hostname	ecs-pa-coding1.ecs.csus.edu
router	router	design	ice_canonical_xor2_delay	0.537872
router	router	design	ice_canonical_nand2_delay	0.219973
router	router	design	testdb_meth_sig_usage_option	98307
router	router	design	testdb_meth_sig_usage	106499

router router design testdb_meth_name multiplexed_flip_flop
router router design map_effort_option 2
router router design map true
router router design exact_sequential_map false
router router design pads_thru_hier false
router router design pads_respect_hier false
router router design redundancy_removal true
router router design instance_name_suffix
router router design multibit_mode non_timing_driven
router router design compile_tdrs_cpu_time 0.350403
router router design compile_lib_cpu_time 0.168066
router router design compile_tot_cpu_time 1.280758
router router design compile_rbo_cpu_time 0.133802
router router design compile_abo_cpu_time 0.551743
router router design compile_tot_wall_time 1.526834
router router design temperature_from_min_lib 0.000000
router router design temperature_from_max_lib 0.000000
router router design max_area 0.000000
router router design ungroup_all_option false
router router design scan_state_route_serial false
router router design scan_state_route_clocks false
router router design scan_state_route_enables false
router router design scan_state_type 1
router router design min_wire_load_selection_type
0
router router design wire_load_selection_type 0
router router design hdl_library WORK
router router design hdl_template router
router router design hdl_canonical_default_params

DATA_WIDTH=32'h00000008,TS1=8'h01,TS2=8'h02,TS3=8'h03

router router design hdl_default_parameters TS1 => 8'h01, TS2 => 8'h02, TS3 => 8'h03, DATA_WIDTH => 8

router router design hdl_canonical_params

router router design hdl_parameters

router router design link_design_libraries WORK

router router design presto_gtech_count 12

router buff_out_reg[0] cell ff_edge_sense 1

router buff_out_reg[0] cell hdl_instance_name buff_out_reg[0]

router buff_out_reg[1] cell ff_edge_sense 1

router buff_out_reg[1] cell hdl_instance_name buff_out_reg[1]

router buff_out_reg[2] cell ff_edge_sense 1

router buff_out_reg[2] cell hdl_instance_name buff_out_reg[2]

router buff_out_reg[3] cell ff_edge_sense 1

router buff_out_reg[3] cell hdl_instance_name buff_out_reg[3]

router buff_out_reg[4] cell ff_edge_sense 1

router buff_out_reg[4] cell hdl_instance_name buff_out_reg[4]

router buff_out_reg[5] cell ff_edge_sense 1

router buff_out_reg[5] cell hdl_instance_name buff_out_reg[5]

router buff_out_reg[6] cell ff_edge_sense 1

router buff_out_reg[6] cell hdl_instance_name buff_out_reg[6]

router buff_out_reg[7] cell ff_edge_sense 1

router buff_out_reg[7] cell hdl_instance_name buff_out_reg[7]

router fifo1_inst cell hdl_instance_name fifo1_inst

router fifo1_inst cell array_ref 0

router fifo2_inst cell hdl_instance_name fifo2_inst

router fifo2_inst cell array_ref 0

router read_inst cell hdl_instance_name read_inst

router read_inst cell array_ref 0

router write_inst cell hdl_instance_name write_inst

router write_inst cell array_ref 0

router buff_out[0] net net_original_name buff_out[0]

router buff_out[0] net three_state true
router buff_out[1] net net_original_name buff_out[1]
router buff_out[1] net three_state true
router buff_out[2] net net_original_name buff_out[2]
router buff_out[2] net three_state true
router buff_out[3] net net_original_name buff_out[3]
router buff_out[3] net three_state true
router buff_out[4] net net_original_name buff_out[4]
router buff_out[4] net three_state true
router buff_out[5] net net_original_name buff_out[5]
router buff_out[5] net three_state true
router buff_out[6] net net_original_name buff_out[6]
router buff_out[6] net three_state true
router buff_out[7] net net_original_name buff_out[7]
router buff_out[7] net three_state true
router clk1 net net_original_name clk1
router clk1 net three_state true
router clk2 net net_original_name clk2
router clk2 net three_state true
router fifo1_datain[0] net net_original_name fifo1_datain[0]
router fifo1_datain[0] net three_state true
router fifo1_datain[1] net net_original_name fifo1_datain[1]
router fifo1_datain[1] net three_state true
router fifo1_datain[2] net net_original_name fifo1_datain[2]
router fifo1_datain[2] net three_state true
router fifo1_datain[3] net net_original_name fifo1_datain[3]
router fifo1_datain[3] net three_state true
router fifo1_datain[4] net net_original_name fifo1_datain[4]
router fifo1_datain[4] net three_state true
router fifo1_datain[5] net net_original_name fifo1_datain[5]

router	fifo1_datain[5]	net	three_state	true
router	fifo1_datain[6]	net	net_original_name	fifo1_datain[6]
router	fifo1_datain[6]	net	three_state	true
router	fifo1_datain[7]	net	net_original_name	fifo1_datain[7]
router	fifo1_datain[7]	net	three_state	true
router	fifo1_datain[8]	net	net_original_name	fifo1_datain[8]
router	fifo1_datain[8]	net	three_state	true
router	fifo1_datain[9]	net	net_original_name	fifo1_datain[9]
router	fifo1_datain[9]	net	three_state	true
router	fifo1_datain[10]	net	net_original_name	fifo1_datain[10]
router	fifo1_datain[10]	net	three_state	true
router	fifo1_datain[11]	net	net_original_name	fifo1_datain[11]
router	fifo1_datain[11]	net	three_state	true
router	fifo1_datain[12]	net	net_original_name	fifo1_datain[12]
router	fifo1_datain[12]	net	three_state	true
router	fifo1_datain[13]	net	net_original_name	fifo1_datain[13]
router	fifo1_datain[13]	net	three_state	true
router	fifo1_datain[14]	net	net_original_name	fifo1_datain[14]
router	fifo1_datain[14]	net	three_state	true
router	fifo1_datain[15]	net	net_original_name	fifo1_datain[15]
router	fifo1_datain[15]	net	three_state	true
router	fifo1_dataout[0]	net	net_original_name	fifo1_dataout[0]
router	fifo1_dataout[0]	net	three_state	true
router	fifo1_dataout[1]	net	net_original_name	fifo1_dataout[1]
router	fifo1_dataout[1]	net	three_state	true
router	fifo1_dataout[2]	net	net_original_name	fifo1_dataout[2]
router	fifo1_dataout[2]	net	three_state	true
router	fifo1_dataout[3]	net	net_original_name	fifo1_dataout[3]
router	fifo1_dataout[3]	net	three_state	true
router	fifo1_dataout[4]	net	net_original_name	fifo1_dataout[4]

router fifo1_dataout[4] net three_state true
router fifo1_dataout[5] net net_original_name fifo1_dataout[5]
router fifo1_dataout[5] net three_state true
router fifo1_dataout[6] net net_original_name fifo1_dataout[6]
router fifo1_dataout[6] net three_state true
router fifo1_dataout[7] net net_original_name fifo1_dataout[7]
router fifo1_dataout[7] net three_state true
router fifo1_dataout[8] net net_original_name fifo1_dataout[8]
router fifo1_dataout[8] net three_state true
router fifo1_dataout[9] net net_original_name fifo1_dataout[9]
router fifo1_dataout[9] net three_state true
router fifo1_dataout[10] net net_original_name fifo1_dataout[10]
router fifo1_dataout[10] net three_state true
router fifo1_dataout[11] net net_original_name fifo1_dataout[11]
router fifo1_dataout[11] net three_state true
router fifo1_dataout[12] net net_original_name fifo1_dataout[12]
router fifo1_dataout[12] net three_state true
router fifo1_dataout[13] net net_original_name fifo1_dataout[13]
router fifo1_dataout[13] net three_state true
router fifo1_dataout[14] net net_original_name fifo1_dataout[14]
router fifo1_dataout[14] net three_state true
router fifo1_dataout[15] net net_original_name fifo1_dataout[15]
router fifo1_dataout[15] net three_state true
router fifo1_empty net net_original_name fifo1_empty
router fifo1_empty net three_state true
router fifo1_full net net_original_name fifo1_full
router fifo1_full net three_state true
router fifo1_ren net net_original_name fifo1_ren
router fifo1_ren net three_state true
router fifo1_wen net net_original_name fifo1_wen

router fifo1_wen net three_state true
router fifo2_dataout[0] net net_original_name fifo2_dataout[0]
router fifo2_dataout[0] net three_state true
router fifo2_dataout[1] net net_original_name fifo2_dataout[1]
router fifo2_dataout[1] net three_state true
router fifo2_dataout[2] net net_original_name fifo2_dataout[2]
router fifo2_dataout[2] net three_state true
router fifo2_dataout[3] net net_original_name fifo2_dataout[3]
router fifo2_dataout[3] net three_state true
router fifo2_dataout[4] net net_original_name fifo2_dataout[4]
router fifo2_dataout[4] net three_state true
router fifo2_dataout[5] net net_original_name fifo2_dataout[5]
router fifo2_dataout[5] net three_state true
router fifo2_dataout[6] net net_original_name fifo2_dataout[6]
router fifo2_dataout[6] net three_state true
router fifo2_dataout[7] net net_original_name fifo2_dataout[7]
router fifo2_dataout[7] net three_state true
router fifo2_empty net net_original_name fifo2_empty
router fifo2_empty net three_state true
router fifo2_ren net net_original_name fifo2_ren
router fifo2_ren net three_state true
router fifo2_wen net net_original_name fifo2_wen
router fifo2_wen net three_state true
router packet_in[0] net net_original_name packet_in[0]
router packet_in[1] net net_original_name packet_in[1]
router packet_in[2] net net_original_name packet_in[2]
router packet_in[3] net net_original_name packet_in[3]
router packet_in[4] net net_original_name packet_in[4]
router packet_in[5] net net_original_name packet_in[5]
router packet_in[6] net net_original_name packet_in[6]

router	packet_in[7]	net	net_original_name	packet_in[7]
router	packet_out1[0]	net	net_original_name	packet_out1[0]
router	packet_out1[1]	net	net_original_name	packet_out1[1]
router	packet_out1[2]	net	net_original_name	packet_out1[2]
router	packet_out1[3]	net	net_original_name	packet_out1[3]
router	packet_out1[4]	net	net_original_name	packet_out1[4]
router	packet_out1[5]	net	net_original_name	packet_out1[5]
router	packet_out1[6]	net	net_original_name	packet_out1[6]
router	packet_out1[7]	net	net_original_name	packet_out1[7]
router	packet_out2[0]	net	net_original_name	packet_out2[0]
router	packet_out2[1]	net	net_original_name	packet_out2[1]
router	packet_out2[2]	net	net_original_name	packet_out2[2]
router	packet_out2[3]	net	net_original_name	packet_out2[3]
router	packet_out2[4]	net	net_original_name	packet_out2[4]
router	packet_out2[5]	net	net_original_name	packet_out2[5]
router	packet_out2[6]	net	net_original_name	packet_out2[6]
router	packet_out2[7]	net	net_original_name	packet_out2[7]
router	packet_out3[0]	net	net_original_name	packet_out3[0]
router	packet_out3[1]	net	net_original_name	packet_out3[1]
router	packet_out3[2]	net	net_original_name	packet_out3[2]
router	packet_out3[3]	net	net_original_name	packet_out3[3]
router	packet_out3[4]	net	net_original_name	packet_out3[4]
router	packet_out3[5]	net	net_original_name	packet_out3[5]
router	packet_out3[6]	net	net_original_name	packet_out3[6]
router	packet_out3[7]	net	net_original_name	packet_out3[7]
router	packet_valid_i	net	net_original_name	packet_valid_i
router	packet_valid_o1	net	net_original_name	packet_valid_o1
router	packet_valid_o2	net	net_original_name	packet_valid_o2
router	packet_valid_o3	net	net_original_name	packet_valid_o3
router	rst	net	net_original_name	rst

router rst net three_state true

router stop_packet_send net net_original_name stop_packet_send

router read_inst/clk net three_state true

router read_inst/fifo1_datain[2]

net three_state true

router read_inst/fifo1_datain[3]

net three_state true

router read_inst/fifo1_datain[4]

net three_state true

router read_inst/fifo1_datain[5]

net three_state true

router read_inst/fifo1_datain[6]

net three_state true

router read_inst/fifo1_datain[7]

net three_state true

router read_inst/fifo1_datain[8]

net three_state true

router read_inst/fifo1_datain[9]

net three_state true

router read_inst/fifo1_datain[10]

net three_state true

router read_inst/fifo1_datain[11]

net three_state true

router read_inst/fifo1_datain[12]

net three_state true

router read_inst/fifo1_datain[13]

net three_state true

router read_inst/fifo1_datain[14]

net three_state true

router read_inst/fifo1_datain[15]

net three_state true

router read_inst/fifo1_empty

net three_state true

router read_inst/fifo1_ren

net three_state true

router read_inst/packet_datain[0]

net three_state true

router read_inst/packet_datain[1]

net three_state true

router read_inst/packet_datain[2]

net three_state true

router read_inst/packet_datain[3]

net three_state true

router read_inst/packet_datain[4]

net three_state true

router read_inst/packet_datain[5]

net three_state true

router read_inst/packet_datain[6]

net three_state true

router read_inst/packet_datain[7]

net three_state true

router read_inst/packet_empty

net three_state true

router read_inst/packet_ren

net three_state true

router read_inst/rst net three_state true

router write_inst/N54 net three_state true

router write_inst/N55 net three_state true

router write_inst/add_97/carry[3]

net three_state true

router write_inst/buff_out[3]
net three_state true
router write_inst/buff_out[4]
net three_state true
router write_inst/buff_out[5]
net three_state true
router write_inst/buff_out[6]
net three_state true
router write_inst/buff_out[7]
net three_state true
router write_inst/clk net three_state true
router write_inst/fifo1_datain[0]
net three_state true
router write_inst/fifo1_datain[1]
net three_state true
router write_inst/fifo1_datain[2]
net three_state true
router write_inst/fifo1_datain[3]
net three_state true
router write_inst/fifo1_datain[4]
net three_state true
router write_inst/fifo1_datain[5]
net three_state true
router write_inst/fifo1_datain[6]
net three_state true
router write_inst/fifo1_datain[7]
net three_state true
router write_inst/fifo1_datain[8]
net three_state true
router write_inst/fifo1_datain[9]

net three_state true

router write_inst/fifo1_datain[10]

net three_state true

router write_inst/fifo1_datain[11]

net three_state true

router write_inst/fifo1_datain[12]

net three_state true

router write_inst/fifo1_datain[13]

net three_state true

router write_inst/fifo1_datain[14]

net three_state true

router write_inst/fifo1_datain[15]

net three_state true

router write_inst/fifo1_full

net three_state true

router write_inst/fifo1_wen

net three_state true

router write_inst/fifo2_wen

net three_state true

router write_inst/rst net three_state true

router buff_out_reg[0]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[1]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[2]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[3]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[4]/CP pin pin_on_clock_network_per_scn

true

router buff_out_reg[5]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[6]/CP pin pin_on_clock_network_per_scn
true
router buff_out_reg[7]/CP pin pin_on_clock_network_per_scn
true
router read_inst/clk pin pin_on_clock_network_per_scn
true
router write_inst/clk pin pin_on_clock_network_per_scn
true
router fifo2_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/read_clk
pin pin_on_clock_network_per_scn
true
router fifo2_inst/write_clk
pin pin_on_clock_network_per_scn
true
router fifo1_inst/write_clk
pin pin_on_clock_network_per_scn
true
router read_inst/select_output_reg_reg[1]/CP
pin pin_on_clock_network_per_scn
true
router read_inst/select_output_reg_reg[0]/CP
pin pin_on_clock_network_per_scn
true
router read_inst/packet_counter_reg[7]/CP
pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[2]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[3]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[4]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/packet_counter_reg[5]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router read_inst/cs_reg[1]/CP

pin pin_on_clock_network_per_scn

true

router write_inst/cs_reg[0]/CP

pin pin_on_clock_network_per_scn

true

router write_inst/cs_reg[1]/CP

pin pin_on_clock_network_per_scn

```
                                        true
router      write_inst/data_counter_reg[2]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      write_inst/data_counter_reg[1]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      write_inst/data_counter_reg[0]/CP
                pin     pin_on_clock_network_per_scn
                                        true
router      read_inst/clear_packet_count_reg
                cell    hdl_instance_name       clear_packet_count_reg
router      read_inst/cs_reg[0]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[0]
                cell    hdl_instance_name       cs_reg[0]
router      read_inst/cs_reg[1]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[1]
                cell    hdl_instance_name       cs_reg[1]
router      read_inst/cs_reg[2]
                cell    ff_edge_sense           1
router      read_inst/cs_reg[2]
                cell    hdl_instance_name       cs_reg[2]
router      read_inst/fifo1_ren_reg
                cell    hdl_instance_name       fifo1_ren_reg
router      read_inst/load_packet_count_reg
                cell    hdl_instance_name       load_packet_count_reg
router      read_inst/packet_counter_reg[0]
                cell    ff_edge_sense           1
```

```
router      read_inst/packet_counter_reg[0]
                cell    hdl_instance_name       packet_counter_reg[0]
router      read_inst/packet_counter_reg[1]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[1]
                cell    hdl_instance_name       packet_counter_reg[1]
router      read_inst/packet_counter_reg[2]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[2]
                cell    hdl_instance_name       packet_counter_reg[2]
router      read_inst/packet_counter_reg[3]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[3]
                cell    hdl_instance_name       packet_counter_reg[3]
router      read_inst/packet_counter_reg[4]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[4]
                cell    hdl_instance_name       packet_counter_reg[4]
router      read_inst/packet_counter_reg[5]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[5]
                cell    hdl_instance_name       packet_counter_reg[5]
router      read_inst/packet_counter_reg[6]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[6]
                cell    hdl_instance_name       packet_counter_reg[6]
router      read_inst/packet_counter_reg[7]
                cell    ff_edge_sense           1
router      read_inst/packet_counter_reg[7]
                cell    hdl_instance_name       packet_counter_reg[7]
```

```
router      read_inst/packet_dec_en_reg
                cell    hdl_instance_name       packet_dec_en_reg
router      read_inst/packet_ren_reg
                cell    hdl_instance_name       packet_ren_reg
router      read_inst/packet_valid_reg
                cell    hdl_instance_name       packet_valid_reg
router      read_inst/select_output_reg[0]
                cell    hdl_instance_name       select_output_reg[0]
router      read_inst/select_output_reg[1]
                cell    hdl_instance_name       select_output_reg[1]
router      read_inst/select_output_reg_reg[0]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[0]
                cell    hdl_instance_name       select_output_reg_reg[0]
router      read_inst/select_output_reg_reg[1]
                cell    ff_edge_sense           1
router      read_inst/select_output_reg_reg[1]
                cell    hdl_instance_name       select_output_reg_reg[1]
router      read_inst/temp_packet_data_reg[0]
                cell    hdl_instance_name       temp_packet_data_reg[0]
router      read_inst/temp_packet_data_reg[1]
                cell    hdl_instance_name       temp_packet_data_reg[1]
router      read_inst/temp_packet_data_reg[2]
                cell    hdl_instance_name       temp_packet_data_reg[2]
router      read_inst/temp_packet_data_reg[3]
                cell    hdl_instance_name       temp_packet_data_reg[3]
router      read_inst/temp_packet_data_reg[4]
                cell    hdl_instance_name       temp_packet_data_reg[4]
router      read_inst/temp_packet_data_reg[5]
                cell    hdl_instance_name       temp_packet_data_reg[5]
```

```
router      read_inst/temp_packet_data_reg[6]
                cell    hdl_instance_name       temp_packet_data_reg[6]
router      read_inst/temp_packet_data_reg[7]
                cell    hdl_instance_name       temp_packet_data_reg[7]
router      write_inst/clear_data_count_reg
                cell    hdl_instance_name       clear_data_count_reg
router      write_inst/cs_reg[0]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[0]
                cell    hdl_instance_name       cs_reg[0]
router      write_inst/cs_reg[1]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[1]
                cell    hdl_instance_name       cs_reg[1]
router      write_inst/cs_reg[2]
                cell    ff_edge_sense           1
router      write_inst/cs_reg[2]
                cell    hdl_instance_name       cs_reg[2]
router      write_inst/data_counter_reg[0]
                cell    ff_edge_sense           1
router      write_inst/data_counter_reg[0]
                cell    hdl_instance_name       data_counter_reg[0]
router      write_inst/data_counter_reg[1]
                cell    ff_edge_sense           1
router      write_inst/data_counter_reg[1]
                cell    hdl_instance_name       data_counter_reg[1]
router      write_inst/data_counter_reg[2]
                cell    ff_edge_sense           1
router      write_inst/data_counter_reg[2]
                cell    hdl_instance_name       data_counter_reg[2]
```

router write_inst/fifo1_datain_reg[0]

cell hdl_instance_name fifo1_datain_reg[0]

router write_inst/fifo1_datain_reg[1]

cell hdl_instance_name fifo1_datain_reg[1]

router write_inst/fifo1_datain_reg[2]

cell hdl_instance_name fifo1_datain_reg[2]

router write_inst/fifo1_datain_reg[3]

cell hdl_instance_name fifo1_datain_reg[3]

router write_inst/fifo1_datain_reg[4]

cell hdl_instance_name fifo1_datain_reg[4]

router write_inst/fifo1_datain_reg[5]

cell hdl_instance_name fifo1_datain_reg[5]

router write_inst/fifo1_datain_reg[6]

cell hdl_instance_name fifo1_datain_reg[6]

router write_inst/fifo1_datain_reg[7]

cell hdl_instance_name fifo1_datain_reg[7]

router write_inst/fifo1_datain_reg[8]

cell hdl_instance_name fifo1_datain_reg[8]

router write_inst/fifo1_datain_reg[9]

cell hdl_instance_name fifo1_datain_reg[9]

router write_inst/fifo1_datain_reg[10]

cell hdl_instance_name fifo1_datain_reg[10]

router write_inst/fifo1_datain_reg[11]

cell hdl_instance_name fifo1_datain_reg[11]

router write_inst/fifo1_datain_reg[12]

cell hdl_instance_name fifo1_datain_reg[12]

router write_inst/fifo1_datain_reg[13]

cell hdl_instance_name fifo1_datain_reg[13]

router write_inst/fifo1_datain_reg[14]

cell hdl_instance_name fifo1_datain_reg[14]

router write_inst/fifo1_datain_reg[15]
cell hdl_instance_name fifo1_datain_reg[15]
router write_inst/fifo1_valid_reg
cell hdl_instance_name fifo1_valid_reg
router write_inst/fifo1_wen_reg
cell hdl_instance_name fifo1_wen_reg
router write_inst/fifo2_wen_reg
cell hdl_instance_name fifo2_wen_reg
router write_inst/load_data_count_reg
cell hdl_instance_name load_data_count_reg
router write_inst/stop_packet_reg
cell hdl_instance_name stop_packet_reg
router write_inst/temp_fifo1_reg[0]
cell hdl_instance_name temp_fifo1_reg[0]
router write_inst/temp_fifo1_reg[1]
cell hdl_instance_name temp_fifo1_reg[1]
router write_inst/temp_fifo1_reg[2]
cell hdl_instance_name temp_fifo1_reg[2]
router write_inst/temp_fifo1_reg[3]
cell hdl_instance_name temp_fifo1_reg[3]
router write_inst/temp_fifo1_reg[4]
cell hdl_instance_name temp_fifo1_reg[4]
router write_inst/temp_fifo1_reg[5]
cell hdl_instance_name temp_fifo1_reg[5]
router write_inst/temp_fifo1_reg[6]
cell hdl_instance_name temp_fifo1_reg[6]
router write_inst/temp_fifo1_reg[7]
cell hdl_instance_name temp_fifo1_reg[7]
router read_inst/N30 net net_original_name SUM(1)
router read_inst/N32 net net_original_name SUM(3)

router read_inst/N34 net net_original_name SUM(5)

router read_inst/N35 net net_original_name SUM(6)

router read_inst/N36 net net_original_name SUM(7)

router read_inst/clk net net_original_name clk

router read_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router read_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router read_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router read_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router read_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router read_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router read_inst/fifo1_datain[8]

net net_original_name fifo1_datain[8]

router read_inst/fifo1_datain[9]

net net_original_name fifo1_datain[9]

router read_inst/fifo1_datain[10]

net net_original_name fifo1_datain[10]

router read_inst/fifo1_datain[11]

net net_original_name fifo1_datain[11]

router read_inst/fifo1_datain[12]

net net_original_name fifo1_datain[12]

router read_inst/fifo1_datain[13]

net net_original_name fifo1_datain[13]

router read_inst/fifo1_datain[14]

net net_original_name fifo1_datain[14]

router read_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router read_inst/fifo1_empty
net net_original_name fifo1_empty
router read_inst/fifo1_ren
net net_original_name fifo1_ren
router read_inst/ns[0] net net_original_name ns[0]
router read_inst/ns[1] net net_original_name ns[1]
router read_inst/ns[2] net net_original_name ns[2]
router read_inst/packet_counter[0]
net net_original_name packet_counter[0]
router read_inst/packet_counter[1]
net net_original_name packet_counter[1]
router read_inst/packet_counter[2]
net net_original_name packet_counter[2]
router read_inst/packet_counter[3]
net net_original_name packet_counter[3]
router read_inst/packet_counter[4]
net net_original_name packet_counter[4]
router read_inst/packet_counter[6]
net net_original_name packet_counter[6]
router read_inst/packet_counter[7]
net net_original_name packet_counter[7]
router read_inst/packet_datain[0]
net net_original_name packet_datain[0]
router read_inst/packet_datain[1]
net net_original_name packet_datain[1]
router read_inst/packet_datain[2]
net net_original_name packet_datain[2]
router read_inst/packet_datain[3]

net net_original_name packet_datain[3]

router read_inst/packet_datain[4]

net net_original_name packet_datain[4]

router read_inst/packet_datain[5]

net net_original_name packet_datain[5]

router read_inst/packet_datain[6]

net net_original_name packet_datain[6]

router read_inst/packet_datain[7]

net net_original_name packet_datain[7]

router read_inst/packet_empty

net net_original_name packet_empty

router read_inst/packet_output_1[0]

net net_original_name packet_output_1[0]

router read_inst/packet_output_1[1]

net net_original_name packet_output_1[1]

router read_inst/packet_output_1[2]

net net_original_name packet_output_1[2]

router read_inst/packet_output_1[3]

net net_original_name packet_output_1[3]

router read_inst/packet_output_1[4]

net net_original_name packet_output_1[4]

router read_inst/packet_output_1[5]

net net_original_name packet_output_1[5]

router read_inst/packet_output_1[6]

net net_original_name packet_output_1[6]

router read_inst/packet_output_1[7]

net net_original_name packet_output_1[7]

router read_inst/packet_output_2[0]

net net_original_name packet_output_2[0]

router read_inst/packet_output_2[1]

net net_original_name packet_output_2[1]
router read_inst/packet_output_2[2]
net net_original_name packet_output_2[2]
router read_inst/packet_output_2[3]
net net_original_name packet_output_2[3]
router read_inst/packet_output_2[4]
net net_original_name packet_output_2[4]
router read_inst/packet_output_2[5]
net net_original_name packet_output_2[5]
router read_inst/packet_output_2[6]
net net_original_name packet_output_2[6]
router read_inst/packet_output_2[7]
net net_original_name packet_output_2[7]
router read_inst/packet_output_3[0]
net net_original_name packet_output_3[0]
router read_inst/packet_output_3[1]
net net_original_name packet_output_3[1]
router read_inst/packet_output_3[2]
net net_original_name packet_output_3[2]
router read_inst/packet_output_3[3]
net net_original_name packet_output_3[3]
router read_inst/packet_output_3[4]
net net_original_name packet_output_3[4]
router read_inst/packet_output_3[5]
net net_original_name packet_output_3[5]
router read_inst/packet_output_3[6]
net net_original_name packet_output_3[6]
router read_inst/packet_output_3[7]
net net_original_name packet_output_3[7]
router read_inst/packet_ren

net net_original_name packet_ren

router read_inst/packet_valid_o1

net net_original_name packet_valid_o1

router read_inst/packet_valid_o2

net net_original_name packet_valid_o2

router read_inst/packet_valid_o3

net net_original_name packet_valid_o3

router read_inst/rst net net_original_name rst

router read_inst/select_output[0]

net net_original_name select_output[0]

router read_inst/select_output[1]

net net_original_name select_output[1]

router read_inst/select_output_reg[0]

net net_original_name select_output_reg[0]

router read_inst/select_output_reg[1]

net net_original_name select_output_reg[1]

router write_inst/N54 net net_original_name SUM(0)

router write_inst/N55 net net_original_name SUM(1)

router write_inst/N57 net net_original_name SUM(3)

router write_inst/N58 net net_original_name SUM(4)

router write_inst/N59 net net_original_name SUM(5)

router write_inst/N60 net net_original_name SUM(6)

router write_inst/N61 net net_original_name SUM(7)

router write_inst/add_97/carry[3]

net net_original_name carry(3)

router write_inst/add_97/carry[4]

net net_original_name carry(4)

router write_inst/add_97/carry[5]

net net_original_name carry(5)

router write_inst/add_97/carry[6]

net net_original_name carry(6)

router write_inst/add_97/carry[7]

net net_original_name carry(7)

router write_inst/buff_out[3]

net net_original_name buff_out[3]

router write_inst/buff_out[4]

net net_original_name buff_out[4]

router write_inst/buff_out[5]

net net_original_name buff_out[5]

router write_inst/buff_out[6]

net net_original_name buff_out[6]

router write_inst/buff_out[7]

net net_original_name buff_out[7]

router write_inst/clk net net_original_name clk

router write_inst/fifo1_datain[0]

net net_original_name fifo1_datain[0]

router write_inst/fifo1_datain[1]

net net_original_name fifo1_datain[1]

router write_inst/fifo1_datain[2]

net net_original_name fifo1_datain[2]

router write_inst/fifo1_datain[3]

net net_original_name fifo1_datain[3]

router write_inst/fifo1_datain[4]

net net_original_name fifo1_datain[4]

router write_inst/fifo1_datain[5]

net net_original_name fifo1_datain[5]

router write_inst/fifo1_datain[6]

net net_original_name fifo1_datain[6]

router write_inst/fifo1_datain[7]

net net_original_name fifo1_datain[7]

router write_inst/fifo1_datain[8]
net net_original_name fifo1_datain[8]
router write_inst/fifo1_datain[9]
net net_original_name fifo1_datain[9]
router write_inst/fifo1_datain[10]
net net_original_name fifo1_datain[10]
router write_inst/fifo1_datain[11]
net net_original_name fifo1_datain[11]
router write_inst/fifo1_datain[12]
net net_original_name fifo1_datain[12]
router write_inst/fifo1_datain[13]
net net_original_name fifo1_datain[13]
router write_inst/fifo1_datain[14]
net net_original_name fifo1_datain[14]
router write_inst/fifo1_datain[15]
net net_original_name fifo1_datain[15]
router write_inst/fifo1_full
net net_original_name fifo1_full
router write_inst/fifo1_wen
net net_original_name fifo1_wen
router write_inst/fifo2_wen
net net_original_name fifo2_wen
router write_inst/ns[0] net net_original_name ns[0]
router write_inst/ns[1] net net_original_name ns[1]
router write_inst/ns[2] net net_original_name ns[2]
router write_inst/packet_valid
net net_original_name packet_valid
router write_inst/rst net net_original_name rst
router write_inst/stop_packet
net net_original_name stop_packet

```
router      clk1            port    pin_on_clock_network_per_scn
                                                true
router      clk1            port    hdl_instance_name       clk1
router      clk2            port    pin_on_clock_network_per_scn
                                                true
router      clk2            port    hdl_instance_name       clk2
router      packet_in[0]    port    hdl_instance_name       packet_in[0]
router      packet_in[1]    port    hdl_instance_name       packet_in[1]
router      packet_in[2]    port    hdl_instance_name       packet_in[2]
router      packet_in[3]    port    hdl_instance_name       packet_in[3]
router      packet_in[4]    port    hdl_instance_name       packet_in[4]
router      packet_in[5]    port    hdl_instance_name       packet_in[5]
router      packet_in[6]    port    hdl_instance_name       packet_in[6]
router      packet_in[7]    port    hdl_instance_name       packet_in[7]
router      packet_out1[0]  port    hdl_instance_name       packet_out1[0]
router      packet_out1[1]  port    hdl_instance_name       packet_out1[1]
router      packet_out1[2]  port    hdl_instance_name       packet_out1[2]
router      packet_out1[3]  port    hdl_instance_name       packet_out1[3]
router      packet_out1[4]  port    hdl_instance_name       packet_out1[4]
router      packet_out1[5]  port    hdl_instance_name       packet_out1[5]
router      packet_out1[6]  port    hdl_instance_name       packet_out1[6]
router      packet_out1[7]  port    hdl_instance_name       packet_out1[7]
router      packet_out2[0]  port    hdl_instance_name       packet_out2[0]
router      packet_out2[1]  port    hdl_instance_name       packet_out2[1]
router      packet_out2[2]  port    hdl_instance_name       packet_out2[2]
router      packet_out2[3]  port    hdl_instance_name       packet_out2[3]
router      packet_out2[4]  port    hdl_instance_name       packet_out2[4]
router      packet_out2[5]  port    hdl_instance_name       packet_out2[5]
router      packet_out2[6]  port    hdl_instance_name       packet_out2[6]
router      packet_out2[7]  port    hdl_instance_name       packet_out2[7]
```

router packet_out3[0] port hdl_instance_name packet_out3[0]

router packet_out3[1] port hdl_instance_name packet_out3[1]

router packet_out3[2] port hdl_instance_name packet_out3[2]

router packet_out3[3] port hdl_instance_name packet_out3[3]

router packet_out3[4] port hdl_instance_name packet_out3[4]

router packet_out3[5] port hdl_instance_name packet_out3[5]

router packet_out3[6] port hdl_instance_name packet_out3[6]

router packet_out3[7] port hdl_instance_name packet_out3[7]

router packet_valid_i port hdl_instance_name packet_valid_i

router packet_valid_o1 port hdl_instance_name packet_valid_o1

router packet_valid_o2 port hdl_instance_name packet_valid_o2

router packet_valid_o3 port hdl_instance_name packet_valid_o3

router rst port hdl_instance_name rst

router stop_packet_send port hdl_instance_name stop_packet_send

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000010,DEPTH=32'h00000002

router fifo reference hdl_parameters DATA_WIDTH=16,DEPTH=2

router fifo reference hdl_template fifo

router fifo reference hdl_parameter_types

router fifo reference hdl_canonical_params DATA_WIDTH=32'h00000008,DEPTH=32'h00000040

router fifo reference hdl_parameters DATA_WIDTH=8,DEPTH=64

router fifo reference hdl_template fifo

SYNTHESIS RESULTS: -

Trial# (map effort)	**Area slack from area report**	**Timing slack from timing report**	**data required time for max path from timing report (Clk1 / Clk2)**	**data arrival time for the max path from timing report (Clk1 / Clk2)**
#1 (Low)	-813	4.11	3.15/9.15	-3.14/-5.04
#2 (Medium)	-815	4.11	3.15/9.15	-3.15/-5.04
#3 (High)	-810	4.11	3.15/9.15	-3.14/-5.04