DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY MIZORAM

DEVICE AND PROCESS MODELING LAB (ECP 2202)

VLSI LAB II (ECP 1801)

List of Experiments

1. Introduction to Silvaco.

2. Develop the structure of a SOI n-type MOSFET at 45 nm technology node with the specifications given in Fig. 01.

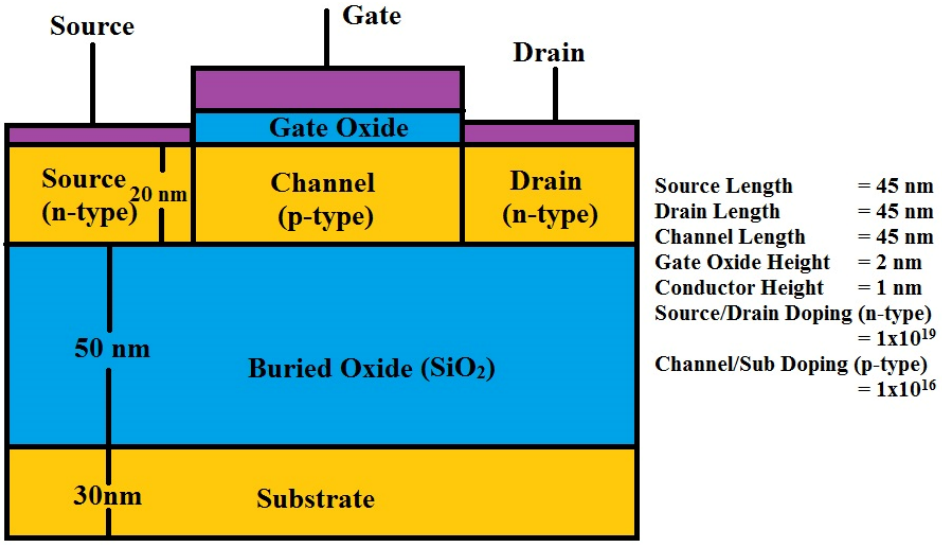
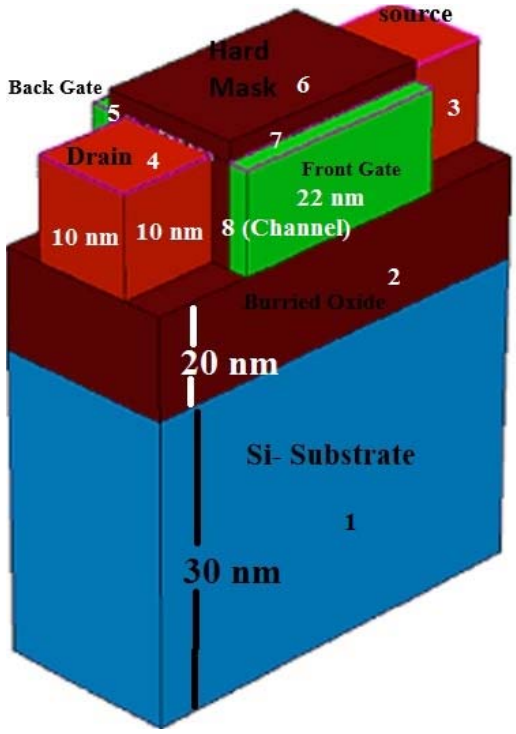


Fig. 01

3. Plot the transfer and output characteristics of the MOSFET developed in Experiment 02 and extract the threshold voltage, on current and leakage current at a drain voltage of 0.1 V. (V_{GS} is varied from 0 to 1 V)

4. Develop the structure of a SOI n-type Double Gate FET with a gate length of 22 nm with the specifications given in Fig. 02.



Substrate Height	**= 30 nm**
BOX Height	**= 20 nm**
Drain/Source Length/Height/Width	**= 10 nm**
Channel Length	**= 22 nm**
Gate Oxide Width	**= 2nm**
Conductor Width	**= 2 nm**
Source/Drain Doping (n-type)	**= 1 x 10^{19}**
Substrate/Channel Doping (p-type)	**= 1 x 10^{16}**

Fig. 02

5. Plot the transfer and output characteristics of the MOSFET developed in Experiment 04 and extract the threshold voltage, on current, leakage current, I_{on}/I_{off} current ratio and Subthreshold Swing at a drain voltage of 0.1 V. (V_{GS} is varied from 0 to 1 V)

6. Develop the structure of a SOI n-type Tri-gate FinFET at 14 nm technology node with the specifications given in Fig. 03.

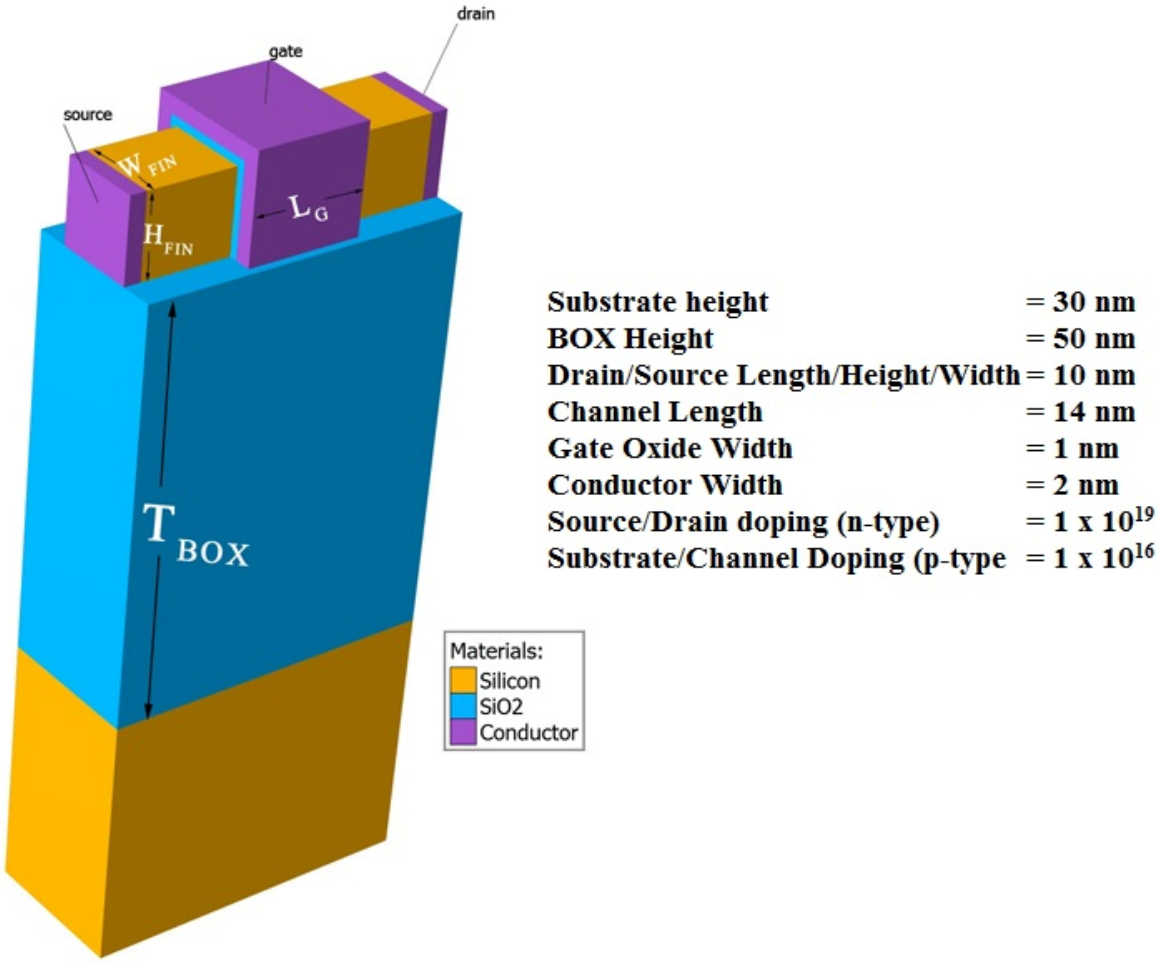


Fig. 03

7. Plot the transfer and output characteristics of the MOSFET developed in Experiment 06 and extract the threshold voltage, on current, leakage current, I_{on}/I_{off} current ratio, Subthreshold Swing and DIBL by considering a drain voltage of 0.1 V and 1.0 V. (V_{GS} is varied from 0 to 1 V)

8. Develop and analyze the above structures in p-channel.