How do I get the values of a previous time slice?

Make a cycle in your HDL part graph. At the initial time slice any internal pins are equal to 0. This only works because the D flip flop component is clocked, otherwise you would get an error in the hardware simulator.

Can I use the nand2tetris builtin chips in this project?

Yes. You may use available built-in chips for all chips except the ones you are required to construct in Project 3. Here is the spirit behind the use of builtin chips: you are encouraged to use the builtin versions for basic chips like many that you have already constructed in prior projects. That said, please do not submit the builtin versions of PC, RAM512 etc. because these are the functionalities we are asking you to build in Project 3. Apply good judgment in line with the spirit of this project. Once Project 3 is in the rear view, then we can use their builtin versions to construct higher order functionalities. The complete list of builtin chips is posted on TIPS channel on our TEAMS page.

Can I use my own custom chips instead of the nand2tetris builtin chips?

Yes. If you wish to use yours instead of built-in chips that's okay but keep in mind that in that case you open the possibility of a carryover 'mistake' and/or 'limitation' from past projects or otherwise that could be avoided if a built-in version was available.

Can I use the builtin Program Counter PC in building advanced chips, AggieCipher and Fibonacci?

Yes. Once you have constructed your own program counter PC chip, you may either use that in constructing other chips, or you may simply use the builtin PC chip in these other chips. Needless to say, you may not instantiate the builtin PC chip in constructing the PC chip itself :-)

Do we need to cover any specific test case in our test script?

No. The test scripts aren't part of your grade and all you are required to do is be confident that your chip is correct.

Are comments required to receive full credit?

No. Comments aren't a part of your grade. That said it is still worth doing for more complex chips to assist in your own understanding.

What happens when an input pin (or part of it) is left unspecified?

Pins default to 0 if they are not connected to another pin.

If a chip requires input of a larger size than I have, how can I pad it with zeroes?

Subslice the input so that it matches your bus, unspecified values will default to zero. For example, suppose you have a chip Add4(a[4],b[4],out[4]) and you want to add two 2-bit busses x and y. You would do it like so:

Add4(a[0..1]=x,b[0..1]=y);

What are some useful resources to start with?

I would like to recommend the following resource list for problems in Project 3 as follows:

- RAM512
  - **Basic principles:** V11 (https://www.youtube.com/watch?v=VFNO_Lkrv0o&feature=youtu.be) *timestamp 30.37.* Here you can learn how to construct RAM4 using FOUR 16-bit registers . Additionally, you may look at Recitation Video RV11 (https://www.youtube.com/watch?v=B_XxDX2BpqE&feature=youtu.be) *timestamp 35:55* to see details of RAM16 built with RAM4. You may apply the principles learnt here to construct RAM512 using the builtin RAM64 chips.
  - **HDL Implementation Technique: LAB 9 Video** (https://www.youtube.com/watch?v=Kzlr_uydVTg). This video and accompanying notes and collateral on LAB 9 archive on Canvas (LAB 9 LINK) will showcase actualy implementation of modular RAM.
- Program Counter (PC)
  - **Principles and Approach**: Lecture Video V11 (https://www.youtube.com/watch?v=VFNO_Lkrv0o&feature=youtu.be) at timestamp 54:56 showcases the process of constructing the program counter. Just remember a small error at timestamp 1:00:38 which is corrected in the accompanying slide in CL11 (LINK).
- Aggie Cipher
  - For this problem you only need to know the background of an adder (you may use the builtin adder Add16) and the program counter as a timer (you may use the builtin Program Counter PC) in order to construct the AggieCipher. One of the key realizations here is how to achieve the 'wraparound' effect of *0,1,2,3,4,5,6,....,15,0,1,2,.....* with a 16-bit counter. When in doubt, simulate the PC chip and watch the lower 4 bits 0..3.
- Fibonacci Sequence Generator
  - For this problem, follow the **schematic drawing of the sequence generator** in Project 3 Document closely just like you may have done for the barrel shifter in

> Project 2. Our goal for you to implement this chip is to see how functions are built in hardware to realize the performance gain from custom hardware. Draw the clocked waveforms for the output to convince yourself of the chip's working before you implement the HDL. It'll be much fun that way.

What is the precedence of the Program Counter flags?

In order of the highest priority you should handle reset first, load second, and increment last. For example, if you reset and load at the same time, the PC should reset.