Analysis and Design Techniques of CMOS Charge-Pump-Based Radio-Frequency Antenna-Switch Controllers

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***Abstract*—Analysis and design techniques of charge-pump-based RF antenna-switch controllers are presented. Loading effects of RF antenna switches that cause voltage drop of the controller have been identified and embedded in the analysis. The proposed analysis also captures effects of MOS-switch on-resistance and parasitic capacitances, so more precise descriptions of the charge-pump output voltage can be obtained. Furthermore, the body biasing technique has been employed to prevent latch-up. The analysis and the design techniques have been verified using a 0.35-μm CMOS technology. RF antenna-switch performances with the designed controller have also been measured and presented.**

***Index Terms*—Body bias, CMOS integrated circuits, charge pump circuits, RF antenna switches.**

I. Introduction

THE integration of multiple wireless standards has become a common feature of modern wireless terminals. This integration trend is driven not only by the need for increased coverage area in more continents but also by the desire to include more services such as the internet and GPS in a single wireless device. The increasing number of wireless standards integrated in a single wireless terminal demands more complicated functionality of RF antenna switches. The RF antenna switches have to meet wide arrays of specifications such as insertion loss, isolation, power-handling capability, and linearity at various output power levels in all frequency bands of interest for each integrated wireless standard.

Due to the requirement of watt-level power-handling capability for GSM and DCS/PCS applications and drawbacks of standard CMOS technology such as low quality factor, lossy substrate, and low breakdown voltage [1], gallium-arsenide (GaAs)-based technology such as pseudomorphic high-electron mobility transistor (p-HEMT) has prevailed in the development of high-power RF antenna switches. The advent of enhancement and depletion mode (E/D mode) p-HEMT technology even enabled the integration of a decoder in a single die with the RF antenna switches. Nevertheless, as more wireless standards such as GSM and DCS/PCS are integrated, a special control scheme becomes necessary for the RF antenna switches to maintain linearity of a high-power RF signal due to the negative threshold voltage of depletion mode (D mode) devices in p-HEMT GaAs technology. The most common scheme is to use a high bias voltage at the drain and source of the RF antenna switches. Since GSM and DCS/PCS require high output power of over 30 dBm and high linearity, it is necessary that the bias voltage is higher than a power supply voltage to satisfy linearity and isolation specifications of the RF antenna switches [2].

Charge pumps have been utilized to generate a higher voltage than the power supply voltage in LCD drivers [3], memory applications [4], [5], voltage regulator [6], sensors [7], and battery chargers [8]. In this paper, a charge pump is employed to generate the higher voltage for the RF antenna switches as shown in Fig. 1. Since the integration of the charge-pump-based controller with the RF antenna switches in the E/D mode p-HEMT technology leads to a larger area and higher cost, it is instead preferred that the controller be made in CMOS technology and the RF antenna switches be in the cost-effective D-mode-only p-HEMT technology as depicted in Fig. 1 [9]. The RF antenna switches cause voltage drop of the charge pump output, and this issue has been identified and embedded in the analysis and the design techniques to design the charge pump suited for the application of interest.

This paper is organized as follows. In Section II, an overview of the RF antenna-switch controller in CMOS technology is presented with a focus on the charge pump that generates the necessary voltage to control the RF antenna switches. Section III deals with the considerations of the loading effects resulting from parasitics of the p-HEMT RF antenna switches. Analysis and design techniques for the charge pump are discussed in Section IV. In Section V, measurement results of the designed controller are presented as well as the performance measurements of the RF antenna switches.

II. Antenna-Switch Controller

The block diagram of the RF antenna-switch controller that employs a charge pump is shown in Fig. 1 [9]. The RF antenna-switch controller consists of four subblocks: an oscillator, a charge pump, a decoder, and level shifters. As shown in Fig. 1, the oscillator generates two out-of-phase clock signals to drive the charge pump. Before the charge pump, there is an inverter

Manuscript received September 29, 2008; revised December 19, 2008. First published February 24, 2009; current version published May 20, 2009. This paper was recommended by Guest Editor H. Schmid.

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Digital Object Identifier 10.1109/TCSI.2009.2016129

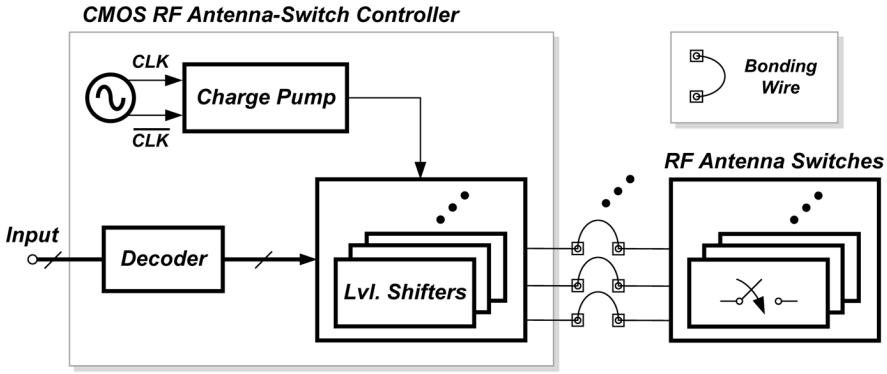


Fig. 1. Block diagram of RF antenna-switch controller.

chain as a clock buffer to provide adequate drive to the charge pump. Using the clock signals out of the buffer, the charge pump creates a voltage higher than power supply voltage. This high voltage is connected to level shifters, and the level shifter output switches between the high voltage and ground according to the decoder output. A conventional level shifter is used as in [9] and [10]. The decoder is utilized to reduce the number of input signals needed to control multiple RF antenna switches.

The first integrated charge pump to generate a voltage higher than a power supply voltage was introduced in [11]. This charge pump, however, suffers from a threshold voltage drop, resulting in a lower voltage gain and efficiency. For higher gain, many modified charge pumps have been proposed [4], [12]–[26]. To avoid the threshold voltage drop of the diode-connected transistors, additional MOS switches were used with the diodes [18]. Then, the charge pump using only MOS switches was introduced to further increase the voltage gain [22]. The more complex clock scheme was also used for higher efficiency [15].

In this paper, the charge pump with only MOS switches was used for the RF antenna-switch controller to maximize the voltage gain. However, the charge pump has a shortcoming that the pMOS switches may incur latch-up. The cause of the latch-up and the technique to avoid it, which was employed in this paper, are described in Section II-B.

A. Charge Pump Operations

Fig. 2 is the circuit diagram of a two-stage charge pump with MOS switches only [22]. Each stage of the charge pump is composed of four MOS switches, M_1–M_4, and two charging capacitors, C_1 and C_2. In one clock period, the MOS switches connecting two stages, for example, M_4 and M_6, are closed to pump charges into the next stage while the other MOS switches M_2 and M_8 are open to prevent the current from going back to the previous stage. In the next clock period, M_4 and M_6 are open to block the reverse current, and M_2 and M_8 are closed to charge the next stage. For instance, if CLK is low, the gate voltage of M_2 and M_4 becomes higher than its source/drain voltage because $\overline{\mathrm{CLK}}$ is high and the voltage across C_1 is added to $\overline{\mathrm{CLK}}$. Since M_2 is closed and M_4 is now open, C_2 is charged until the next clock cycle comes, as indicated with light arrows in Fig. 2. This process keeps repeating in a complementary manner as shown with arrows until all of the charging capacitors are

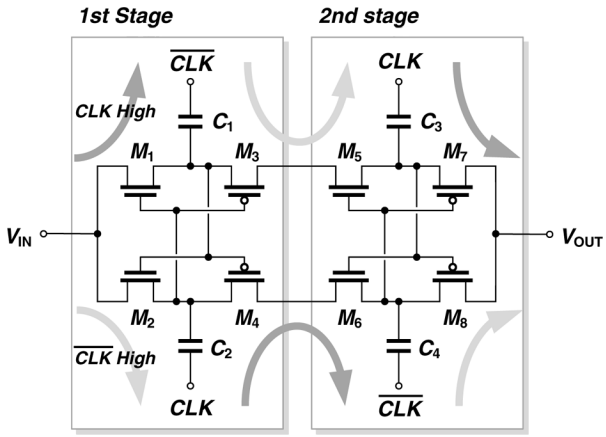


Fig. 2. Circuit diagram of a two-stage charge pump with only MOS switches.

charged to the power supply voltage if there is no output current. However, if there is output current, the charge pump should keep pumping in the extra charges every period at the cost of voltage drop. Therefore, it is necessary to identify the output current prior to the charge pump design to generate a certain voltage level. The voltage drop also depends on the charging capacitance and the on-resistance of the MOS switches. Thus, it is important to choose proper values of the charging capacitance and the MOS-switch width to design the charge pump, assuming the length of MOS switches are at minimum. At the end of the charge pump, there is an output capacitor acting as a filter that reduces ripple generated by the complementary charge pumping.

B. Body Biasing Technique

In Fig. 3(a), the body biasing circuit for the pMOS switches of the charge pump is shown. The auxiliary pMOS switches M_2 and M_3 connect the higher between the drain and the source of M_1 to the body [9], [19]. The body biasing circuit is necessary to keep the junction diodes between the drain/source and the body of the MOS switches reverse-biased at all time even before the voltage of the following stage is charged higher. As shown in Fig. 3(b), if the body of the MOS switch is tied to the output, the output voltage is lower than that of V_A, making the voltages at each node of the junction diode as shown in Fig. 3(c). This forward-biases the junction diode and allows charges to be

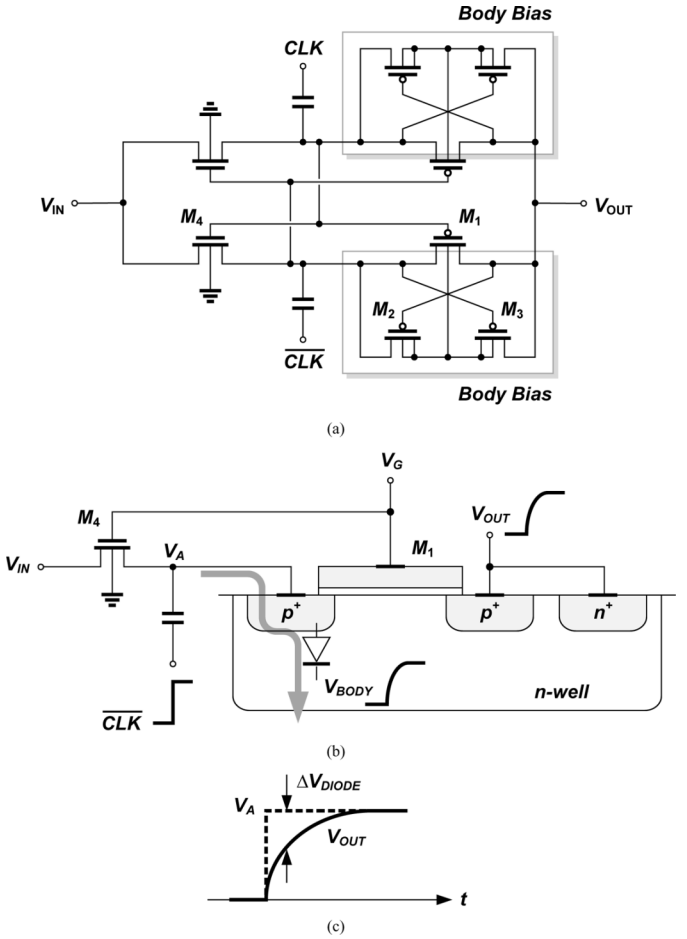


Fig. 3. (a) Body biasing circuit diagram. (b) Cross-sectional view of the pMOS switches. (c) Illustration of the voltage difference of the junction diode.

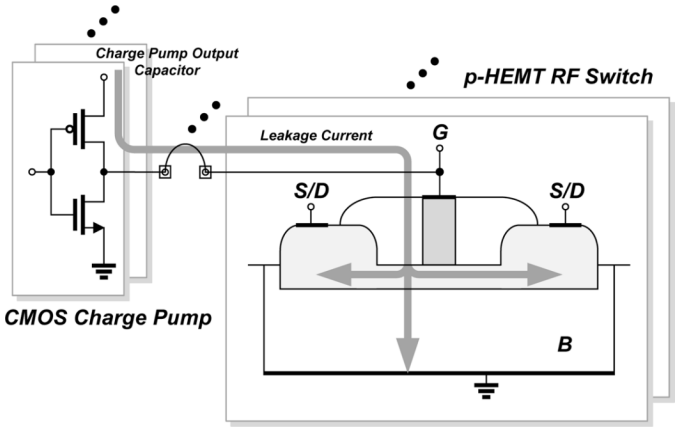


Fig. 4. Illustration of the leakage current drawn from the charge pump, reducing the output voltage.

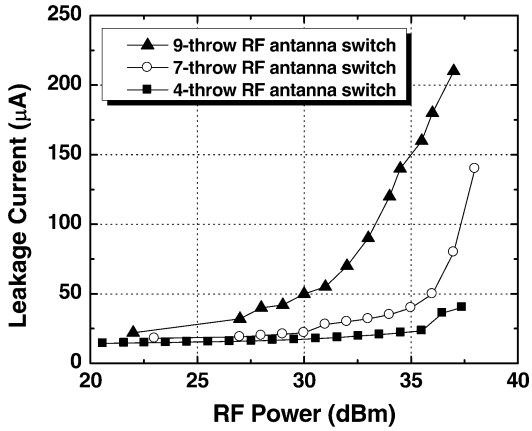


Fig. 5. Measured leakage currents from the charge pump to ground with different number of RF antenna switches.

dumped into the body, as shown in Fig. 3(b). This may cause latch-up and can damage the device. Thus, the body bias circuit is employed to prevent these problems for the charge pump circuits shown in Fig. 2.

III. Load Considerations

The RF antenna switches should ideally be seen as open to the charge pump due to the nature of the p-HEMT since the charge pump output is connected to a gate terminal. Thus, no charges can be drawn out from the output capacitor of the charge pump, resulting in no voltage drop. However, leakage current creates a current path from the charge pump to ground as shown in Fig. 4 [27]. When the output voltage of the charge pump is connected to the gate of the RF antenna switch to turn it on, the ideal open circuit looking into the gate becomes resistive because of the leakage current, and the quantity of the current is not negligible because the RF antenna switch is very large in size for high RF power. As the number of RF antenna switches increases to cover multiple wireless standards, the leakage current becomes larger as shown in Fig. 4. Moreover, the leakage current further increases as RF power going through the p-HEMT device rises because the voltage at the gate increases with higher RF power [27], [28]. This nonnegligible leakage current becomes problematic in designing the RF antenna-switch controller unlike memory or LCD applications because it decreases the output voltage of the charge pump. The measured increasing leakage current is shown in Fig. 5. As shown, the leakage current depends on the number of RF antenna switches and RF power. This nonnegligible leakage current flow lowers the output voltage of the charge pump, degrading linearity and isolation performances of the RF antenna switches [2]. Therefore, it is important to consider the load condition for the charge pump design, especially for multiple throw RF antenna switches. The design techniques described in Section IV take into account these loading effects in designing the charge pump.

IV. Charge Pump Circuit Analysis And Design

The circuit diagram of the charge pump with parasitic capacitances is shown in Fig. 6. C is a charging capacitor, and $C_{\rm PT}$ and $C_{\rm PB}$ are parasitic capacitances at the top layer and the bottom layer of the charging capacitor, respectively. In addition, $C_{\rm PT}$ includes the parasitic capacitance of the charge pump MOS switches, and $C_{\rm PB}$ includes the parasitic capacitance of the clock buffer.

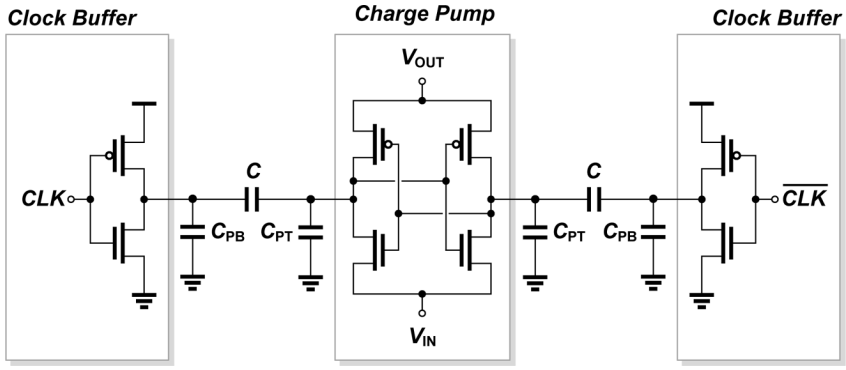


Fig. 6. Circuit diagram showing one stage of a charge pump with parasitic capacitances and clock-buffer stages.

A. Output Voltage

The first integrated charge pump was introduced and analyzed in [11]. The output voltage of the charge pump is given by

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}} + NV_{\mathrm{GAIN}} - \frac{NI_{\mathrm{OUT}}}{(C + C_{\mathrm{PT}})f} \tag{1}$$

where V_{IN} is the input voltage to the charge pump, V_{GAIN} is the voltage gain of each stage, N is the number of stages, I_{OUT} is the output current, and f is the clock frequency. The input voltage and the gain of each stage are reduced because of the threshold voltage and can be written as

$$V_{\mathrm{IN}} = V_{\mathrm{DD}} - V_{\mathrm{T}} \tag{2}$$

$$V_{\mathrm{GAIN}} = \left(\frac{C}{C + C_{\mathrm{PT}}}\right) V_{\mathrm{DD}} - V_{\mathrm{T}} \tag{3}$$

respectively. Due to its generality, (1) has been used as a model even for different topologies using MOS switches and capacitors as the charge-pumping medium. However, there are several aspects to be considered for a better description of the output voltage, such as on-resistance of the MOS switches, especially for the topology shown in Figs. 2 and 6.

The output voltage of the topology shown in Fig. 6 can be divided into four elements as

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}} + N(V_{\mathrm{GAIN}} - \Delta V_{\mathrm{I}} - \Delta V_{\mathrm{RC}}) \tag{4}$$

where ΔV_{I} is the voltage loss due to the output current and ΔV_{RC} is the voltage loss caused by the *RC* network, which is composed of the MOS-switch on-resistance and the charging capacitance including its parasitics. The first two elements, V_{IN} and V_{GAIN}, are the same as (1) except that the topology in Fig. 6 does not suffer from a threshold voltage drop [22].

To provide the output current, each branch of the charge pump delivers charges of $(C + C_{\mathrm{PT}})\Delta V_{\mathrm{I}}$ for each half clock period. Thus, the voltage loss due to the output current at each stage is given by

$$\Delta V_{\mathrm{I}} = \frac{I_{\mathrm{OUT}}}{2(C + C_{\mathrm{PT}})f} \tag{5}$$

where the factor 2 reflects the parallel structure of the charge pump in Fig. 6. The parasitic capacitance comes from the top-layer connections of the charging capacitors and the gate/drain capacitances of the MOS switches and is given by

$$C_{\mathrm{PT}} = \alpha C + C'W \tag{6}$$

where α is the ratio between the charging capacitance and the top-layer parasitic capacitance, $C'W$ is the parasitic capacitance of the MOS switches, and W is the width of the MOS switches.

As the clock frequency reaches tens of megahertz or higher to reduce ripple of the output voltage, the on-resistance of the MOS switches and the charging capacitance with its parasitic form a relatively slow *RC* network compared to ideal square signals, resulting in the voltage loss. The voltage loss can be written as

$$\Delta V_{\mathrm{RC}} = kV_{\mathrm{DD}} \left(\frac{C}{C + C_{\mathrm{PT}}}\right) e^{\frac{-1}{(2R_{\mathrm{ON}}(C + C_{\mathrm{PT}})f)}} \tag{7}$$

where R_{ON} is the on-resistance of the MOS switches. The factor k in (7) is introduced to prevent the voltage loss from being overemphasized, and this quantity depends on the output current because the increased output current further slows the charging process of the *RC* network. The k value tends to increase to reduce the output voltage as the size of the clock buffer decreases. Since the current level to charge the *RC* network is reduced with smaller buffer, it takes longer to charge the *RC* network, resulting in the voltage drop. The buffer size brings a tradeoff between the current consumption and the voltage drop as other design parameters. The effects of the buffer size will be discussed in the following section.

Substituting (5)–(7) into (4), the output voltage can be written as

$$V_{\mathrm{OUT}} = V_{\mathrm{DD}} + \left(\frac{N}{C + \alpha C + C'W}\right) \times \left(CV_{\mathrm{DD}} - (k' + k''I_{\mathrm{OUT}})CV_{\mathrm{DD}} e^{\frac{-W}{2R'(C + \alpha C + C'W)f}} - \frac{I_{\mathrm{OUT}}}{2f}\right) \tag{8}$$

where R' is the resistance per unit width of the MOS switches, and k' and k'' are experimentally determined factors to include the effects of the *RC* network. To provide insight on how the charging capacitance and the width of MOS devices change the output voltage, Fig. 7(a) and (b) are included. This shows the contributions toward the output voltage from each term in (4)

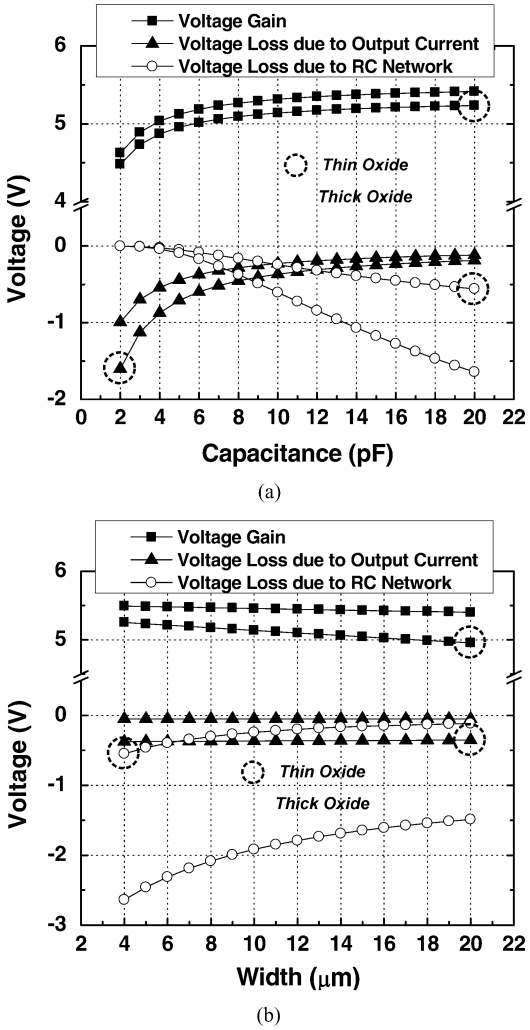


Fig. 7. Simulated voltages of each term in (4) toward the output voltage with (a) different charging capacitances and (b) with different widths of MOS devices.

where N is 2. It can be noted that, unlike (1), the output voltage is a function of both the charging capacitance and the width of the MOS switches. At first, the voltage gain increases as the charging capacitance increases. However, the voltage loss due to the *RC* network increases while the voltage gain saturates as shown in Fig. 7(a). Thick MOS devices suffer from higher voltage loss as charging capacitance increases due to more parasitic capacitance and lower transconductance. The width was fixed to be 10 μm. In Fig. 7(b), increasing width helps to decrease the voltage drop due to the *RC* network, but it decreases the voltage gain as well. In this case, thick MOS devices suffer from the slow *RC* network in a lot greater degree than thin MOS devices. The capacitance was set to be 10 pF. As a result, these two parameters should be deliberately chosen to generate the higher output voltage while providing the required output current. Moreover, it can be noted that the output current in (8) has larger effect on the output voltage compared to the analysis in (1). Hence, the load considerations described in Section III should precede the charge pump design. The proposed analysis allows to precisely expect the behavior of the output voltage as the charging capacitance and the width of MOS devices vary.

B. Current Consumption

The current consumption of the charge pump in Fig. 6 ideally depends only on the amount of the output current. However, the parasitic capacitances increase the current consumption of the charge pump [29]. The extra current consumption includes the dynamic current to drive the parasitic capacitance at the top layer of the charging capacitors and that at the bottom layer. Considering these parasitic effects, the current consumption of the charge pump is given by

$$I_{\mathrm{POWER}} = (N+1)I_{\mathrm{OUT}} + N(I_{\mathrm{CLK}} + I_{\mathrm{ST}}) \tag{9}$$

where I_{CLK} is the current to drive the bottom-layer parasitic capacitance and I_{ST} is the current to drive the top-layer parasitic capacitance. They can be written as

$$I_{\mathrm{CLK}} = 2\beta C V_{\mathrm{DD}} f \tag{10}$$

$$I_{\mathrm{ST}} = 2(\alpha C + C'W)\Delta V_n f \tag{11}$$

where β is the ratio between the charging capacitance and the bottom-layer parasitic capacitance and ΔV_n is the voltage swing across the charging capacitor. ΔV_n is the same as V_{GAIN} in (4). The factor of 2 in (10) and (11) comes from the parallel structure of the charge pump. Substituting (10) and (11) into (9), the current consumption becomes

$$\begin{aligned} I_{\mathrm{POWER}} =& (N+1)I_{\mathrm{OUT}} \\ &+ N\left(2\beta C V_{\mathrm{DD}} f + 2(\alpha C + C'W)\right. \\ &\left.\times\left(\frac{C}{C+\alpha C + C'W}\right)V_{\mathrm{DD}} f\right). \end{aligned} \tag{12}$$

The current consumption is also a function of the charging capacitance and the width of the MOS switches.

C. Analysis Verification

The proposed analysis was verified using the 0.35-μm CMOS technology. This technology does not provide a deep n-well process, so the body terminal of every nMOS device is tied together to a common substrate, which is ground. As the number of stages increases, the voltage differences between gate/drain/source and the body of nMOS devices become larger than the breakdown voltage, 8-V dc between junctions. The gate, source, and drain of nMOS devices for a two-stage charge pump are biased at 7 V. Three stages give that of 9.8 V, which is larger than the breakdown voltage. Thus, the number of stages cannot be increased larger than two with a power supply voltage of 2.8 V. Thus, the number of stages was chosen to be two, resulting in an output voltage less than 8 V. The process parameters such as C' and R' had been determined by simulations as well as k' and k''. To validate the analysis, simulations with a wide range of different parameters have been carried out.

Shown in Fig. 8 are the comparisons between the proposed analysis and simulation results. The width of the nMOS devices was fixed to be 5 μm while the width of the pMOS devices was varied because the on-resistance of the pMOS devices is a limiting factor. In addition to the higher mobility of the nMOS devices, the threshold voltage of the nMOS devices is smaller than that of the pMOS devices since the bulk of the nMOS devices is

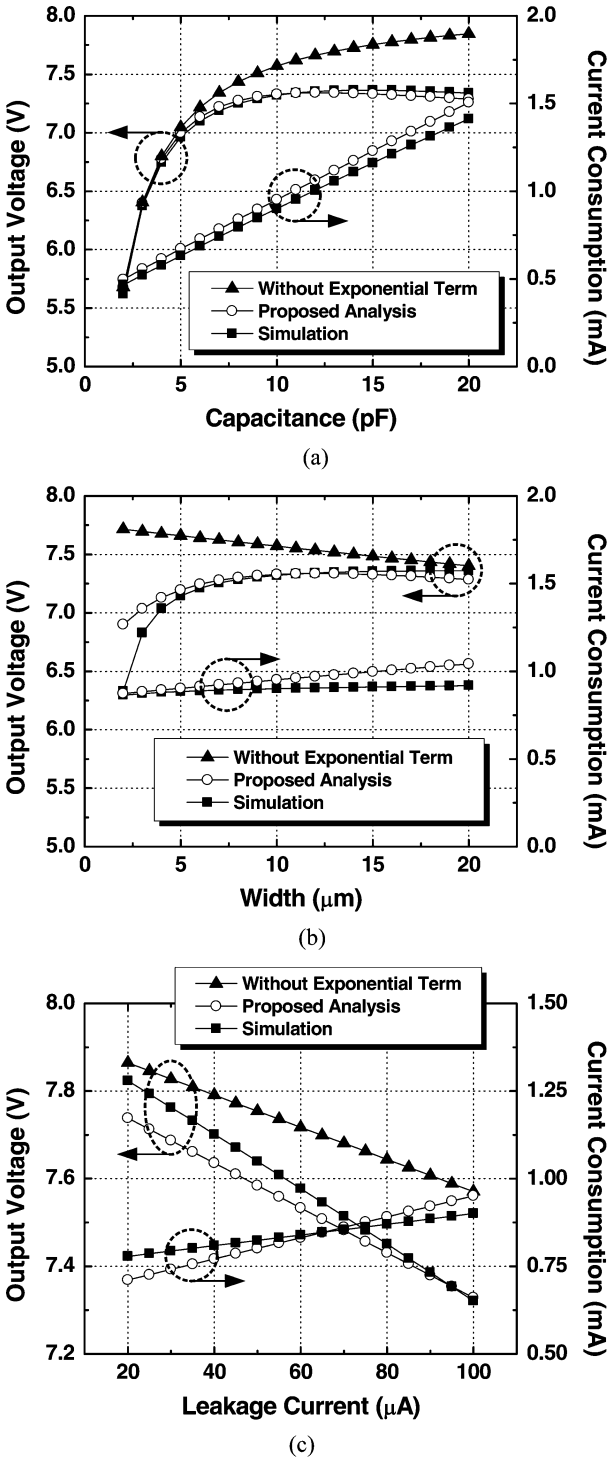


Fig. 8. Comparisons of output voltage and current consumption between the analysis and simulation: (a) with different charging capacitances, (b) with different widths of pMOS switches, and (c) with different output currents.

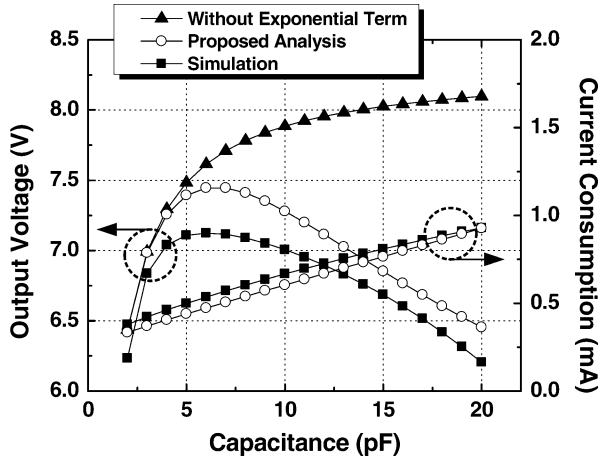
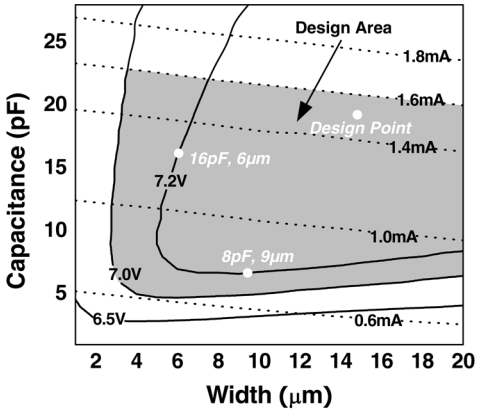


Fig. 9. Comparisons of output voltage and current consumption between the analysis and simulation with different charging capacitances.

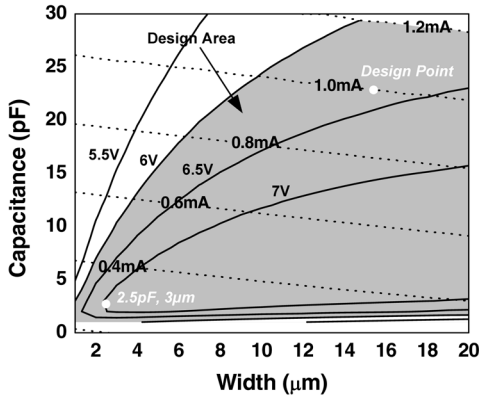
connected to ground while the gate voltage increases. Thus, the nMOS-device on-resistance does not affect the overall on-resistance as much as that of the pMOS devices does, and the larger nMOS devices only add more parasitic capacitance. First, output voltage and current consumption of the charge pump with different charging capacitances are shown in Fig. 8(a). The power supply voltage is 2.8 V, the output current is 100 μA, the pMOS width is 10 μm, and the parasitic capacitance factors, α and β, are 0.05 and 0.15, respectively. Considering ripple of the output voltage, the frequency of the clock was set to 25 MHz.

As shown in Fig. 8(a), the output voltage falls abruptly when the charging capacitance becomes less than 6 pF, and it saturates after 10 pF. The proposed analysis successfully captured the behavior of the output voltage. To show the ability of the proposed analysis to precisely describe the output voltage behavior, the analysis without the exponential term such as (1) and the analysis in [29] is also shown. The analysis without the exponential term does not follow the simulation results after 6 pF of the charging capacitance. Fig. 8(b) shows output voltage and current consumption with different widths for the pMOS switches. The charging capacitance is 10 pF. Similarly, the proposed analysis is able to describe the dependency of the output voltage on the pMOS width. Another simulation for output voltage and current consumption was done, varying the output current. The results are shown in Fig. 8(c). The charging capacitance and the width of each pMOS switch are 10 pF and 10 μm, respectively. As expected from the analysis, it was found that the output voltage is a function of both the charging capacitance and the width of the MOS switches. Both the analysis and the simulation show the same dependency on these two parameters. Compared to the analysis without the exponential term, the proposed analysis shows more closely matched results.

Fig. 9 shows the same comparisons as Fig. 8(a) with another set of design parameters to widen the applicability of the proposed analysis. Instead of 0.35-μm MOS devices, thick-oxide MOS devices with length of 0.5 μm were used. This changes the on-resistance and the parasitic capacitance of the MOS devices. Furthermore, the size of the clock buffers was minimized to provide just enough current to drive the charge pump with the lowest output leakage current so that it can be seen the buffer size also affects the output voltage drop as expected by (8). As shown in Fig. 9, the output voltage drops after 8 pF of the charging capacitance dissimilar to that shown in Fig. 8(a). There is an optimal capacitance value that gives the highest output voltage. The major difference between the results of Figs. 8(a) and 9 is the size of the clock buffers. As the buffer size decreases to save current, the output voltage



(a)



(b)

Fig. 10. Design area of the charge pump for the given requirements (a) for thin-oxide MOS devices and (b) for thick-oxide MOS devices.

drops rapidly with larger charging capacitances while the large enough buffer keeps the output voltage flat even with larger capacitances. Thus, it is important to size the buffer properly to keep the output voltage from dropping with larger capacitances, considering the output leakage current level to design the charge-pump-based controllers.

D. Design Strategy

The above analysis was applied to design a charge pump to drive the RF antenna switches with two different sets of design parameters detailed in Section IV. First, the target output voltage is given to be 7 V, using thin-oxide MOS devices with length of 0.35 μm. The power supply voltage is 2.8 V, and the maximum output leakage current is 100 μA. As mentioned earlier, because the 0.35-μm CMOS technology does not support the deep n-well process, the number of stages of the charge pump was set to be two to prevent the MOS switches from breaking down. The current consumption of the charge pump is required to be less than 1.6 mA. For low ripple of the output voltage, the clock frequency was set to be 25 MHz.

In Fig. 10(a), equal-voltage and equal-current lines generated by the analysis in (8) and (12) are shown on the same plot to determine the range of the charging capacitance and the width of the pMOS switches as free design variables. The shaded area represents the design area where the output voltage is over 7 V and the current consumption is less than 1.6 mA. The charging capacitance ranges from 5 to 21 pF, and the width of the pMOS switches should be larger than 3 μm to meet the requirements. Since the current consumption does not strongly depend on the width of the pMOS switches but rather on the charging capacitance, it is suggested that the width of the pMOS switches be increased to lessen current consumption and area by using the smaller charging capacitance. For example, the charging capacitance should be 16 pF to generate 7.2 V with the 6-μm pMOS switches where the charging capacitance only needs to be 8 pF with the 9-μm pMOS switches to generate the same voltage, as indicated in Fig. 10(a). The current consumption and the area can be reduced by employing the latter design strategy. In the design with the consideration of the RF antenna-switch load, however, the ripple of the output voltage is another important parameter to reduce the noise to the RF antenna switches. Furthermore, it was necessary to have a safe margin to guarantee the output voltage over 7 V. Thus, for fabrication, the charging capacitance was chosen to be 20 pF as shown in Fig. 10(a), where the output voltage is 7.4 V to have a margin of 0.4 V and ripple of the output voltage less than 30 mV.

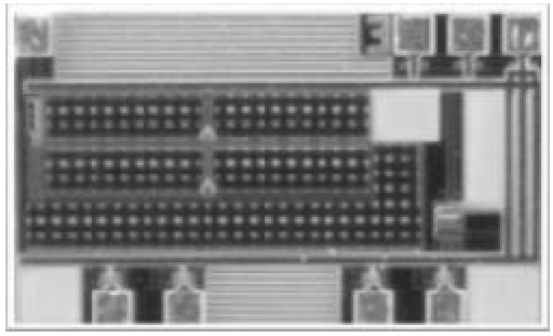
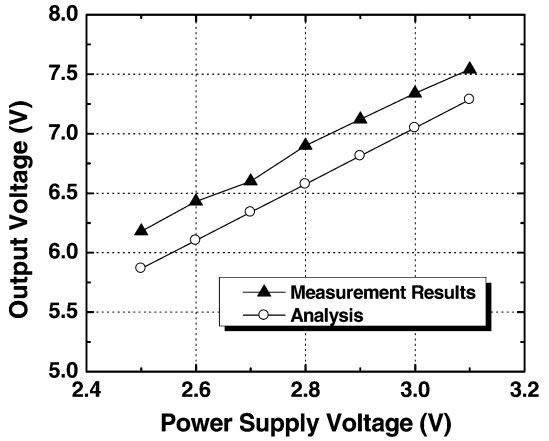


Fig. 11. Die photograph of the fabricated RF antenna-switch controller.

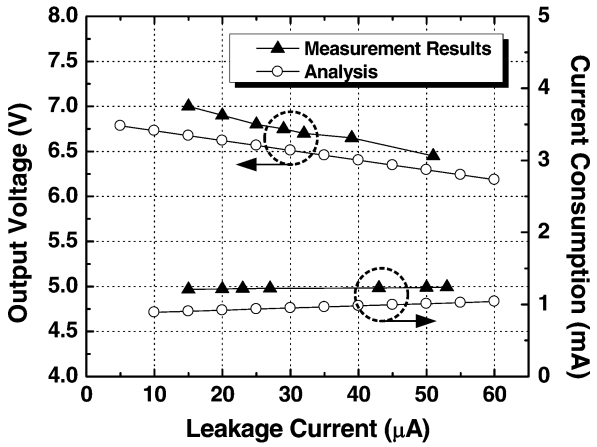
The thick-oxide MOS devices are used for the second set of design parameters. The length of MOS devices is 0.5 μm. The target output voltage is over 6 V with power supply voltage of 2.8 V. Maximum output leakage current is 60 μA. As the first case, the number of stages is set to be two. The current consumption should be less than 1.2 mA. The design area is shown in Fig. 10(b). As shown in the first design example, the design point at the lower left corner of the equal-voltage line, e.g., 2.5 pF and 3 μm, is the optimal point at the particular output voltage in terms of the output voltage and the current consumption. However, to reduce the ripple and have a safe margin of 0.4 V, the design point with 23 pF of charging capacitance and 15 μm of MOS device width has been selected for fabrication.

V. Measurements

The charge pump shown in Fig. 2 was fabricated in a 0.35-μm CMOS technology, using thick oxide MOS devices. Special care was taken to prevent electromigration effects from occurring in the layout since the tens of megahertz clock frequency may generate a relatively heavy current level during the charging and discharing period. A die photograph of the fabricated RF antenna-switch controller is shown in Fig. 11. The dimension of the switch controller is 1.16 mm $\times$ 0.68 mm. As mentioned in Section IV, the number of stages of the charge pump was



(a)



(b)

Fig. 12. Comparison of the output voltage (a) with different power supply voltages and (b) with different output currents between the analysis and measurements.

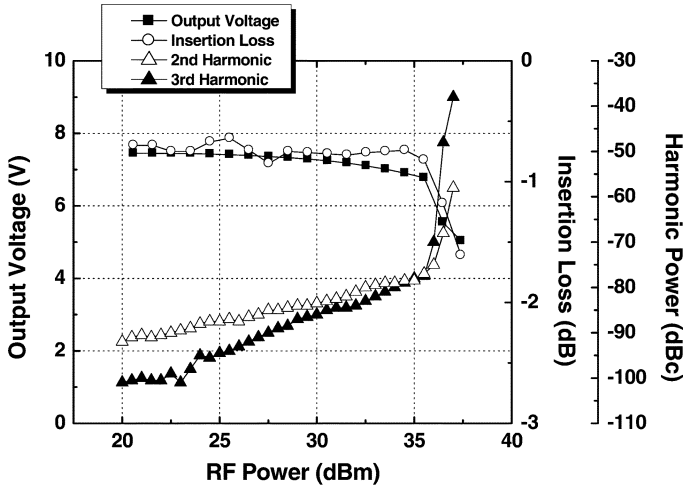


Fig. 13. RF antenna-switch performance measurements: insertion loss and harmonic powers of the RF antenna switches with charge-pump output voltage.

chosen to be two. The charging capacitance is chosen to be 23 pF to reduce the ripple at the output, and the width of the MOS switches is 15 μm. Shown in Fig. 12 are comparisons of the output voltage and the current consumption of analysis and measurements with different power supply voltages and output currents. The output current for Fig. 12(a) is 26 μA. The measurement results of the output voltage have a good agreement with the analysis. The ripple of the output voltage was measured to be less than 40 mV. The measured current consumption also follows the analysis. The parasitic capacitance ratio for the top-layer connections of the charging capacitor has been overly emphasized, resulting in lower voltage for the analysis than the measurements. This can be acceptable for the design to have an extra safe margin.

The performances of the RF antenna switches were also measured with the designed charge pump controlling the RF antenna switches. As mentioned earlier, the output power and the linearity requirements for the RF antenna switches are stringent, and the charge pump should sustain the high output voltage while providing the leakage current to the RF antenna switches. Shown in Fig. 13 are the insertion loss and the harmonic powers of the RF antenna switches. The insertion loss is less than 1 dB where the RF antenna-switch controller generates the output voltage over 6.5 V with power supply voltage of 3 V. The insertion loss increases as the output voltage decreases. The linearity measure of the RF antenna switches is shown by looking at harmonic powers. The RF antenna switches that support the various wireless standards such as GSM, PCS/DCS, and UMTS bands should support output power up to 35 dBm with less than -68 dBc of harmonics. The designed RF antenna-switch controller maintain the output voltage over 6 V so that the RF antenna switches can output 35 dBm of power with -70 dBc of the second and the third harmonics. The designed RF antenna-switch controller was able to generate sufficiently high voltage to drive the RF antenna switches while withstanding the output leakage current.

VI. Conclusion

The analysis and the design techniques of charge-pump-based RF antenna-switch controllers have been presented in this paper. The described approach takes into consideration the effects of the loading conditions for the charge pump, which vary with the RF input power to the RF antenna switches. Furthermore, the proposed analysis newly shows that the output voltage of the charge pump depends on both the charging capacitance and the width of the MOS switches. Analysis and design techniques of the charge pump were verified with the 0.35-μm CMOS technology. The measurement results show that the analysis matches well with the measurements and the designed controller can successfully drive the RF antenna switches while meeting the output power and the linearity requirements.

Acknowledgment

The authors would like to thank the staff at Samsung Yokohama Research Institute (SYRI) for testing and measurements.

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