A ±9 V Fully Integrated CMOS Electrode Driver for High-Impedance Microstimulation

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***Abstract*—A high-voltage electrode driver dedicated to intracortical microstimulation is presented. It is intended to significantly increase the voltage swing in order to maintain constant current stimulation through high-impedance electrode-tissue contacts. Charge pumps are used to generate high-voltage supplies of 8.615 V and -8.348 V from 3.3 V with low ripples (less than 1.6 %) while driving a maximal stimulation current of 200 μA. The negative charge pump architecture has been carefully implemented to suppress latch-up triggering. This high-voltage system is fully integrated and has been implemented with the C08E CMOS 0.8μm 5V/20V process from DALSA Semiconductor. The final output voltage compliance is 14.82 V, allowing constant current stimulation for an implantable *in-vivo* prototype.**

I. Introduction

With the downscaling of microelectronics technologies, implantable devices have become efficient solutions to recover lost functions of the human body [1]–[3]. They are used for neural signal acquisition in order to detect abnormal behaviors or to sense the user's intentions for artificial member control. They are also used to replace dysfunctional organs or neural command signals by stimulating peripheral nerves or specific regions of the cortex.

The interface formed with the stimulation electrode and the biological tissues has a highly variable impedance. This impedance being nonlinear, current stimulation is often preferred to voltage stimulation in many applications for security concerns [4]. Models of the electrode-tissue interface impedance have been proposed over time [5]. The impedance magnitude depends globally on the electrode geometry and material, but also on the stimulation frequency. It can reach very high values, in the order of 100 kΩ, especially for microelectrodes often used in intracortical implants. This is an important design constraint for an intracortical microstimulator because a maximal current of typically about 150 μA [1], [6] could be used. Considering these values, a voltage swing of 15 V would be required. This restriction is incompatible with the low-power limitation of these cortical stimulators. Most of these devices are supplied by batteries and are used daily. It is thus essential to lower their power consumption by using low-voltage CMOS circuit technologies. These standard CMOS processes do not support high-voltage operations, which limits the output voltage range. This issue is often neglected in stimulator designs. In these cases, discrete components are used to realize the high-voltage interface for *in-vivo* experimental prototypes [1]. These systems are thus not implantable.

Only a few have considered the high-impedance issue in their design. Some use voltage supplies as high as ±5.5 V [7], but the source delivering these voltages is unspecified and considered external. Moreover, the low-voltage circuitry is on the same 1.2μm chip as the output stage. Power consumption could thus be reduced by choosing a smaller process for the low-voltage section. More recently, [8] proposed a system that generates its own high-voltage supplies from a single 3.3 V. It uses two integrated circuits in different technologies in order to generate the high-voltages for the output stage while keeping the digital part in a low-voltage technology for reducing power consumption. Unfortunately, the latter design uses external capacitors which are to be avoided for an intracortical device and no specific attention was spent for the negative voltage generation leading to potential problems.

The proposed system is detailled in Section II and the post-layout simulation results are presented and discussed briefly in Section III.

II. Proposed system

In this paper, a fully integrated high-voltage constant current electrode driver for intracortical microstimulation is presented. This design is implemented with the C08E CMOS/DMOS 0.8μm 5V/20V process offered by DALSA Semiconductor. This quadruple well technology is adapted for multiple power supplies designs and its CMOS devices operate at supply voltages up to 20 V.

The different modules of the output stage are illustrated in Fig. 1. Briefly, this circuit generates high-voltage supplies of ±9 V from 3.3 V and increases the voltage compliance in order to stimulate through high-impedance microelectrodes. The stimulation pattern, considered as an arbitrary continuous waveform, would be generated by another chip made in low-voltage technology and is not presented here. The proposed

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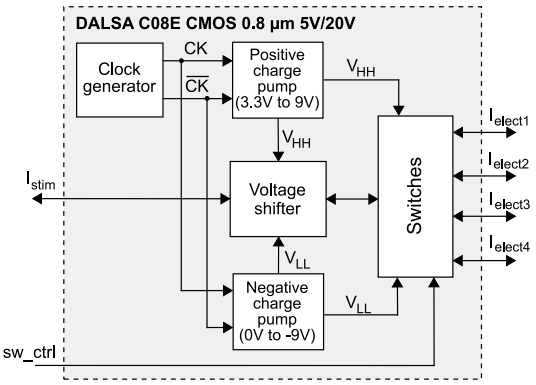

Fig. 1. Block diagram of the proposed high-voltage microelectrode driver

system can then be used as an output stage for any low-voltage microstimulator in order to perform *in-vivo* implantations.

A. Charge pumps

The Pelliconi charge pump [9] has been chosen for its small area and high efficiency. Moreover, it has been adapted and tested for DALSA's high-voltage CMOS process [10]. The basic positive stage, represented by Fig. 2a, is composed of low-voltage MOS transistors, which are isolated from the P-epitaxy substrate by deep N-wells. These devices are used as switches to transfer the charge from a pumping capacitor to another across the stages at each clock cycle.

The pumping capacitors C_p have been fixed to 25 pF. They are small enough to be integrated on the chip. The transistors *W/L* ratios are set to (100/1) μm for the NMOS devices (M_{Ni}) and to (200/1) μm for the PMOS devices (M_{Pi}). The positive charge pump is composed of two cascaded stages with the 3.3 V supply as input, as it is illustrated in Fig. 2b. According to [10], the same basic cell can be used to generate negative voltages by simply interchanging the input and output and using the ground as input. The resulting basic stage is shown in Fig. 2c. To reach a voltage of -9 V, three stages are required as shown in Fig. 2d.

The resulting V_{HH} and V_{LL} supply voltages are then used by the voltage shifter and the switches. The V_{LL} voltage being most negative voltage of the chip, it is connected to the P-epitaxy substrate. The load capacitances C_L for the positive and negative charge pumps consist of poly-poly capacitors of respectively 56.24 pF and 35.52 pF and of the parasitic capacitances from the wells, the pads and the substrate in the case of V_{LL}.

Simply switching the input and output to realize the negative charge pump is problematic, even if the NMOS and PMOS devices are in separated wells as it is proposed in [10]. Experimental results obtained by [8] have confirmed that a latch-up is triggered in its negative charge pump. Investigations have lead to the following observations. Before the negative charge pump is enabled, the P-epitaxy substrate is connected to V_{LL} which is near 0 V. During the first charge pumping cycles, there are short moments for which the interstage voltages of the negative charge pump (V_{m1} and V_{m2} in Fig. 2d) are lower

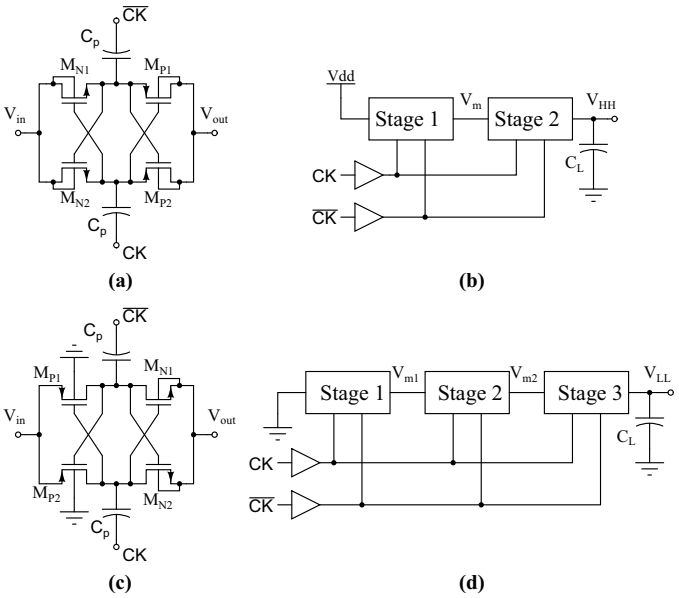

Fig. 2. Charge pumps architecture. (a) Positive pumping stage, (b) Positive charge pump composed of two stages, (c) Negative pumping stage, (d) Negative charge pump composed of three stages.

than the substrate voltage V_{LL}. This is due to the pumping mechanism that moves the charges at a rate of one stage per clock cycle. It thus takes a few cycles before the output voltage gets lower than V_{m1} and V_{m2}. If the sources of the PMOS transistors are connected to their bulk, i.e. to the deep N-wells as it is shown in Fig. 3a, latch-up circuits will then be triggered

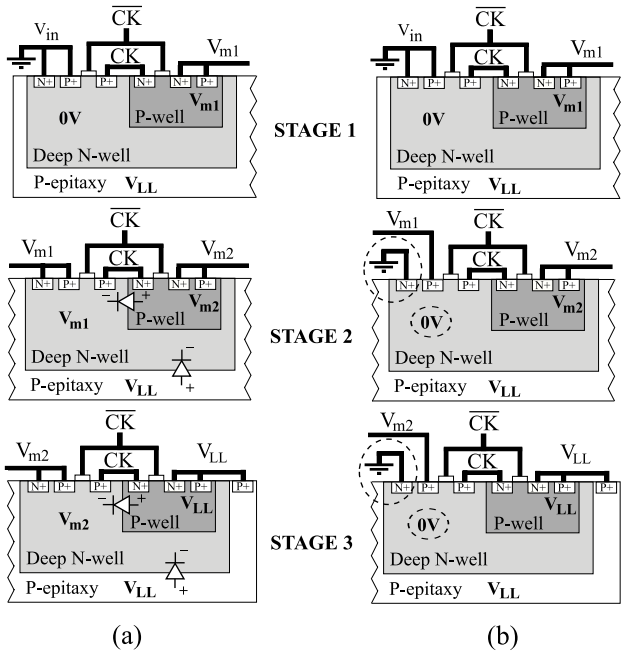

Fig. 3. Cross-sectional view of the wafer showing the well connections of the negative charge pump. (a) Deep N-wells tied to the source of the PMOS devices with the possible forward-biased PN junctions shown, (b) Deep N-wells tied to the ground

at start-up. To prevent this, the deep N-wells of the negative charge pump are all tied to the ground as in Fig. 2c and Fig. 3b.

B. Clock generator

The pumping mechanism of the charge pumps is driven by a two-phases clocking scheme. For more flexibility in the choice of the pumping frequency, the clocks are generated on-chip by a ring oscillator. The load of each clock phase being considerable, a special attention has been spent to design clock drivers large enough to drive the pumping capacitances.

C. Voltage shifter

This module increases the voltage swing of the stimulation without affecting the current. It consists of two paths of two stages of current mirrors. Each path either sources or sinks current to support biphasic stimulation. The first stage is composed of low-voltage MOS transistors supplied by 0 V and 3.3 V to interface the external stimulation generator realized in a low-voltage process. The second stage is composed of high side drain and source extended MOS devices as defined by DALSA. These devices are high-voltage transistors and are supplied with V_{HH} and V_{LL} in order to mirror the current at the output with an increased voltage swing.

The stimulation waveform is arbitrary and continuous, so linearity of the voltage shifter is essential. Cascode mirrors have been chosen to maximize the linearity by having a very high output impedance, resulting in a loss of voltage compliance.

D. High-voltage switches

In order to support the stimulation modes described in [1], a switch matrix is required to connect the four outputs to the desired node. Each electrode can be left floating or connected to I_{stim}, V_{HH} or V_{LL} to provide monopolar and bipolar biphasic stimulations for all electrodes.

III. Postlayout Simulation Results

The layout of the proposed system is shown in Fig. 4. The dimensions of the chip are 2.87 mm × 2.92 mm. All the following results were obtained from postlayout simulations.

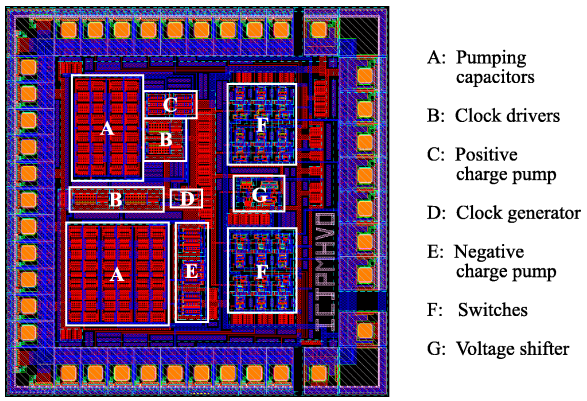

Fig. 4. Layout of the proposed high-voltage microelectrode driver

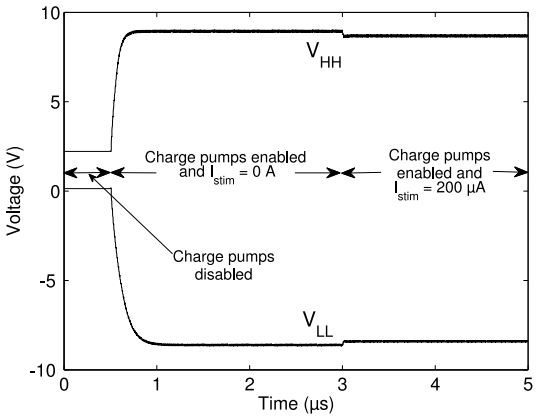

Fig. 5. Generated high-voltage supplies (V_{HH} and V_{LL}) variation

The charge pumps outputs, i.e. V_{HH} and V_{LL}, are shown in Fig. 5. It can be observed that V_{HH} = 2.22 V and V_{LL} = 136.8 mV when the charge pumps are disabled. With no load current, these voltages respectively reach 8.946 V and -8.610 V with peak-to-peak ripples of 131 mV and 96 mV respectively after the charge pumps are enabled. When a stimulation input current of 200 μA is applied, a voltage drop is observed and the outputs are V_{HH} = 8.615 V and V_{LL} = -8.348 V and the peak-to-peak ripples are respectively 136 mV and 102 mV. Under these conditions, power efficiencies of 41.77 % for the positive charge pump and of 35.88 % for the negative charge pump have been calculated.

The evolution of the voltages between the stages of the negative charge pump at the start-up has been observed to justify the well connections used and shown in Fig. 3b. The corresponding results are given by Fig. 6, where V_{m1} and V_{m2} are defined by Fig. 2d. During the first pumping cycle, it is noticed that V_{m1} and V_{m2} drop significantly lower than V_{LL}. For instance, at t = 1.02 μs, the interstage voltages are V_{m1} = -1.379 V and V_{m2} = -2.056 V, while the substrate voltage is V_{LL} = -325 mV. Having the bulk connected to the source for each PMOS device [8], [10] as shown in Fig. 3a, latch-

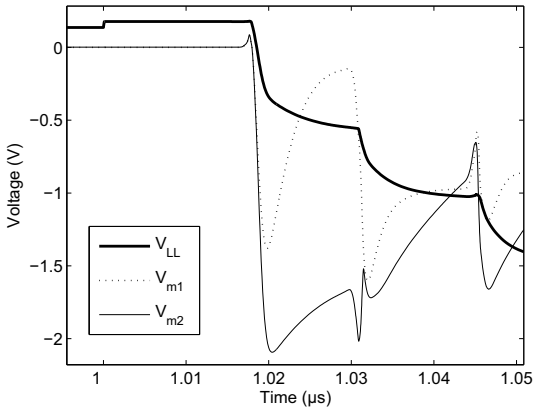

Fig. 6. Interstage voltages (V_{m1} and V_{m2}) and output voltage (V_{LL}) of the negative charge pump at start-up

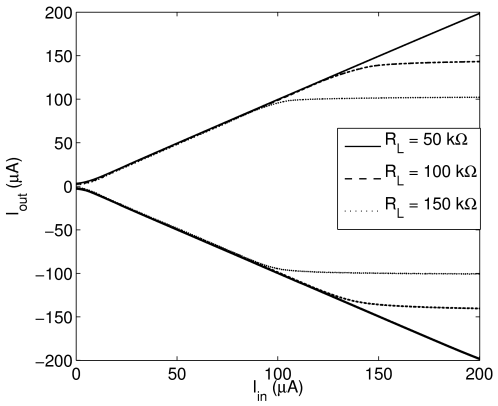

Fig. 7. Output stimulation current I_{out} versus input current I_{in} with the load impedance fixed at R_L = 50, 100 and 150 kΩ

up circuits will be triggered at that moment. Considering the third stage, the voltage differences between the deep N-well and both the P-epitaxy substrate and the P-well reache 1.731 V. Moreover, the voltage across the substrate and deep N-well of the second stage is 1.054V. All these corresponding PN junctions are strongly forward-biased. These results justify tying the deep N-wells to the ground as it is shown in Fig. 2c and Fig. 3b because these latch-ups are suppressed.

The linearity of the output stage is shown in Fig. 7 where the output current is represented in function of the input current from 0 to 200 μA with a load impedance (R_L) of 50, 100 and 150 kΩ. The voltage compliance of the output stage is 14.82 V for both sourcing and sinking stimulation currents. Hence, constant current as high as 100 μA can be driven through a electrode-tissue impedance up to 148.2 kΩ without any distorsion.

In stand-by mode, i.e. when the charge pumps are disabled, the power consumption for the whole circuit is 31.02 μW. It reaches 31.94 mW when driving a stimulation current of 200 μA. The parameters of the system proposed in this paper are compared to other stimulators found in the literature in Table I.

TABLE I
PARAMETERS AND RESULTS COMPARISON

	[8]* 2006	[6] 2007	This work 2009
Process	0.8μm	3μm	0.8μm
High-voltage interface	10 V	±5 V	±9 V
Maximum stimulation current	2 mA	127 μA	200 μA
Output voltage swing	8.25 V	$<$ 10 V	14.82 V
Results type	Experimental	Experimental	Postlayout simulations
Integration	External capacitors	External high-voltage supplies	Fully integrated

* Experimental results have shown that the negative charge pump is not functional.

IV. Conclusion

A high-voltage electrode driver dedicated to intracortical microstimulation has been presented. It is designed and implemented by DALSA C08E CMOS/DMOS 0.8μm 5V/20V process to significantly increase the output voltage compliance. It has the capability to drive high-impedance electrode-tissue interface while being fully integrated. A special attention has been spent on the negative voltage generation in order to realize a latch-up free negative charge pump. Postlayout simulation results show that supply voltages of 8.697 V and -8.415 V are generated with low ripples while I_{stim} = 200 μA. The corresponding output voltage compliance is 14.82 V. The proposed system clearly overcomes the high-impedance issue and brings the possibility to interface microelectrodes with any low-voltage microstimulator without using discrete components. Implantable prototypes for *in-vivo* experiments are then realizable.

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