Introduction

The program VDmostool creates a board level mosfet model from datasheet, which can only be used in LTspice. This is because it makes use of a new mosfet model called VDMOS and is only available in LTspice. This device replaces the subcircuit models, which you can find on the vendors websites. These subcircuit models can work but often they don't and if they do work the simulation runs too slow to make it use full. The VDmos model in LTspice is not a subcircuit but a new built in device model that uses a model statement. The has some more improvements which makes the simulation run much faster however, VDmos models for LTspice are not available and therefore the need of a tool came to make the models yourself right from the datasheet.

DC characteristics

When the program is started the tab DC characteristics is shown. All the textboxes are already filled in as an example. The values correspond to the 20N60C3 mosfet from Infineon.

General electrical characteristics

```
Rds_on  [160m ]  Ohm @ Vgs=[10 ]    V
Vgs(th) [3   ]  V    Rg [540m ]  Ohm  [?]
```

The first important parameter of a mosfet we need from the datasheet is the Rdson. This comes always with a test condition like the Drain current, temperature and gate source voltage. What we need is the typical Rdson at 25 degree C fully turned on, in many cases that's at 10V gate source voltage. Datasheet of the the example fet 20N60C3 shows:

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=13.1A				Ω
		T_j=25°C	-	0.16	0.19	
		T_j=150°C	-	0.43	-	

The second set of values is the gate threshold voltage Vgs(th) and the internal gate resistance Rg. Look for typical values at 25C.

Gate threshold voltage	$V_{GS(th)}$	I_D=1000µA, V_{GS}=V_D	2.1	3	3.9

The Rg parameter is not always specified but Infineon and recently ST does:

Gate input resistance	R_G	f=1MHz, open drain	-	0.54	-

Internal gate resistance Rg

If you happen to have a mosfet where the internal gate resistance is not specified you could click on the question mark button and a window pops up. In this window you are asked to enter switching times and gate charges at certain test conditions. This little window is trying to guesstimate the gate resistance. This method is not very accurate but it is better then using zero or a user a wild guess.

| Turn-on delay time | $t_{d(on)}$ | V_{DD}=380V, V_{GS}=0/13V, I_D=20.7A, R_G=3.6Ω, T_j=125 | - | 10 | - | ns |

Gate Charge Characteristics

Gate to source charge	Q_{gs}	V_{DD}=480V, I_D=20.7A	-	11	-	nC
Gate to drain charge	Q_{gd}		-	33	-	
Gate charge total	Q_g	V_{DD}=480V, I_D=20.7A, V_{GS}=0 to 10V	-	87	114	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=480V, I_D=20.7A	-	5.5	-	V

This tool calculates an internal gate resistance when you hit the OK button. In this example it calculates 2.2 Ohm while the spec mentions 0.54 Ohm. When 10V is used for the gate driver voltage it calculates 0.52 Ohm. It could be a typo in the datasheet for the driver voltage.

Transfer and output characteristics

Transfer Characteristics

| Vgs (V)		Id (A)
5.5	?	20.7
7.5	?	70

Vds Test 50 V

Output Characteristics

Vds range 25 V

The next step in the DC modeling process is to model the transfer characteristics of the mosfet. What is meant by this is the drain current vs the gate source voltage in saturated region. The saturated region of a mosfet is the part of the output characteristics were the fet behaves like a current source (practically no change in Id when Vds is changed). The output and transfer characteristics are very related to each other.

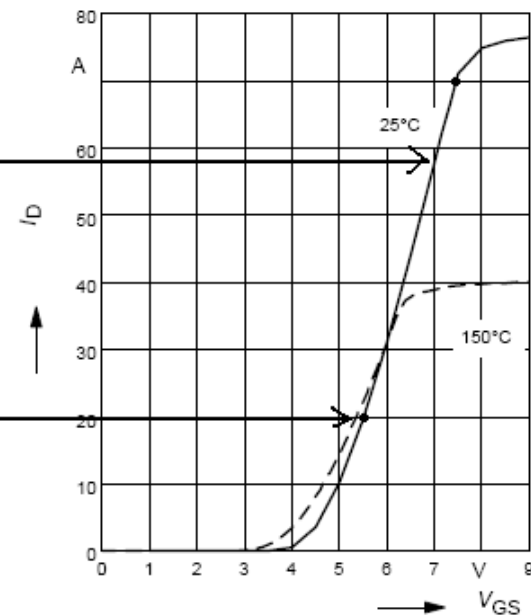### 7 Typ. output characteristic

$I_D = f(V_{DS})$; $T_j = 25°C$

parameter: $t_p = 10 \mu s$, V_{GS}
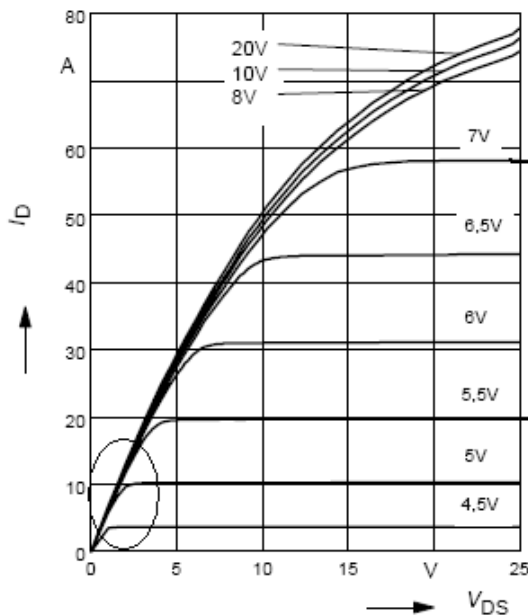
11 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

parameter: $t_p = 10 \mu s$

The tool requires two value pairs from the transfer characteristics. The first value pair is preferably the gate source plateau voltage and the test current from the gate charge characteristics, which are in this case 20.7A and a gate plateau voltage reading of 5.5V. The second value pair must be chosen at a higher gate voltage. In the example 7.5V and

70A is used, but 6V and 31A could be used too. The Vds test value is the drain source voltage test condition mentioned in the Transfer characteristics. The example mosfet shows that this voltage is a function of the Rdson and drain current. Using 50V makes sure that the fet is always in the saturated region and the output characteristics of the example fet shows that this mosfet has no significant change in drain current as function of Vds in the saturated region so 25V could be used too. Finally but not mandatory is the value entering field for the Output characteristics. You are asked to type in the Vds range (0 is always the starting point). This is used for the test circuits under the menu item "file-> save test circuits", which the program generates, not for making the model.

12 Typ. gate charge

$$V_{GS} = f\ (Q_{Gate})$$

parameter: $I_D = 20.7$ A pulsed
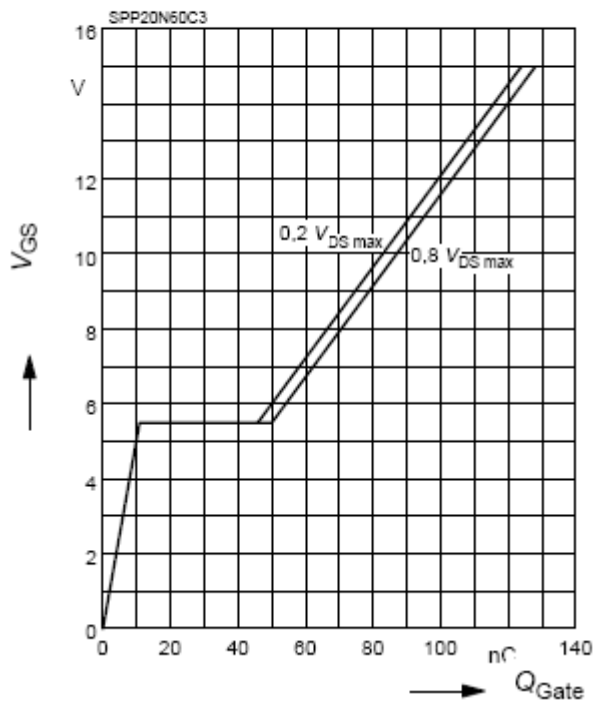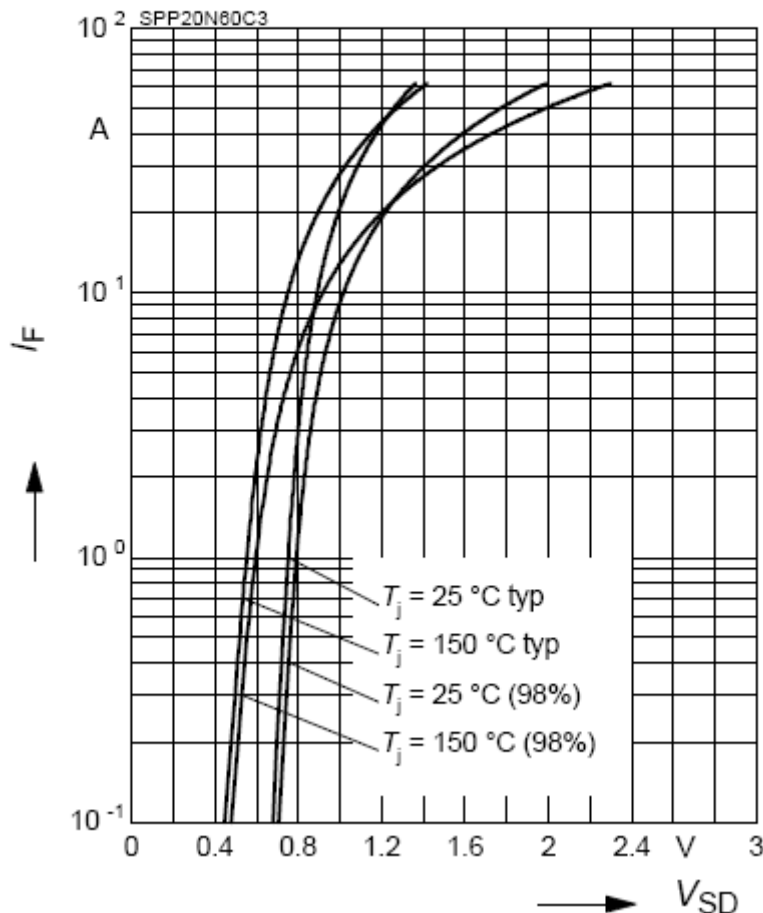
Body diode DC forward characteristics

Body Diode DC Forward

Vsd	Isd
700m	400m
800m	3
1.2	45

Here you are required to enter three value pairs for the source to drain voltage and source to drain current. The solver for the body diode model is most accurate if the first two value pairs are decades lower then the last value pair. This could be a hard job to read the forward characteristics from the datasheet so you might want to measure it with a simple power supply and two multi meters.
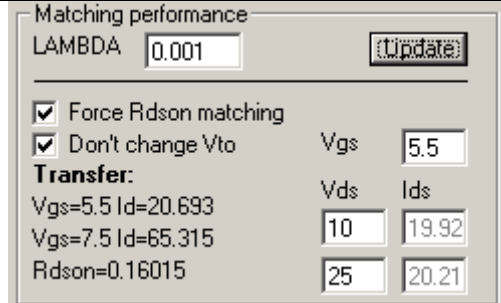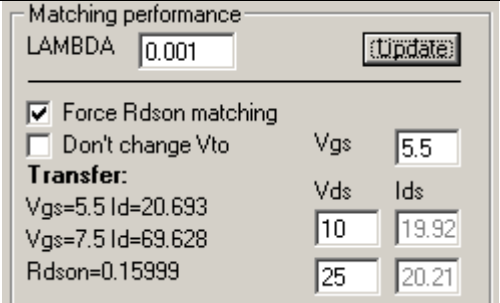
13 Forward characteristics of body diode

$$I_F = f(V_{SD})$$

parameter: T_j , tp = 10 µs

SPP20N60C3

$T_j = 25\ °C$ typ

$T_j = 150\ °C$ typ

$T_j = 25\ °C$ (98%)

$T_j = 150\ °C$ (98%)

I_F

V_{SD}

Matching performance

This relaxes the matching of the second value pair of the transfer graph	This setting allows the solver to change Vto to have both value pairs matched.
Matching performance LAMBDA 0.001 [Update] ☑ Force Rdson matching ☑ Don't change Vto Vgs 5.5 **Transfer:** Vds Ids Vgs=5.5 Id=20.693 Vgs=7.5 Id=65.315 10 19.92 Rdson=0.16015 25 20.21	Matching performance LAMBDA 0.001 [Update] ☑ Force Rdson matching ☐ Don't change Vto Vgs 5.5 **Transfer:** Vds Ids Vgs=5.5 Id=20.693 Vgs=7.5 Id=69.628 10 19.92 Rdson=0.15999 25 20.21

The purpose of this part of the tool is to give the user a preview of how well the model performs regarding the transfer and output characteristics. Since the VDmos model uses the level-1 DC equations (and is implemented in the program to solve the drain current as function of Vgs and Vds), it is very likely that not all entered datasheet values are matched. You can play here with the LAMBDA parameter and solver checkboxes to get a satisfied matching of the datasheet. Things that should match is at least the Rdson and the first value pair of the transfer characteristics (The 5.5V and 20.7A) and finally the Vto should be close to the datasheet Vgs(th) value. The rest is nice to have because 10% matching error is very normal for the level-1 model.

AC characteristics
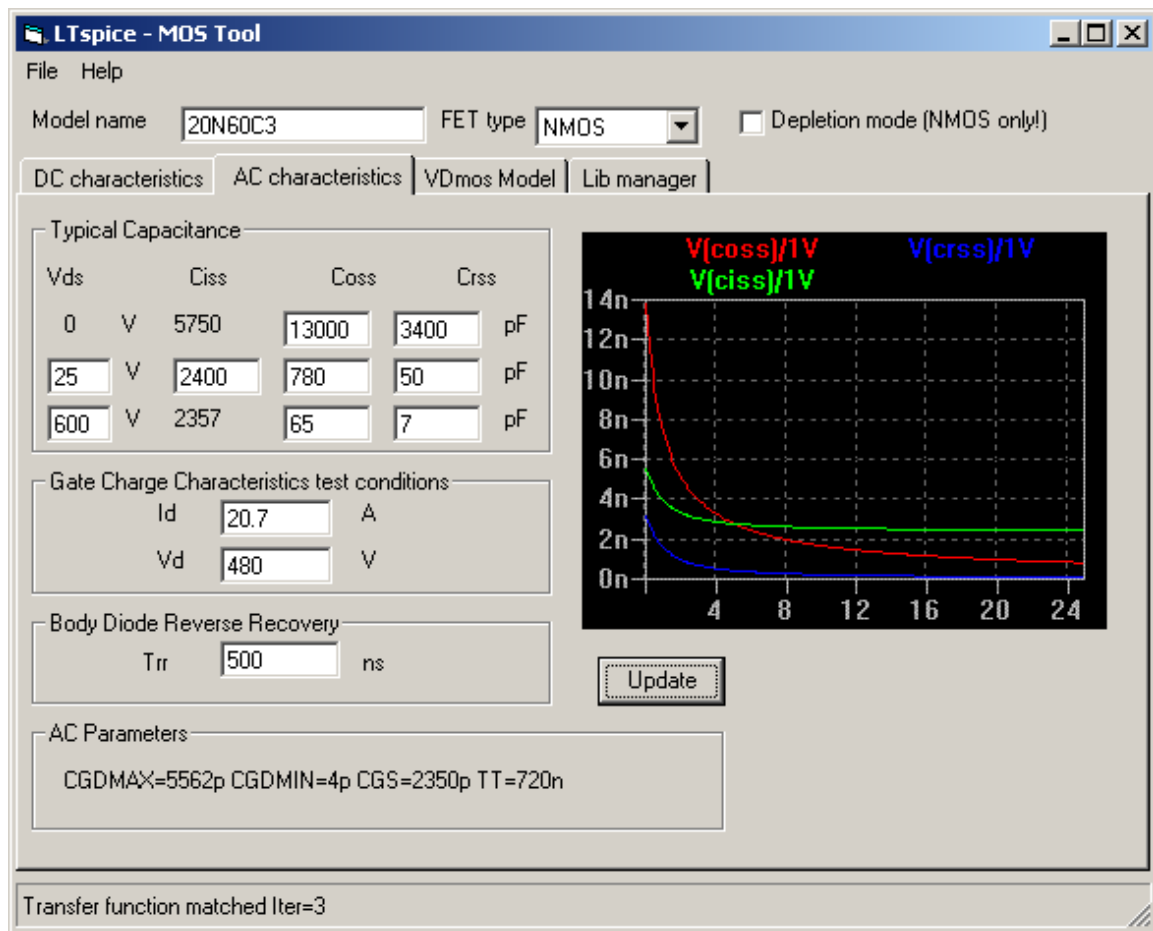
The user is asked here to enter values from the typical capacitance plot at three different drain source voltages. At Vds = 0V the output and reverse (miller) capacitance are needed. You can try to read the datasheet graph. If it's too hard to read you can try a workbench measurement for the Coss. For such high power fets a simple capacitance meter can measure this. Short the gate to the source and measure the drain source capacitance. The Crss is not so easy to measure. You need to somehow measure the HF current from the gate to source with a known HF small signal voltage on the drain source and then calculate the Crss from vds and igs. You could still try to read it from the datasheet graph once you know what the Coss is and the Coss is always higher then Crss.

The second set of capacitance values (25V or 10V) can easily be found in the datasheet table:

Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V,	-	2400	-	pF
Output capacitance	C_{oss}	f=1MHz	-	780	-	
Reverse transfer capacitance	C_{rss}		-	50	-	

The third and last set of capacitance values is not very critical. It is meant to be the readings from the capacitance graph at the highest Vds.

The gate charge test conditions are also found in the table on the datasheet at the parameter Gate Plateau Voltage:

Gate Charge Characteristics

| Gate to source charge	Q_{gs}	V_{DD}=480V, I_D=20.7A	-	11	-	nC
Gate to drain charge	Q_{gd}		-	33	-	
Gate charge total	Q_g	V_{DD}=480V, I_D=20.7A, V_{GS}=0 to 10V	-	87	114	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=480V, I_D=20.7A	-	5.5	-	V

These values are used for the test circuits under the menu item "file-> save test circuits", not for making the model. If you like you can omit them or what ever.

Test circuits for LTspice

Once you have finished putting in all the datasheet values and you have successfully created a model line you can check the performance of the mosfet in LTspice by saving the test circuits under the menu item file->save testcircuits.
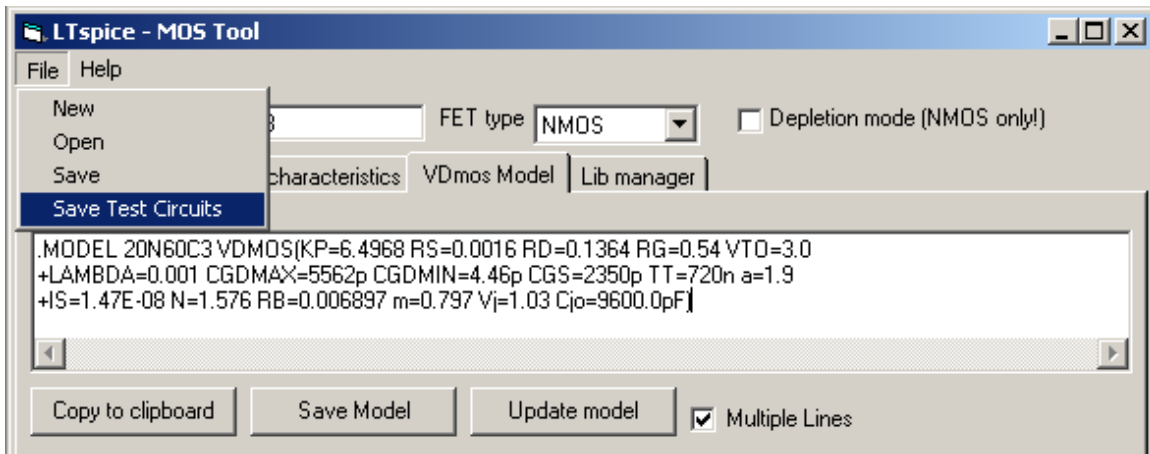
Now open LTspice and open one of the circuits you want to simulate. Here a screen shot of all the circuits at once.
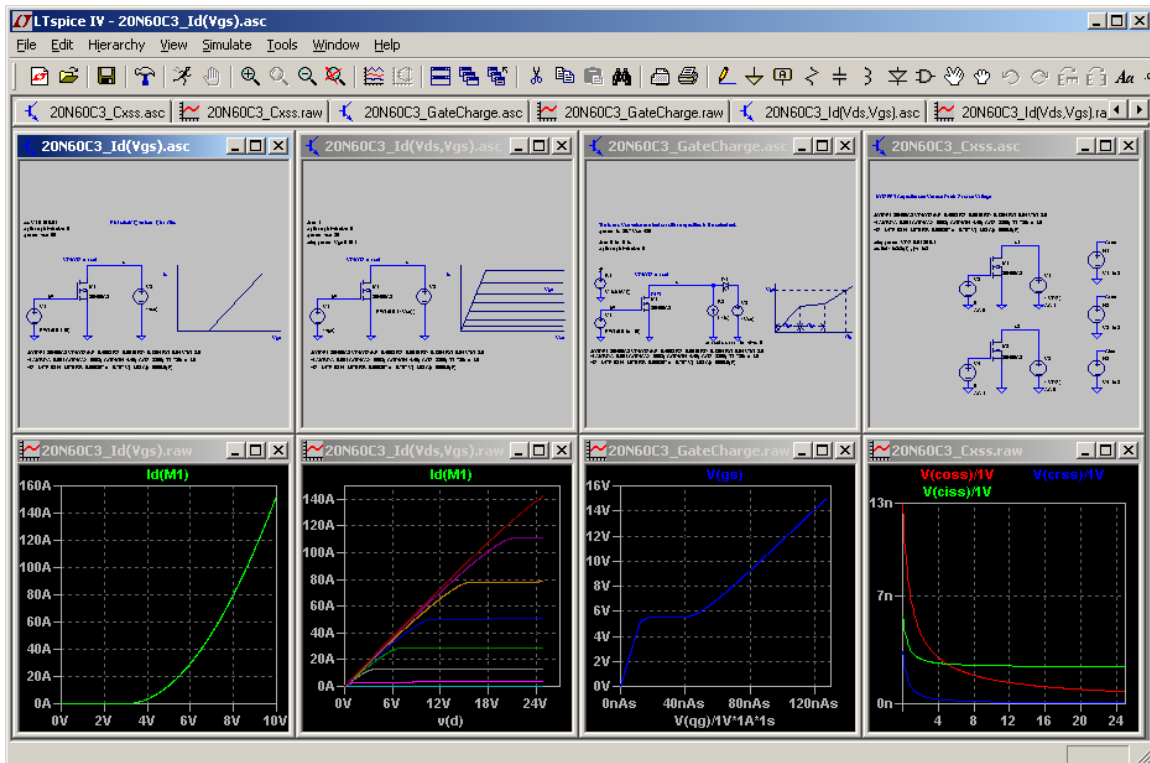
VDmos model
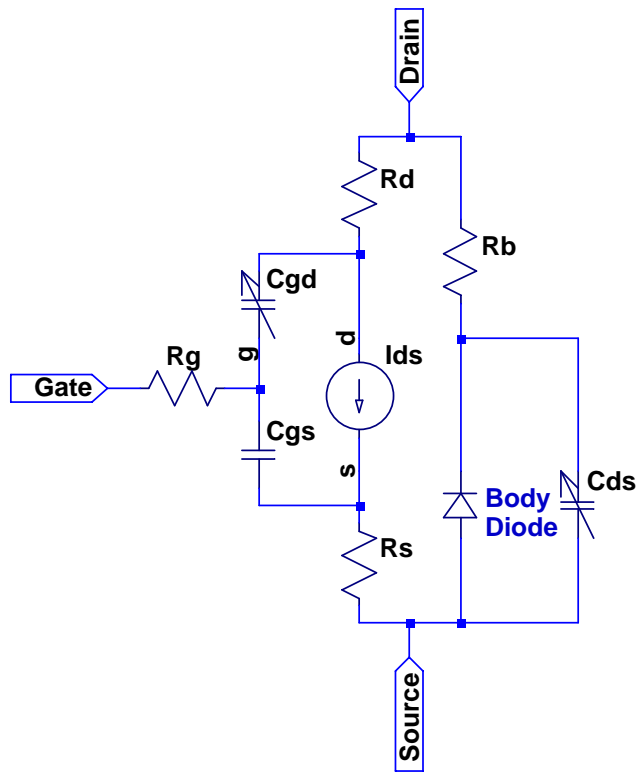
LEVEL 1 Model Equations

Cuttoff region: Vgs<Vto

Ids=0

Linear Region: Vds<Vgs-Vto

Ids=KP* W/L * (1+LAMBDA*Vds)*(Vgs-Vto-Vds/2)*Vds

Saturation Region: Vds>Vgs-Vto

Ids=KP/2 * W/L * (1+LAMBDA*Vds)*(Vgs-Vto)^2

Nonlinear Gate Drain capacitor

For Vgd<0:

$$Cgd = \left(\frac{\frac{Cgd\,min}{\pi/2} + Cgd\,max}{1+\pi/2} - \frac{Cgd\,min}{\pi/2} \right) * a\tan(A*Vgd) + \frac{Cgd\,min + Cgd\,max*\pi/2}{1+\pi/2}$$

For Vgd>0

$$Cgd = \left(Cgd\,max - \frac{Cdg\,min + Cgd\,max*\pi/2}{1+\pi/2} \right) * \tanh(A*Vgd) + \frac{Cgd\,min + Cgd\,max*\pi/2}{1+\pi/2}$$

Nonlinear Drain Source capacitor

$$Cds = Cjo * \left(1 + \frac{Vsd}{Vj} \right)^{-m}$$

Body diode

$$Vsd = Isd * Rb + N\frac{kT}{q}\ln\left(\frac{Isd}{Is} + 1 \right)$$

VDmos model parameters solved by the tool:

DC model parameters		AC model parameters		
Mosfet DC level 1	Body diode DC parameters	Nonlinear Cgd	Nonlinear Cds (Body diode)	Gate source capacitor
KP	Rb	Cgdmin	Cjo	Cgs
Vto	N	Cgdmax	m	
LAMBDA	Is	A	Vj	
Rs			TT	
Rd				
Rg				