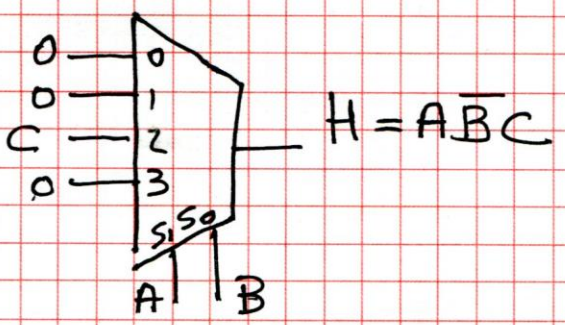
GRUPO B

1a) 0010 0000

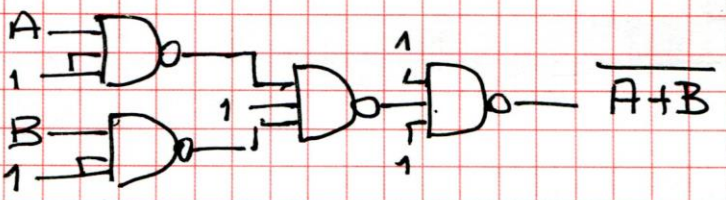
1b) 8ns

1c)



1d) FlipFlopT : Process (T, CLK)

1e) $A \text{ NOR } B = \overline{A+B} = \overline{\overline{A} \cdot \overline{B}}$



2) $f_{max} = \dfrac{1}{t_{pd\,CLK\to Q} + t_{setup} + t_{pd\,AND1}} = 20{,}4\,\text{OM}$

FlipFlopT.vhd

```
1
2   --Archivo FlipFlopT.vhd
3   --Sergio Noriega 2020
4   library ieee;
5   use ieee.std_logic_1164.all;
6
7   entity FlipFlopT is
8
9      Port ( T, CLK, RST    : in  std_logic;
10            Q, nQ           : out std_logic
11          );
12
13  end FlipFlopT;
14
15  architecture Comportamiento of FlipFlopT is
16
17  signal salidaQ, salidanQ : std_logic;
18
19      begin
20
21     FFT: process (T, CLK, RST)
22               begin
23               if (RST = '1') then
24                    salidaQ  <= '0';
25                 elsif (CLK'EVENT AND CLK = '0') then
26                    if (T='1') then salidaQ <= NOT salidaQ;
27                 end if;
28               end if;
29                    end process;
30
31     salidanQ <= NOT salidaQ;
32     Q  <= salidaQ;
33     nQ <= salidanQ;
34
35  end Comportamiento;
36
37
```