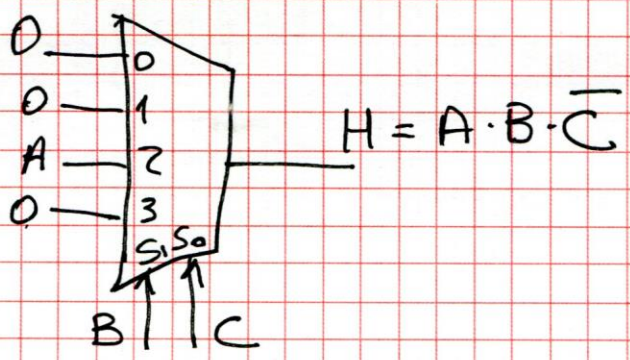
GRUPO C

1a) 1010 1000

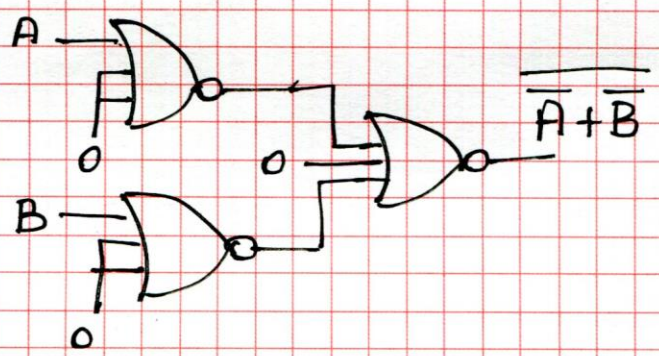
1b) SI

1c)



1d) FLIP-FLOP JK en VHDL

1e) A AND B $A \cdot B = \overline{\overline{A} + \overline{B}}$



1f) 15 ns

2) $f_{max} = \frac{1}{t_{pd\,CLK\to Q} + t_{setup} + t_{pd\,AND1}} = 20{,}4\,MHz$

FlipFlopJK.vhd

Compilation Report - Fl

```
1
2   --Archivo FlipFlopJK.vhd
3   --Sergio Noriega 2020
4   library ieee;
5   use ieee.std_logic_1164.all;
6
7   entity FlipFlopJK is
8   ||
9      Port ( J, K, CLK, RST   : in  std_logic;
10            Q, nQ            : out std_logic
11          );
12
13  end FlipFlopJK;
14
15  architecture Comportamiento of FlipFlopJK is
16
17  signal salidaQ, salidanQ : std_logic;
18
19      begin
20
21     FFJK: process (J, K, CLK, RST)
22              begin
23               if (RST = '1') then
24                              salidaQ  <= '0';
25                           elsif (CLK'EVENT AND CLK = '1') then
26                              if (J /= K) then salidaQ <= J;
27                           elsif (J='1' AND K='1') then salidaQ <= NOT salidaQ;
28                          end if;
29               end if;
30                    end process;
31
32     salidanQ <= NOT salidaQ;
33     Q  <= salidaQ;
34     nQ <= salidanQ;
35
36  end Comportamiento;
37
38
```