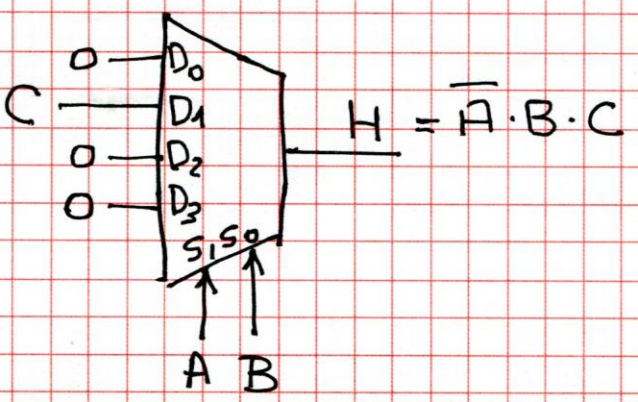
GRUPO A

1 a) 0110, 0100, 00001

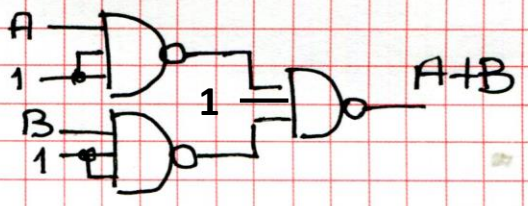
1 b) SI

1 c)



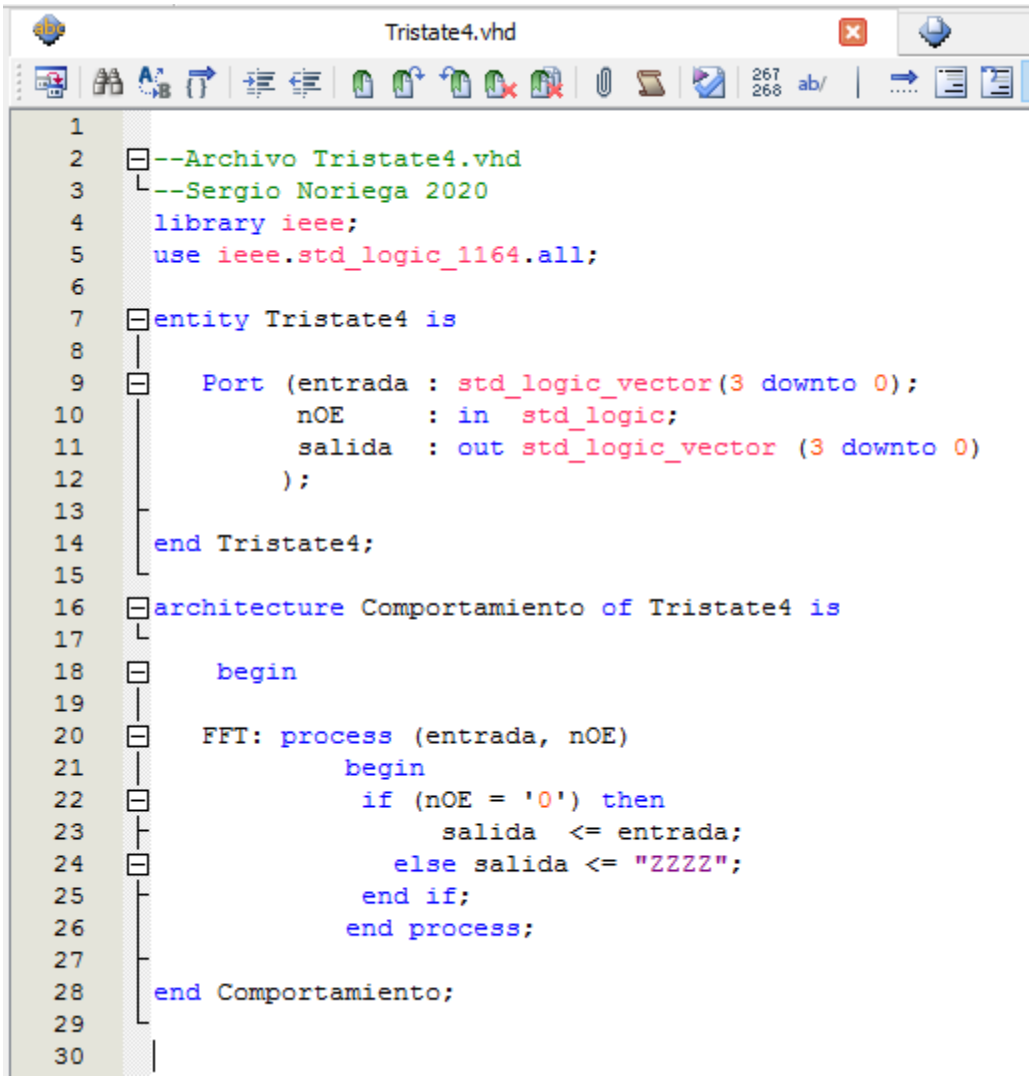
1 d) Tristate4 : Process (entrada, nOE)

1 e) $A+B = \overline{\overline{A} \cdot \overline{B}}$



1 f) 8ns.

2) $f_{max} = \frac{1}{t_{pd\,CLK \to Q} + t_{pd\,AND1} + t_{setup}} = 20{,}40\,MHz$


Tristate4.vhd
1
2 --Archivo Tristate4.vhd
3 --Sergio Noriega 2020
4 library ieee;
5 use ieee.std_logic_1164.all;
6
7 entity Tristate4 is
8
9 Port (entrada : std_logic_vector(3 downto 0);
10 nOE : in std_logic;
11 salida : out std_logic_vector (3 downto 0)
12);
13
14 end Tristate4;
15
16 architecture Comportamiento of Tristate4 is
17
18 begin
19
20 FFT: process (entrada, nOE)
21 begin
22 if (nOE = '0') then
23 salida <= entrada;
24 else salida <= "ZZZZ";
25 end if;
26 end process;
27
28 end Comportamiento;
29
30