									Page 1 (T	otal 4 pages)		
Shanghai University, Year 2012~2013, Spring Semester, Final Exam Paper A						Final Exa	m Pap	er A	2) Dynamic RAM It must be refreshed periodically. While it is being refreshed, the data cannot be accessed.			
Course Name: Microprocessors and Embedded Microcontrollers  Score						ntrollers		S				
THE OPTOCOSSOTS AND EMBOCATED THE TOTAL STATE OF THE STAT						itioners				3) The data bus and control buses are bidirectional.		
Course Code: <u>23325032</u> Credit: <u>6</u>							答案卷	<ul><li>4) All the ports upon RESET are configured as output ports.</li><li>5) The longer the cable, the higher the data transfer baud rate.</li></ul>				
应试人声明:									The longer the caole, the higher the data transfer badd rate.			
我保证	E遵守《」	上海大学学	学生手册》	中的《上	_海大学考	场规则》	,如有	考试进	<b></b> 超、作	3. In the 8051 addressing mode, the offset of the relative address is from128_ to _127		
弊行为,	愿意接受	《上海大	学学生考	试违纪、作	作弊行为界	定及处分	分规定》	》的纪	律处分。	3. In the 6031 addressing mode, the offset of the relative address is from126_ to _127		
Student N	lame			Studer	nt number					4. Which of the following instructions are legal? 1		
									•	1) MOV 25H, #25H 2) ADD R7, R4 4) MOVY A 20H		
		1				<u> </u>				3) MOV R9, #50H 4) MOVX A, 80H 5) ADDC A, #500 6) MOV @R3, #03H		
PROBLEN	1 1	2	3	4	5	6	7	8	9	0) NOV @R3, #0311		
Score										5. Suppose SP=0AH originally and internal RAM locations 09H and 0AH contain the values		
										30H and 01H respectively. After the instruction RETI is executed, the SP will be		
Notes to o										<u>08H</u> and PC will be <u>0130H</u> .		
-			examination	on paper u	sing pen o	r ball poi	nt pen	and ref	turn it at	6. Every 8051 family member wakes up at address0000H when it is powered up.		
the end of				41.:						o. Every 6031 family member wakes up at address when it is powered up.		
SFR	D7	D6	D5	this exam	D3	D2	I	D1	D0	7. In 8051 assembly programming, after adding packed BCD numbers, the result is no longer		
IE	EA	-	ET2	ES	ET1	EX1		ЕТО	EX0	BCD, therefore, the instruction <u>DA A</u> must be used after the addition of BCD		
IP	-	-	PT2	PS	PT1	PX1		то	PX0	operands.		
SCON	SM0	SM1	SM2	REN	TB8	RB8	,	TI	RI			
TCON	TF1	TR1	TF0	TR0	IE1	IT1	I	E0	IT0	8. If an 8051 is rate as 25MHz, which of the following frequency can be connected to the		
TMOD	GATE	C/T	M1	M0	GATE	C/T	N	M1	M0	microcontroller? 1,2 1) 15MHz 2) 25MHz		
										3) 35MHz 4) 50MHz		
Problem	1 (20 poin	its):								0. The havedesimal growther of the desired growther 2022 is 756. The 2's		
	_		stions. Car	ndidates sh	nould answ	er <b>ALL</b> ti	he ques	stions. (	2 marks	9. The hexadecimal number of the decimal number <b>2022</b> is The 2's complement of the hexadecimal number <b>4A</b> is 36H (00110110) .		
for each q	uestion)									complement of the nexadecimal number 4A is 5011 (00110110).		
<b>1</b> . If a m	icrocontro	oller is wi	th an 24-1	hit address	s hus ther	the data	a snace	which	ı can be	10. The decimal number -23 is represented by the assembler as <u>2</u> . The decimal number -128 is represented by the assembler as <u>5</u> .		
1. If a microcontroller is with an 24-bit address bus, then the data space which can be addressed by the computer is $2^{24}$ bytes, namely, $16$ megabytes?							-		1) 10001100 2) 11101001 3) 11100100			
addressed by the computer is 2 bytes, namely, 10 megabytes.					<u></u>	ao y tos :	•	4) 100010111 5) 10000000 6) 01111111				
1) 0 and		Ū			oout the 80 on the tele				2 onverted			

### Problem 2 (24 points):

Problem 2 contains six questions. Candidates should answer ALL questions. (4 marks for each question)

1) Assume accumulator A contains 56H. What are the results in accumulator A after the following instructions execute, respectively?

1) XRL A, 0FF

2) ANL A, 0FH

3) ORL A, 0FH

4) CPL A

Solution:

A9H

06H

5FH

A9H

(1 point each)

2) Assuming XTAL = 12MHz, indicate when the TF0 flag is raised for the following program.

MOV TMOD, #01 MOV TL0, #1BH MOV TH0, #FFH SETB TR0

Solution: FFFFH-FF1BH+1H=00E5H=229; T=1/f=1us; 229\*1us=229us

The TF0 flag is raised after 229us

3) Find the time delay for the delay subroutine shown to the right, if the system frequency is 12 MHZ.

DELAY: MOV R2, #100 AGAIN: MOV R3, #150

HERE: NOP

NOP

DJNZ R3, HERE DJNZ R2, AGAIN

RET

Answer:

$$T=12*1/f=1 \mu s$$

The delay time is 1+100\*(1+150\*4+2)+1=60302 machine cycles= $60302\mu$ s

4) For the instruction

#### LCALL LOC SUB

If SP=0AH initially and the label "LOC\_SUB" is at program memory location 0300H, after executing the instruction at location 0102H, what values are in the SP, PC, and internal RAM locations 0BH and 0CH.

Solution: SP = 0CH, PC = 0300H,

(0BH) = 05H, (0CH) = 01H (1 point each)

5) Write down the priority of the six interrupts in 8051 after the instruction **MOV IP**, #00001010B is run.

Solution: RST T0 T1 INT0 INT1 Serial

6). Find the CY and AC flags for each of the following.

(e) MOV A, #0EFH

SETB C

(f) CLR C

ADDC A, #0

ADDC A, #17

MOV A, #0FEH

ADDC A, #0

Solution:

(e) CY: 0 AC: 1 (f) CY: 0 AC: 1

## Problem 3 (6 points)

Find the result at points (1), (2), and (3) in the following code?

CJNE A, #AAH, COMP

.. ;point (1)

COMP: JNC NEXT

;point (2)

NEXT: ... ;point (3)

Solution:

Point(1) A = #AAH

Point(2) A < #AAH

Point(3) A > #AAH

#### Page 3 (Total 4 pages)

### **Problem 4 (15 points)**

The following program is used to add the augend 55 and 66 in RAM locations 40H and 41H with the addend 66 and 88 in RAM locations 50H and 51H, and then store the sum of the addition into RAM locations 50H. 51H and 52H. Fill in the following blanks. (1 point for each blank in the code, 0.5 point for each blank in the results)

Source c	code	Address	The results
ORG	0000Н		The first cycle The second cycle
START:MOV	R0,#40H	H0000	(R0) = 40H
MOV	R1,#50H	0002H	(R1) = 50H
MOV	R2,#2	0004H	(R2) = 02H
<u>CLR</u>	C	0006H	(CY)= 0
LOOP: MOV	A,@R0	0007H	$(ACC)= 55H \qquad (ACC)=66H$
<u>ADDC</u>	A,@R1	0008H	(ACC)=BBH (ACC)=EFH
DA	<u>A</u>	0009H	$(ACC) = 21H \qquad (ACC) = 55H$
MOV	@R1,A	000AH	((R1))= 21H $((R1))=55H$
INC	R0	000BH	(R0) = 41H $(R0) = 42H$
INC	R1	000CH	(R1)= 51H $(R1)=$ 52H
DJNZ	R2, <u>LOOP</u>	000DH	(R2) = 01H $(R2) = 00H$
CLR	A	000FH	(ACC) = 00H
ADDC	A,#0	0010H	$(ACC) = 01H \qquad (CY) = 1$
MOV	@R1,A	0012H	((R1)) = 01H
NOP			
END			

# Problem 5 (6 points)

Assuming XTAL = 12 MHz, write a 8051 program to generate a square wave on pin P1.3 using timer 0 in mode 2.

ORG 0000H

MAIN: MOV SP, #60H

**MOV TMOD**, <u>#02H</u> (0.5point)

MOV TL0, #E7H MOV TH0, #E7H

LOOP: SETB <u>TR0</u> (0.5point)

LOOP1: JNB TF0, LOOP1	(1point)
CLR TR0	
<u>CPL</u> P1.3	(0.5point)
CLR <u>TF0</u>	(0.5point)
SJMP <u>LOOP</u>	(0.5point)
<b>END</b>	(0.5point)

The frequency of the square wave is: (2 points)

$$N = 25$$
,  $f = 1/(50us) = 20KHz$ 

### Problem 6 (5 points)

Program timer 1 to be an event counter. Set the initial count to 10. Use mode 1 and display the binary count on P1 and P2 continuously until the count reaches 0000H.

	MOV	TMOD, <u>#50H</u>	(1point)
	MOV	TH1, <u>00H</u>	(0.5point)
	MOV	TL1, <u>0AH</u>	(0.5point)
	SETB	<u>TR1</u>	(1point)
LOOP:	MOV	A, TL1	
	MOV	P1, A	
	MOV	A, TH1	
	MOV	P2, A	
	<u>JNB</u>	TF1, LOOP	(1point)
	CLR	<u>TR1</u>	(0.5point)
	CLR	TF1	
	END	_	(0.5point)

# Problem 7 (4 points)

Calculate the total number of bits transferred if 100 pages of ASCII data are sent using asynchronous serial data transfer. Assume a data size of 8 bits, 1 stop bit, no parity. Assume each page has  $48 \times 20$  of text characters. How long will the data transfer take if the baud rate

is 9600?

Solution:

100\*48\*20\*(8+2)=960000 bits (2 points)

T = 960000/9600 = 100s (2 points)

#### Page 4 (Total 4 pages)

#### Problem 8 (10 points)

The following program is written for the 8051 to get data from P1 and send it to P2 continuously while incoming data from the serial port is send to P0. Assume crystal frequency to be 11.0592MHz and SMOD = 1. Set the baud rate at 4800. Calculate the initial value in TH1. Fill in the following blanks. (Hint: SMOD = 0, baud rate at 9600, then TH1 = FD).

	ORG LJMP ORG LJMP	<u> </u>	1 point 1 point
MAIN:	ORG MOV MOV MOV MOV	TH1 <u>, #0F4H</u>	0.5 point 0.5 point 0.5 point
	SETB MOV SJMP	P2, P1 HERE	0.5 point 0.5 point
	MOV CLR RETI	TRANS P0, SBUF RI	0.5 point 0.5 point 0.5 point
TRANS:	CLR RETI END	<u>TI</u>	0.5 point 0.5 point

The initial value in TH1 should be: (3 points)

TH1 = -12 = F4H

### Problem 9 (10 points):

Answer the following questions:

- (1) In the 8051 which port provides the A0 A7 address bits? (1 points)
- (2) In the 8051 which port provides the A8 A15 address bits? (1 points)
- (3) In the 8051 which port provides the D0 D7 data bits? (1 points)
- (4) Which signal must be used in fetching data from external RAM? (a) RD (b) WR (c) PSEN (1 points)

(5) Write a program to transfer 100 bytes of data from external data ROM to external data RAM. The external data ROM address is 3000H, and the external data RAM starts at 8000H. (Hint: the address of DPL is 82H) (6 points)

#### Solution:

- (1) P0 provides the A0 A7 address bits.
- (2) P2 provides the A8 A15 address bits.
- (3) provides the D0 D7 data bits.
- (4) It's RD

(5)

ORG 0000H

MOV R0, #00H

LOOP: MOV DPH, #30H

MOV 82H, R0; the address of DPL is 82H

CLR A

MOVX A, @DPTR MOV DPH, #80H MOVX @DPTR, A

INC R0

CJNE R0, #100, LOOP

**END**