Assignment 2

Chapter 2

4. Name a 16-bit register in the 8051.

Answer: PC and DPTR

7. Which of the following is (are) illegal?
(a) MOV R3,#500 (b) MOV R1, #50 (c) MOV R7, #00
(d) MOV A, #255H (e) MOV A, #50H (f) MOV A, #F5H
(g) MOV R9, #50H

Answer: (a) (d) (f) (g)
Note:
(a) MOV R3,#XXH or MOV DPTR,#XXXXH (X=0~F)
(d) MOV A, #XXH (X=0~F)
(g) MOV Rn, #50H (n=0~7)

8. Which of the following is (are) illegal?
(a) ADD R3, #50H (b) ADD A, #50H (c) ADD R7, R4
(d) ADD A, #255H (e) ADD A, R5 (f) ADD A, #F5H
(g) ADD R3, A

Answer: (a) (c) (d) (f) (g)

Note:
(a) ADD A, #50H
(c) ADD A, R4
(d) ADD A, #XXH (X=0~F)
(g) ADD A, R3

18. Do the ORG and END directives produce opcodes?

Answer: ORG and END directives don't produce opcodes.

21. Every 8051 family member wakes up at address 0000H when it is powered up.

Answer: 0000H

30. Compile and state the contents of each ROM location for the following data.

```
ORG 340H
DAT_1: DB  22, 56H, 10011001B, 32, 0F6H, 11111011B
```

Answer:

$(22)_{10}$ =16H	(340H)=16H
56H	(341H)=56H
10011001B=99H	(342H)=99H
$(32)_{10}$ =20H	(343H)=20H
0F6H	(344H)=0F6H
11111011B=0FBH	(345H)=0FBH

34. In the ADD instruction, when is CY raised?

Answer: When there is a carry out from D7 bit after ADD instruction is performed, the bit CY in the special function register PSW is raised.

35. In the ADD instruction, when is AC raised?

Answer: When there is a carry out from D3 to D4 during an ADD instruction operation, the bit CY in the special function register PSW is raised.

40. On power up, what is the location of the first stack?

Answer: When powered up, the first stack is 08H.

41. In the 8051, which register bank conflicts with the stack?

Answer: In the 8051, the register bank 1 is in conflict with the stack

45. Assuming the use of bank 0, find at what RAM location each of the following lines stored the data.
(a) MOV R4, #32H (c) MOV R7, #3FH

Answer:

	address	data
(a) MOV R4, #32H	0000,0100 (or 04H)	0011,0010 (or 32H)
(c) MOV R7, #3FH	0000,0111 (or 07H)	0011,1111 (or 3FH)

48. Show the stack and stack pointer for each line of the following program.

Answer: SP=07H, default stack pointer

```
ORG 0
MOV R0, #66H
MOV R3, #7FH
MOV R7, #5DH
PUSH 0      ;SP=08H, stack [08H] = #66H
PUSH 3      ;SP=09H, stack [08H] = #66H, [09H] = #7FH
PUSH 7      ;SP=0AH, stack [08H] = #66H, [09H] = #7FH, [0AH] = #5DH
CLR A
```

```
MOV R3, A
MOV R7, A
POP 3          ;SP=09H, stack [08H] = #66H, [09H] = #7FH,
POP 7          ;SP=08H, stack [08H] = #66H
POP 0          ;SP=07H, empty stack
```

49. In problem 48, does the sequence of POP instructions restore the original values of registers R0, R3, and R7? If not, show the correct sequence of instructions.

Answer:

(1) No, after the sequence of POP, the value of R0 remains the original value, but the values of R3 and R7 changed as follows:
R0 = #66H R3 = 5DH R7 = 7FH

(2) The correct sequence of POP instructions are as followings:

```
POP 7
POP 3
POP 0
```

Chapter 5

9. Which registers are allowed to be used for register indirect addressing mode when accessing data in RAM?

Answer: The registers R0 and R1 can be used for register indirect addressing mode when accessing data in RAM.

11. Write a program to copy 10 bytes of data starting at ROM address 400H to RAM locations starting at 30H.

Answer:

```
        ORG 0000H
        MOV DPTR, #0400H
        MOV R0, #30H
        MOV R1, #0AH
LOOP:   CLR A
        MOVC A, @A+DPTR
        MOV @R0, A
        INC R0
        INC DPTR
        DJNZ R1, LOOP
        END
```

Chapter 14

10. Which of the following, EPROM, DRAM, and SRAM, must be refreshed periodically?
Answer: DRAM must be refreshed periodically.

30. True or false. For any member of the 8051 family, if EA=Gnd it fetches program code form external ROM.

Answer: True

34. In the 8051 which port provides the A0 – A7 address bits?

Answer: P0 provides the A0 – A7 address bits.

35. In the 8051 which port provides the A8 – A15 address bits?

Answer: P2 provides the A8 – A15 address bits.

36. In the 8051 which port provides the D0 – D7 data bits?

Answer: P0 provides the D0 – D7 data bits.

39. Which of the following signals must be used in fetching program code from external ROM?
(a) RD (b) WR (c) PSEN

Answer: It's PSEN

52. Write a program to transfer 100 bytes of data from external data ROM to external data RAM. The external data ROM address is 3000H, and the external data RAM starts at 8000H.

Answer: (Solution 1)

```
        ORG 0000H
        MOV R0, #00H                ; CLR R0 is wrong
LOOP:   MOV DPH, #30H
        MOV 82H, R0                 ; the address of DPL is 82H
        CLR A
        MOVX A, @DPTR
        MOV DPH, #80H
        MOVX @DPTR, A
        INC R0
        CJNE R0, #100, LOOP
```

```
        END
```

(Solution 2)

```
        ORG 0000H
        MOV DPTR 3000H
        MOV R1, #100
        MOV R0, #00H
LOOP:   MOVX A, @DPTR
        MOV P2, #80H
        MOVX @R0, A
        INC R0
        INC DPTR
        DJNZ R1, LOOP
        END
```