Assignment 3

Chapter 3

3. In calculating the target address for a jump, a displacement is added to the contents of register PC .

4. The mnemonic SJMP stands for short jump and it is a 2 -byte instruction.

5. The mnemonic LJMP stands for long jump and it is a 3 -byte instruction.

7. True or false. The target of a short jump is within -128 to +127 bytes of the current PC.

Answer: True

14. Find the number of times the following loop is performed.

```
        MOV R6, #200
BACK:   MOV R5, #100
HERE:   DJNZ R5, HERE
        DJNZ R6, BACK
```

Answer:

LOOP "HERE": 20000 times
LOOP "BACK": 200 times

20. The LCALL target address is limited to 64K bytes form the present PC.

25. Show the stack for the following code.

```
000B    120300          LCALL DELAY
000E    80F0            SJMP BACK
0010
                ; This is the delay subroutine
0300                    ORG 300H
0300            DELAY:
0300                    MOV R5, #0FFH
0302    DDFE    AGAIN:  DJNZ R5, AGAIN
0304    22              RET
```

Answer:

Before LCALL the stack is assumed to point to X

LCALL to RET the stack is: 00
0E
X

After RET the stack is back to X

35. Find the time delay for the delay subroutine shown to the right, if the system frequency is 16 MHZ.

```
DELAY:  MOV   R2, #150
AGAIN:  MOV   R3, #250
HERE:   NOP
        NOP
        NOP
        DJNZ  R3, HERE
        DJNZ  R2, AGAIN
        RET
```

Answer:

T=12*1/f=0.75μs

1+150*(1+250*5+2)+1=187952 machine cycles=140964μs

Chapter 6

1. Find the CY and AC flags for each of the following.

(e)
```
MOV A, #0FEH
SETB C
ADDC A, #01
```

(f)
```
CLR C
MOV A, #0FFH
ADDC A, #01
ADDC A, #0
```

Answer:

(e) CY: 1
AC: 1

(f) CY: 0
AC: 0

3. Write a program to add the following numbers and save the result in R2, R3. The data is stored in on-chip ROM.

```
        ORG 250H
MYDATA: DB 53, 94, 56, 92, 74, 65, 43, 23, 83
```

Answer:

```
        MOV   R2, #00
        MOV   R3, #00
        MOV   R1, #09
        MOV   DPTR, #MYDATA
        CLR   C
LOOP:   CLR   A
```

```
MOVC    A, @A+DPTR
ADD     A, R2
DA      A
MOV     R2, A
MOV     A, R3
ADDC    A, #00
DA      A
MOV     R3, A
INC     DPTR
DJNZ    R1, LOOP
```

8. True or false. The “DA A” instruction works on register A and it must be used after the ADD and ADDC instructions.

Answer: True

16. Show how the following are represented by the assembler.
(a) -23 (b) +12 (c) -28
(d) +6FH (e) -128 (f)+127

Answer:
(a) 11101001
(b) 00001100
(c) 11100100
(d) 01101111
(e) 10000000
(f) 01111111

Chapter 7

1. Assume that these registers contain the following: A=F0, B=56, and R1=90. Perform the following operations. Indicate the result and the register where it is stored.
Note: The operations are independent of each other.
(a) ANL A, #45H (b) ORL A, B
(c) XRL A, #76H (g) ANL A, #0FFH
(j) XRL A, #0AAH

Answer:
(a) A=40H

F0H	11110000
45H	01000101
40H	01000000

(b) A=F6H

F0H 11110000
56H 01010110
F6H 11110110

(c) A=86H
F0H 11110000
76H 01110110
86H 10000110

(d) A=F0H
F0H 11110000
FFH 11111111
F0H 11110000

(e) A=5AH
F0H 11110000
AAH 10101010
5AH 01011010

6. Indicate the status of CY after CJNE is executed in each of the following cases.

(f) MOV R3, #0AAH
ANL R3, #55H
CJNE R3, #00, NEXT

Answer: CY is unchanged.

8. Find register A contents after each of the following is executed.

(d) SETB C
MOV A, #7AH
SWAP A
RLC A
RLC A

Answer:
A=9FH

17. Find the result at points (1), (2), and (3) in the following code?

```
        CJNE A, #50, NOT_EQU
        …                   ;point (1)
NOT_EQU: JC NEXT
        …                   ;point (2)
NEXT:     …                     ;point (3)
```

Answer:
Point(1) A = #50
Point(2) A > #50

Point(3) A < #50

Chapter 8

1. “SETB A” is a(n) invalid (valid, invalid) instruction.

2. “CLR A” is a(n) valid (valid, invalid) instruction.

3. “CPL A” is a(n) valid (valid, invalid) instruction.

7. Write a program to generate a square wave with 75% duty cycle on bit P1.5.

Answer:

```
Loop:  SETB    P1.5
       LCALL   Delay
       LCALL   Delay
       LCALL   Delay
       CLR     P1.5
       LCALL   Delay
       SJMP    Loop
Delay:  .......
```

37. Write instructions to save the CY flag bit in bit location 4.

Answer:

```
MOV  4, C
```