EE2A

Integrated Mechatronic Project Wire-Following Signal Generator

1.0 Aims

(i) To interface a 12-bit digital-to-analogue converter to an 18F27K40 processors using an SPI interface.

(ii) To generate a hardware-controlled latch signal to synchronise the digital-to-analogue converter using a PWM timer device.

(iii) To use the Pulse Width Modulated (PWM) hardware-controlled latch signal to generate an interrupt function. This function will output the next value to the digital-to-analogue converter.

(iv) To use Matlab to generate look-up table values and corresponding C statements.

(v) To switch between 1 kHz, 2 kHz and summed output signals implemented using look-up tables to provide Direct Digital Synthesis (DDS) functionality.

(vi) To demonstrate the concepts of offset binary notation used by many digital-to-analogue converters.

This experiment is designed to allow students to familiarise themselves with counter-timer circuits, Pulse Width Modulated (PWM) units, interrupts. Digital-to-analogue converters, SPI interfaces, look-up tables and Matlab-generated C statements.

2.0 Learning Outcomes

Deliverables:

i) A demonstration of a 1 kHz, 2 kHz and combined analogue signal output.

ii) Well-structured and -commented PIC programs that deliver the specification stages given in Section 3.1.

iii) A log book containing any preparatory work undertaken outside the lab, design decisions, test procedures and a discussion of the issues involved.

iv) Ability to generate your own mark scheme and rigorous evaluation procedures (can you pre-empt a cynical boss?).

What will be assessed:

i) The program source code, with particular emphasis on adequate comments, program layout and elegance.

ii) A practical demonstration.

iii) The adequacy of the log book (lab books not written up during the experiment will incur penalty marks).

3.0 Activities

3.1 Specification

This laboratory experiments has a single overall aim – to design and build a test signal generator for your integrated mechatronic project vehicle. Many new skills will need to be learnt and these are best acquired by breaking the problem down into small components.

3.1.0 Demonstrate a digital-to-analogue converter latch signal

The data transmitted to the digital-to-analogue converter is latched on an active-low signal applied to the LDAC input of the MCP4821 device. Use the Pulse Width Modulated (PWM) capabilities of the PIC18F27K40 to generate a signal at a rate of 32 kHz with a low-duration of 1 μs.

3.1.1 Demonstrate an interrupt routine access

The PWM signal may be used to trigger an interrupt. Write a very simple interrupt routine to place an IO pin of your choice high and then low. Use a two-channel oscilloscope triggered off the PWM (LDAC) signal to examine this IO pin. You are attempting to access the interrupt routine immediately after the PWM (LDAC) signal.

3.1.2 Demonstrate the use of programmable peripheral programming pins

The PIC 18F27K40 has the ability to map the peripheral such as the SPI interface to many, but not all, of the IO pins. Learn how to map the SPI peripheral to the pins defined by your circuit diagram to your program.

3.1.3 Demonstrate an SPI signal to the digital-to-analogue converter

Add two SPI writes within the interrupt routine to output a 16-bit constant. You will also need to include the Chip Select (CS) control signal. Use the two channels of the oscilloscope to confirm the SDI, SCK and CS signals agree with the MCP4821 data sheet.

3.1.4 Matlab code to generate sine wave look-up tables

Write a Matlab script to generate three look-up tables corresponding to a 1 kHz, 2 kHz and 1 kHz+ 2 kHz combined signal. Cut-and-paste the look up tables into the main C code. The format of the data should be in offset binary and confined to the range 0x000 to 0xFFF. Incorporate tests to ensure that the data does not exceed the range of the digital-to-analogue converter. Assume that the sampling rate is 32 kHz.

3.1.5 Total System Demonstration

Use switches to select between the three look-up tables and view the generated signals on an oscilloscope.

That's it – now do it!

3.1.6 Expected results

I obtained the following results, which may be useful as benchmarks. The sampling frequency was 32 kHz. The 'Vout' signal is illustrated on Channel 1 at 1 V/div and the 'LDAC' signal is illustrated on Channel 2 at 2 V/div.

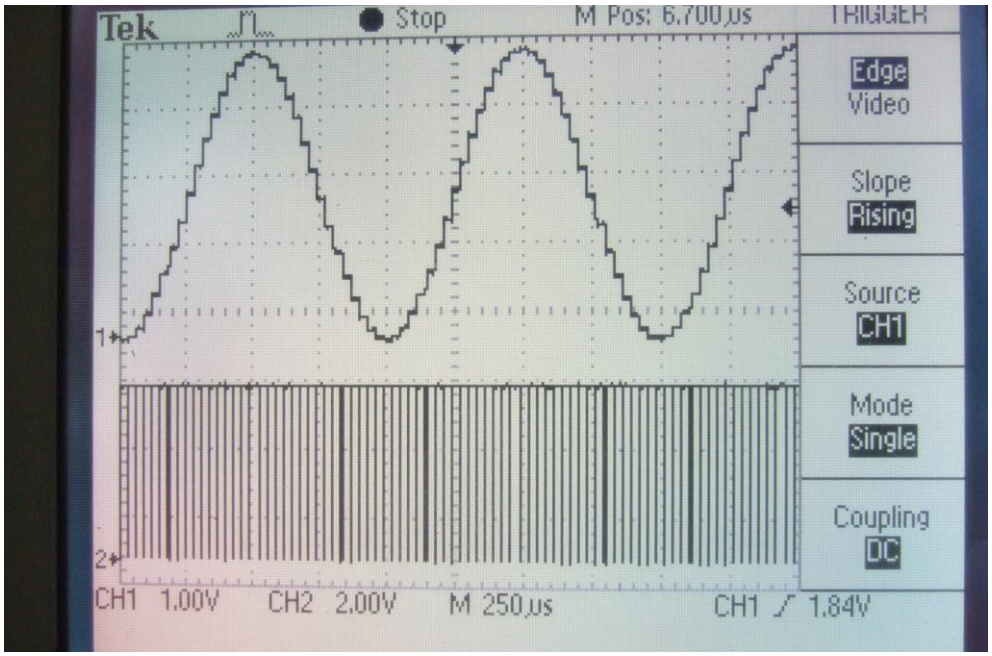


Figure 1. Typical result for 1 kHz signal. Channel 1 represents the Vout signal, Channel 2 represents the LDAC signal.

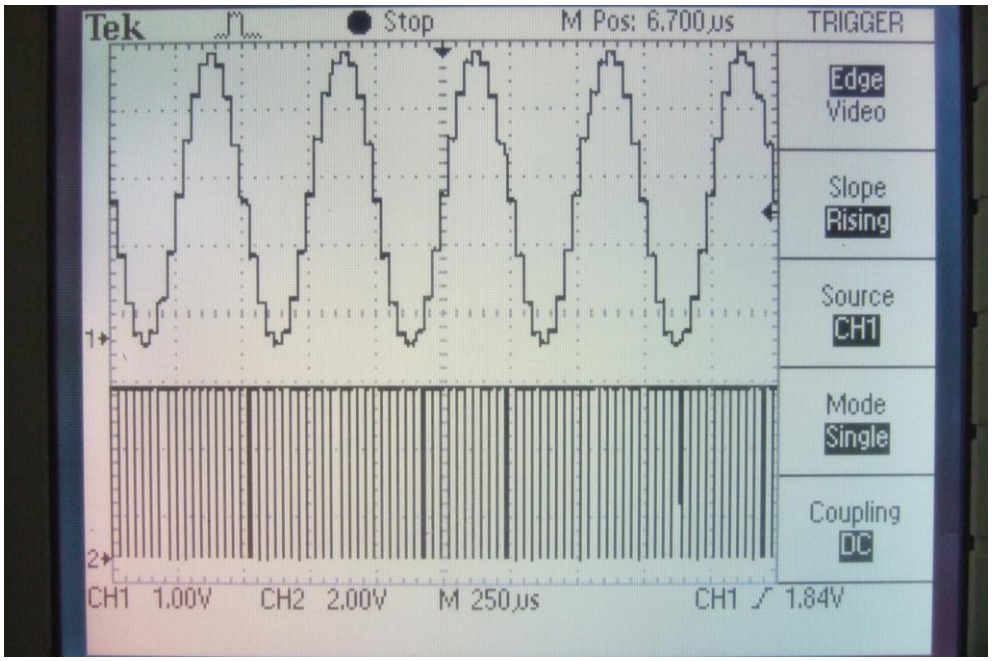


Figure 2. Typical result for 2 kHz signal. Channel 1 represents the Vout signal, Channel 2 represents the LDAC signal.

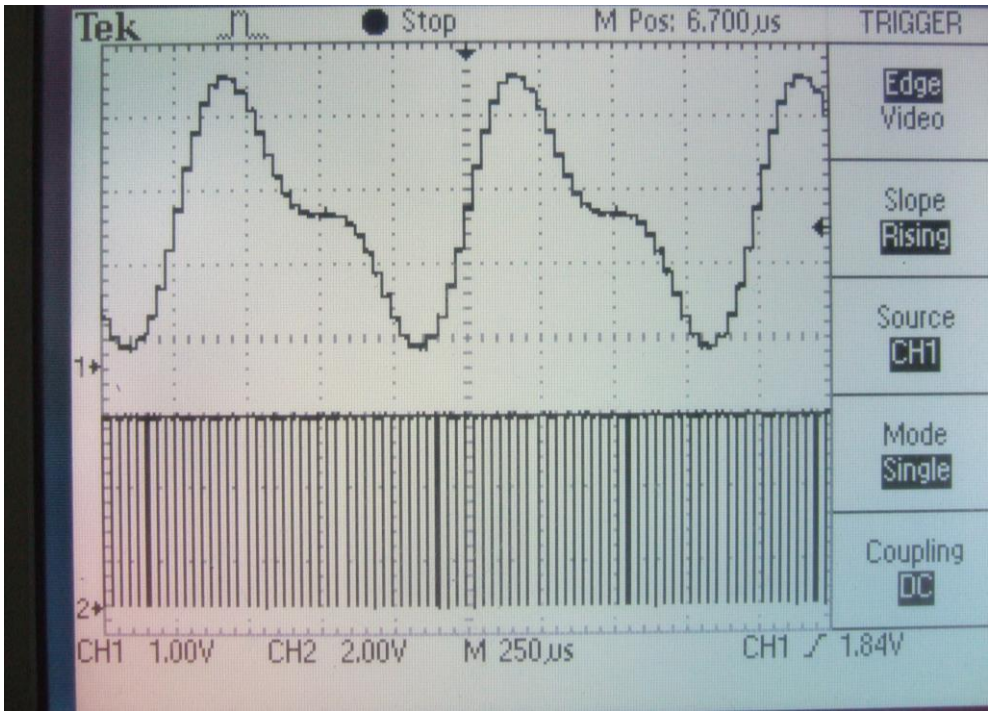


Figure 3. Typical result for 1 kHz and 2 kHz combined signal. Channel 1 represents the Vout signal, Channel 2 represents the LDAC signal.

4.1 Preparatory Work

The following sections aim to guide you through some of the design processes.

4.1.1 Hardware

It is suggested that you connect the MCP4821 to the spare signals (RA4..5, RA7 and RB4..5) not used in the previous experiment. You may wish to add a resistor-capacitor low-pass filter to the output of the digital-to-analogue converter. The resistor value should be chosen such that not more than 10 mA flows when the output is effectively short-circuited by the tracking wire.

PW1. Draw a complete schematic circuit diagram of the PIC 18F27K40, programmer and the interface components. This will be the circuit diagram that you will wire up within the laboratory. All power supply connections, LEDs, resistors, decoupling capacitors and switches should be clearly labelled.

Checklist to Obtain a 'W' during Demonstration

Switch Code	Comment	Seen
00	Demonstrate that a 1 kHz signal is output on pin 8 of the MCP4821. No clipping or non-linear distortion should be present.	
01	Demonstrate that a 2 kHz signal is output on pin 8 of the MCP4821. No clipping or non-linear distortion should be present.	
10	Demonstrate that a combined 1 kHz + 2 kHz signal is output on pin 8 of the MCP4821. No clipping or non-linear distortion should be present.	

Technical Information Notes

TN1. MCP4821 Digital-to-Analogue Converter

The MCP4821 Digital-to-Analogue Converter is a 12-bit device powered from a single +5V supply and containing an internal 2.048 V voltage reference. This pin layout for this device is shown in Figure TN1.1. Pin 1 is a power supply pin and should be connected +5V, whilst the 0V supply is connected to Pin 7. The SPI digital interface is implemented using three pins; Chip Select (CS) connected to Pin 2, Serial Clock (SCK) connected to Pin 3 and Serial Data In (SDI) connected to Pin 4. A Latch signal (LDAC) is connected to Pin 5 to define when the output voltage should be updated. The device should be permanently activated by connecting the Shutdown (SHDN) signal on Pin 6 to +5V. Finally, the analogue output signal appears on Pin 8.

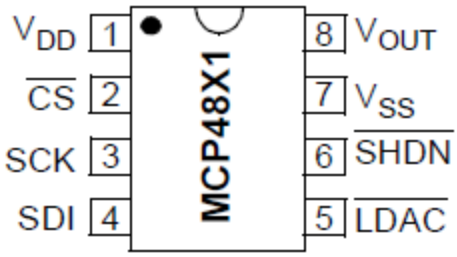


Figure TN1.1: MCP4821 Pin Layout

Engineers need to know about the internal structures of devices and this is shown for the MCP4821 in Figure TN1.2. This diagram shows that internal power-on reset circuitry is included and that an output voltage gain control is present.

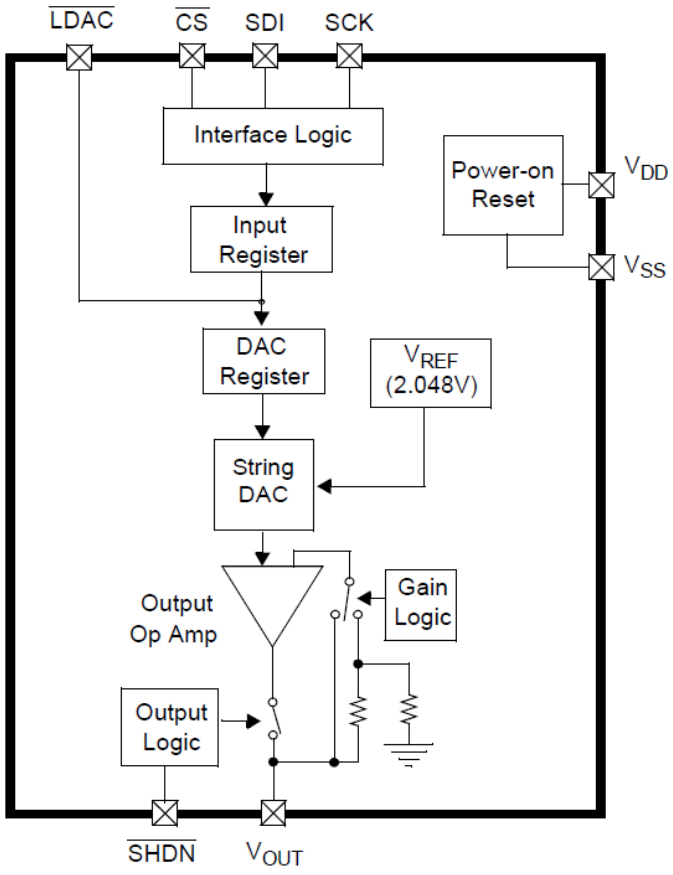


Figure TN1.2: Internal Structure of MCP4821

The data transmitted from the microcontroller to the MCP4821 must be transmitted in the format shown in Figure TN1.3. Twelve bits of data corresponding of an offset-binary format is transmitted in the least significant bits of the word. The Shutdown signal is replicated in thirteenth bit – this would normally be set high. Finally, the output gain stage is controlled by fourteenth bit (also normally set high).

REGISTER 5-1: WRITE COMMAND REGISTER FOR MCP4821 (12-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
0	—	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15															bit 0

Figure TN1.3: Format of data word required by MCP4821

The data word is transmitted in big-endian format (most significant bit first) as shown in Figure TN1.4.

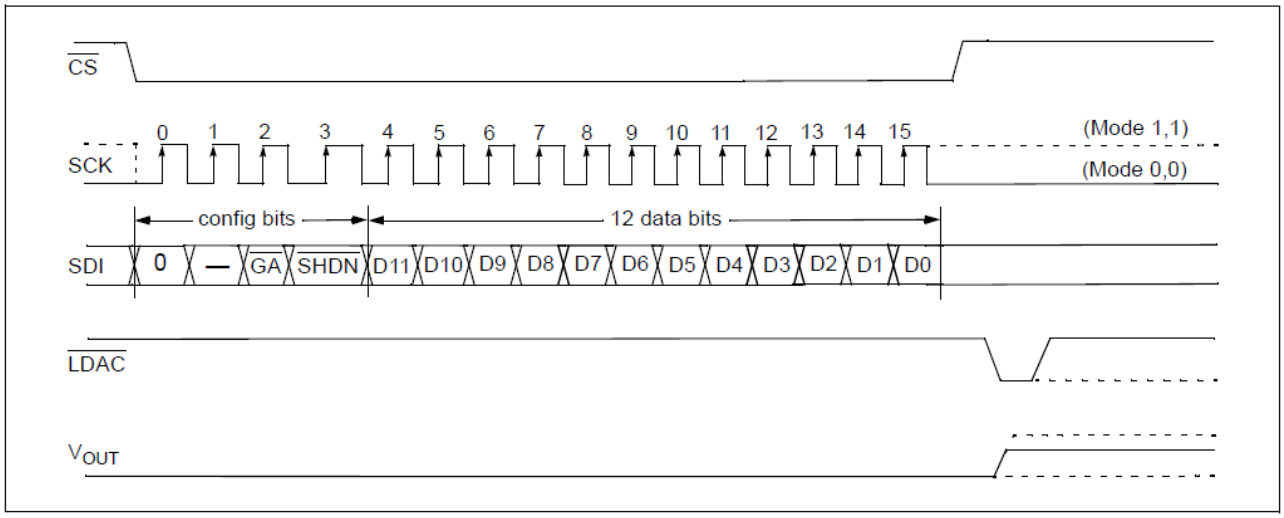
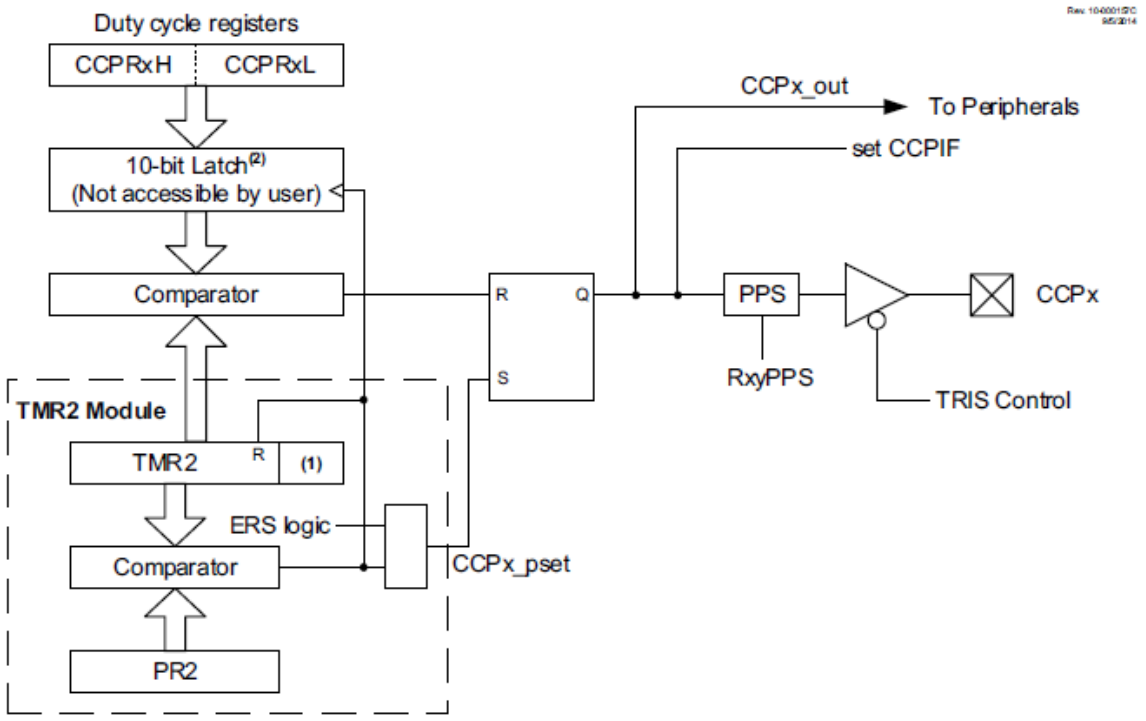


Figure TN1.4: Schematic timing diagram of data word required by MCP4821

TN2. Pulse Width Modulator and Timers

A 1 µs active-low LDAC signal is required at a 32 kHz sampling rate. Typically, a Capture Compare Module (CCP) is used in conjunction with a PWM module. It is suggested that you consider using Timer 2 coupled with CCP4 to drive PWM4.

The block diagram of the pulse width modulator is shown in Figure TN2.1. Timer 2 is used to increment at a rate determined by the main system clock. Timer 2 would normally consist of an 8-bit counter, but in this case an extra two bits are added from an internal pre-scaler. This 10-bit counter is compared to a register (CCPR4) holding a constant value.



Notes: 1. 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.
2. The alignment of the 10 bits from the CCPR register is determined by the FMT bit.

Figure TN2.1: Block diagram of a PWM unit

The pulse width modulated period is specified by the PR2 register of Timer 2. The period may be calculated by the following equation:

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC

First, remember that the PR2 register is 8-bits. Thus the best resolution is obtained when the value in PR2 is as large as possible (nearest to 255). So start off with a high system clock frequency such as 32 MHz and calculate the division ratio required to obtain a 32 kHz sampling rate. Remember that the PIC divides the main system clock by a factor of four, so you might get away with a value of one for the pre-scaler and 250 for [(PR2) + 1]

You will need to use the command:

```
setup_timer_2(….);
```

Next, a suitable value must be entered into the CCPR4 register. This value is determined by calculating the period equivalent to a 32 kHz sampling rate and using this as an absolute maximum value.

$$Pulse\ Width = (CCPRxH{:}CCPRxL\ register\ pair) \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

The command required to set the CCPR2 register is:

```
set_pwm4_duty(….);
```

If the output is permanently high, you value of pulse width is probably too large. Try reducing it to one and see if you obtain a short, active-high pulse.

Somewhere near the start of your main program and before and of the above register settings, you need to define resource usage by commands such as:

```
setup_ccp2(CCP_PWM|CCP_USE_TIMER1_AND_TIMER2);  // Configure CCP2 as a PWM,
// CCP2 is paired with Timer 2
setup_pwm4(PWM_ENABLED|PWM_ACTIVE_HIGH|PWM_TIMER2);
```

Name:

EE2A Experiment 3

Wire Following Signal Generator

Feedback Mark Sheet – Paste into the logbook

The following will be assessed during the laboratory session (PGTA to circle, date and sign)

Circuit construction and demonstration:	Yes	Partially	No
Demonstration of 1 kHz, 2 kHz and combined direct digital synthesis signal generator (35%)	**W**	**WP**	**NW**

Inspection Mark For Log Book:	Could not be better	Good attempt	Room for improvement	Appalling
A 'flick-test' of the log book will be carried out. This will be based on the purpose of the log book – to convey useful information to other engineers and to allow others to carry on with the work.	**4**	**3**	**2**	**1**

At the end of the year, the log-book will be handed in and assessed using the following criteria:

Preparatory Work:
Evidence of adequate preparatory work undertaken outside laboratory (15%). Students to have decided what is 'adequate' as part of their work.
Source Code:
Existence and completeness of the program header (author, date, filename, target device, fuse settings, program function) (5%). Appropriateness and clarity of comments, labels and variable/constant definitions (5%). Efficient use of code (i.e. no redundancy) (5%). Program Elegance (5%). Technical content (10%). Code print-outs are assumed.
Reflective journal:
Care and neatness of preparatory work (written up outside lab) (5%). Sensible attempt at keeping a log-book (written up at the time) to convey engineering information to other professionals. (10%). If this student was a professional engineer who left his/her organization today, could another engineer pick up the pieces in six months time? Conclusions- sensible executive summary & record of the learning experiences gained by the student during this experiment. (5%).

Verbal feedback will be provided during the laboratory.

Timeliness (Autumn Term)

Week in which experiment was demonstrated to supervisor (shaded blocks show overrun)

Week 4	Week 5	Week 6	Week 8	Week 9	Week 10	Week 11
	Excellent Progress	Excellent Progress	Excellent Progress	Excellent Progress	Excellent Progress	Good Progress