EE2A

Laboratory Experiment 1

Discrete Logic Synchronous Finite State Machine

2017-2018

1.0 Aims

(i) To design, build and test a synchronous finite state machine using discrete logic that steps through states in a pre-defined order.

(ii) To build and then to fault-find the most complicated discrete component circuit encountered during the second year.

(iii) To generate effective documentation that a junior engineer working for you could follow with ease.

The techniques developed for methodically building and fault finding this discrete-component finite state machine will provide an invaluable insight into the problems encountered in many large-scale electronic systems. For this reason, no student will be permitted to continue with the rest of the laboratory course until a working finite state machine has been demonstrated to the laboratory supervisor. An average student will be able to demonstrate a working finite state machine after two laboratory sessions.

2.0 Specification

A synchronous finite state machine is to be designed, built and demonstrated which will give one output pulse equal in length to a clock cycle, after a pre-defined number of clock transitions. The finite state machine should contain four secondary state variables and be designed to count cyclically through a **pre-defined** series of states corresponding to standard binary notation whilst skipping unallocated states (e.g. for Group 1: S11, S12, S8, S15, S10, S3, S13, etc. = {1011, 1100, 1000, 1111, 1010, 0011, 1101} etc.). The finite state machine is to re-synchronise within one clock pulse should the system enter an unallocated state at switch-on time. **The state into which the finite state machine re-synchronises should be chosen to minimise the complexity of the circuitry.** In order to test the finite state machine, it is necessary to include a means of loading states into the finite state machine (usually via the set and reset inputs on the flip-flops). The machine will contain output combinational logic to generate a single *Z* output – thus a total of five signals will be demonstrated (4 SSVs, 1 Z Output).

Any number of 74xxx devices may be used, but the choice will be limited to 74x00, 74x04, 74x10, 74x20, 74x30 combinational logic and 74x74 D-type flip flops.

The specification for each of the laboratory groups is as follows:

Group Number	Pre-defined order of States	Not Allowed States	Output active on state number
1	11, 12, 8, 15, 10, 3, 13, 7, 2, 1, 4	0, 5, 6, 9, 14	11
2	12, 10, 13, 4, 2, 7, 6, 14, 5, 3	0, 1, 8, 9, 11, 15	12
3	11, 13, 2, 6, 15, 14, 3, 8, 12, 4	0, 1, 5, 7, 9, 10	11
4	15, 3, 10, 6, 11, 4, 9, 12, 2	0, 1, 5, 7, 8, 13, 14	15
5	12, 9, 1, 7, 4, 2, 5, 8, 14, 11, 13	0, 3, 6, 10, 15	12
6	6, 3, 15, 7, 4, 14, 1, 9, 10, 13, 2	0, 5, 8, 11, 12	6

Group Number	**Pre-defined order of States**	**Not Allowed States**	**Output active on state number**
7	14, 5, 10, 1, 2, 7, 3, 9, 6	0, 4, 8, 11, 12, 13, 15	14
8	6, 1, 15, 11, 7, 13, 9, 3, 14, 4	0, 2, 5, 8, 10, 12	6
9	14, 4, 5, 15, 13, 2, 3, 11, 12, 1	0, 6, 7, 8, 9, 10	14
10	11, 8, 3, 9, 1, 2, 13, 7, 15, 4, 5	0, 6, 10, 12, 14	11
11	12, 15, 6, 14, 11, 10, 4, 5, 1	0, 2, 3, 7, 8, 9, 13	12
12	15, 8, 9, 5, 3, 1, 10, 14, 2, 11	0, 4, 6, 7, 12, 13	15
13	1, 3, 9, 10, 11, 6, 8, 13, 15, 14	0, 2, 4, 5, 7, 12	1
14	3, 4, 15, 14, 13, 10, 6, 7, 9, 11	0, 1, 2, 5, 8, 12	3
15	4, 5, 2, 15, 7, 11, 6, 8, 3, 13, 9	0, 1, 10, 12, 14	4
16	9, 11, 8, 7, 12, 14, 3, 2, 10, 4	0, 1, 5, 6, 13, 15	9
17	6, 1, 9, 11, 4, 14, 3, 8, 5, 15, 13	0, 2, 7, 10, 12	6
18	12, 1, 9, 8, 15, 5, 13, 7, 4	0, 2, 3, 6, 10, 11, 14	12
19	6, 4, 14, 2, 3, 7, 13, 15, 8, 11	0, 1, 5, 9, 10, 12	6
20	13, 11, 12, 6, 7, 4, 10, 9, 15, 8, 14	0, 1, 2, 3, 5	13
21	6, 13, 1, 14, 4, 11, 8, 12, 7, 10	0, 2, 3, 5, 9, 15	6
22	1, 7, 6, 12, 9, 8, 2, 14, 4, 15, 3	0, 5, 10, 11, 13	1
23	14, 8, 7, 15, 12, 13, 11, 9, 3, 1	0, 2, 4, 5, 6, 10	14
24	13, 7, 5, 9, 11, 6, 15, 14, 4, 8	0, 1, 2, 3, 10, 12	13
25	2, 10, 1, 15, 14, 13, 7, 12, 11, 4, 9	0, 3, 5, 6, 8	2
26	5, 2, 13, 14, 8, 7, 4, 9, 15	0, 1, 3, 6, 10, 11, 12	5
27	8, 7, 11, 2, 14, 6, 10, 4, 3, 12	0, 1, 5, 9, 13, 15	8
28	15, 4, 11, 5, 8, 9, 7, 2, 3	0, 1, 6, 10, 12, 13, 14	15
29	8, 6, 13, 4, 11, 15, 9, 10, 5	0, 1, 2, 3, 7, 12, 14	8
30	3, 12, 13, 1, 5, 10, 4, 7, 11, 15, 6	0, 2, 8, 9, 14	3
31	7, 15, 3, 13, 8, 4, 1, 6, 12	0, 2, 5, 9, 10, 11, 14	7
32	9, 15, 14, 2, 12, 13, 4, 3, 8, 1	0, 5, 6, 7, 10, 11	9
33	7, 1, 5, 10, 13, 15, 2, 12, 8	0, 3, 4, 6, 9, 11, 14	7
34	13, 8, 5, 4, 7, 3, 15, 2, 1, 9, 10	0, 6, 11, 12, 14	13
35	2, 13, 9, 11, 10, 5, 8, 3, 4, 6, 7	0, 1, 12, 14, 15	2

Now deliver and impress me (Some hints on how you might achieve this are included in a supplementary document, but in later documents you are left to derive this material for yourself).