

HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY – VNU HCMC
OFFICE FOR INTERNATIONAL STUDY PROGRAM
FACULTY OF ELECTRICAL AND ELECTRONIC ENGINEERING

————— * —————



DIGITAL SYSTEMS (LAB) EXPERIMENTAL REPORT (Prelab 1)

Lecturer : **Mr. Nguyễn Tuấn Hùng**
Subject : **Digital Systems**
Class : **TT06**
Name : **Lương Triển Thắng**
Student ID : **2051194**

Ho Chi Minh City, 31st May, 2022

Contents

- I **Laboratory 1:**
 - Get started with *FPGA**** **2**
 - 1. Get started with FPGA 2
 - 2. Know how to program one-bit wide 2-to-1 multiplexer 2
 - a. Code 3
 - b. Waveform 3
 - c. Result of RTL viewer 3
 - 3. Know how to interface 7-segment LED 4
 - a. Code 4
 - b. Waveform 4
 - c. Result of RTL viewer 5

I Laboratory 1

Get started with FPGA

1. Get started with FPGA

```
LEDR(9) <= SW(9);  
LEDR(8) <= SW(8);  
...  
LEDR(0) <= SW(0);
```

Code

```
LIBRARY IEEE;  
USE IEEE.STD_LOGIC_1164.ALL;  
  
ENTITY Exc1 IS  
    PORT (  
        SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);  
        LEDR : OUT STD_LOGIC_VECTOR(9 DOWNTO 0)  
    );  
END ENTITY;  
  
ARCHITECTURE behavior OF Exc1 IS  
BEGIN  
    LEDR <= SW;  
END ARCHITECTURE;  
END Logic;
```

2. Know how to program one-bit wide 2-to-1 multiplexer

$$m \leq (\text{NOT } (s) \text{ AND } x) \text{ OR } (s \text{ AND } y)$$

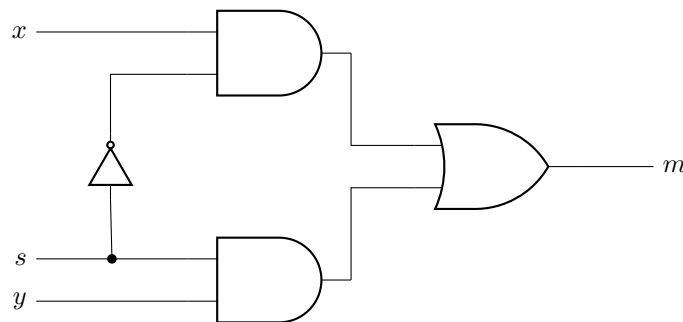


Figure 1.2.a: Circuit diagram

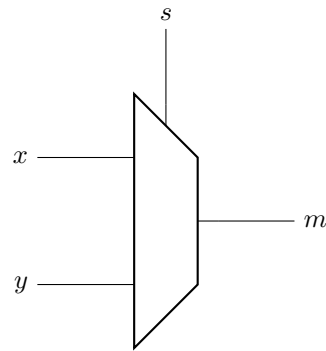


Figure 1.2.b: Circuit diagram

a. Code

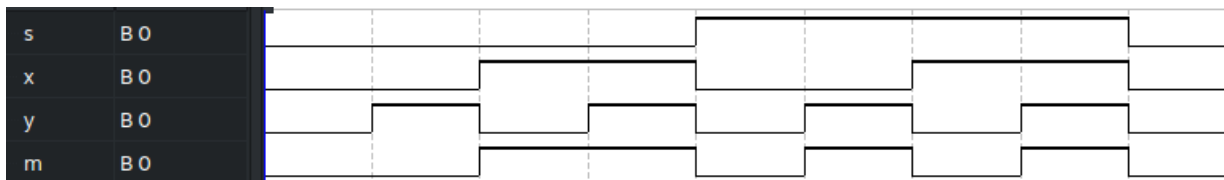
```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Exc2 IS
    PORT (
        x : IN std_logic;
        s : IN std_logic;
        y : IN std_logic;
        m : OUT std_logic
    );
END ENTITY;

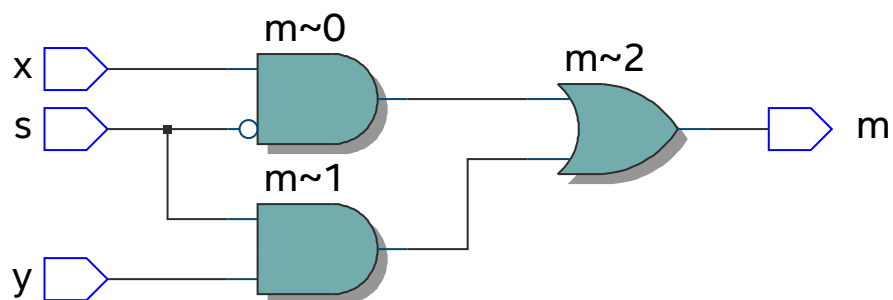
ARCHITECTURE arch OF Exc2 IS
BEGIN
    m <= (NOT(s) AND x) OR (s AND y);
END arch;

```

b. Waveform



c. Result of RTL viewer



3. Know how to interface with 7-segment LED

c_1	c_0	HEX0	LED
0	0	0 1 1 1 1 0 1	8
0	1	1 0 0 1 1 1 1	E
1	0	0 1 1 0 0 0 0	9
1	1	1 1 1 1 1 1 0	0

a. Code

```

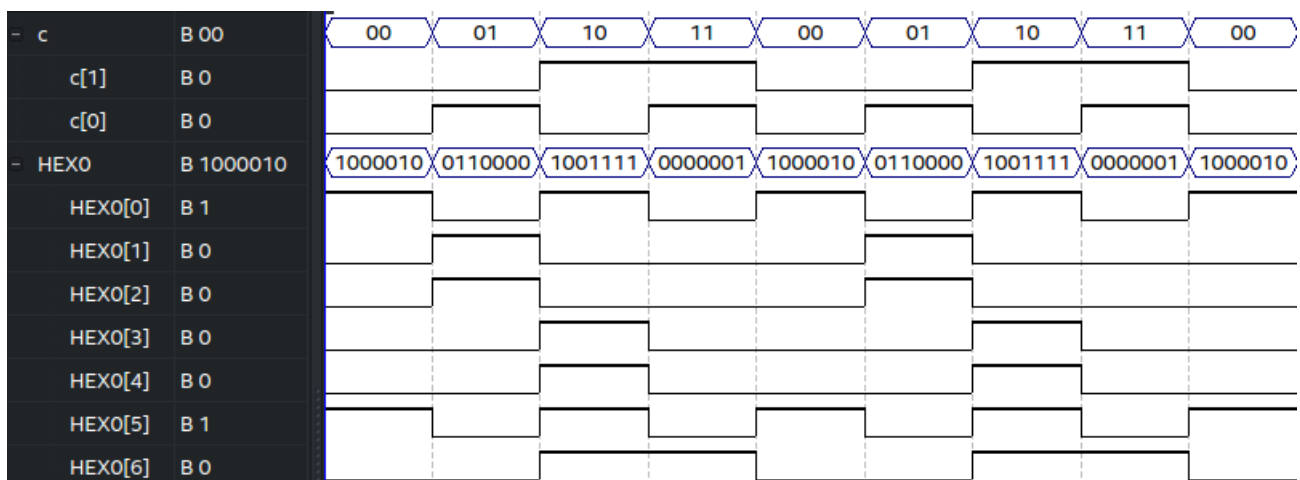
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Exc3 IS
    PORT (
        c : IN std_logic_vector(1 DOWNTO 0);
        HEX0 : OUT std_logic_vector(0 TO 6)
    );
END Exc3;

ARCHITECTURE behavior OF Exc3 IS
    SIGNAL HEX : std_logic_vector(0 TO 6);
BEGIN
    HEX0 <= NOT(HEX); -- 7SEGLED is active low.
    WITH c SELECT
    HEX <= "0111101" WHEN "00",
           "1001111" WHEN "01",
           "0110000" WHEN "10",
           "1111110" WHEN "11",
           "0000000" WHEN OTHERS;
END behavior;

```

b. Waveform



c. Result of RTL viewer

