

HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY – VNU HCMC  
OFFICE FOR INTERNATIONAL STUDY PROGRAM  
FACULTY OF ELECTRICAL AND ELECTRONIC ENGINEERING

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## DIGITAL SYSTEMS (LAB) EXPERIMENTAL REPORT (Prelab 2)

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# II Pre Laboratory 2

## Adder and flip-flop

### 1. Known how to program full adder

$$s = a \oplus b \oplus c_{in}$$
$$c_{out} = ab \oplus c_{in}(a + b)$$

#### a. Code

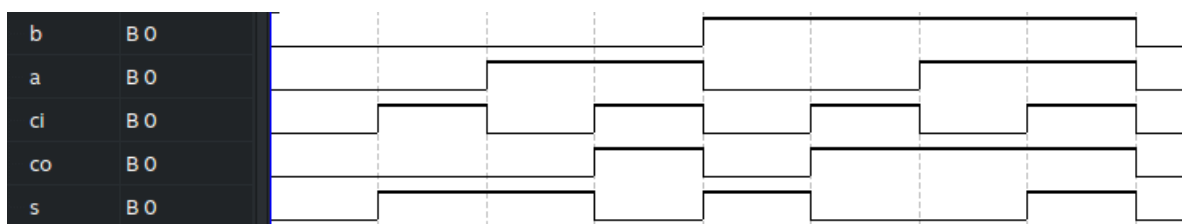
Exc1.vhdl

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

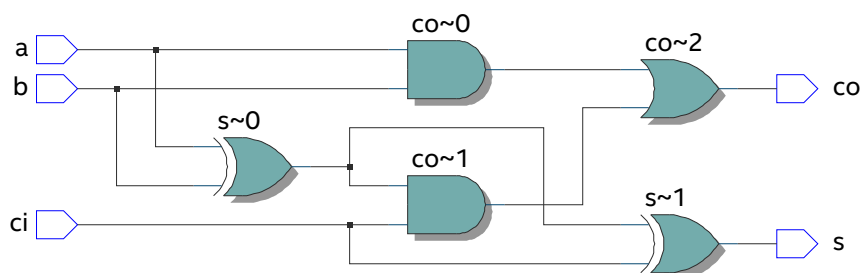
ENTITY Exc1 IS
    PORT (
        a : IN STD_LOGIC;
        b : IN STD_LOGIC;
        ci : IN STD_LOGIC;
        s : OUT STD_LOGIC;
        co : OUT STD_LOGIC
    );
END Exc1;

ARCHITECTURE arch OF Exc1 IS
BEGIN
    s <= a XOR b XOR ci;
    co <= (a AND b) OR (ci AND (a XOR b));
END ARCHITECTURE;
```

#### b. Waveform



#### c. Result of RTL viewer



## 2. Understand RS-latched circuit

### a. Code

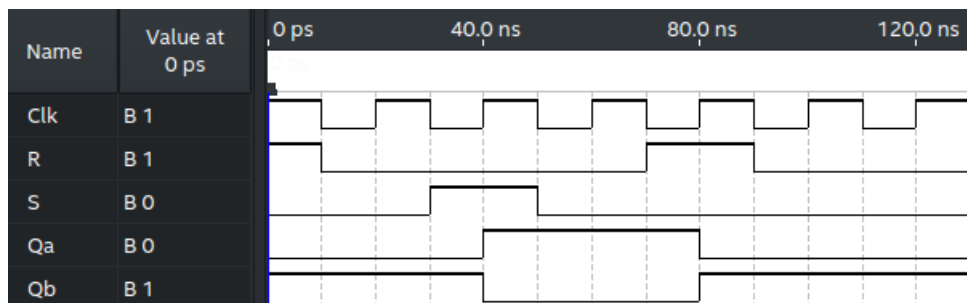
Exc2.vhdl

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

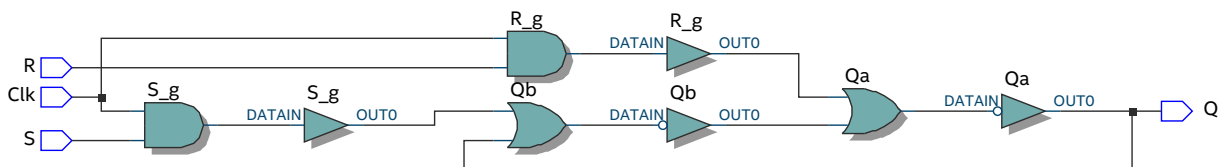
ENTITY Exc2 IS
    PORT (
        Clk, R, S : IN STD_LOGIC;
        Q : OUT STD_LOGIC
    );
END Exc2;

ARCHITECTURE Structural OF Exc2 IS
    SIGNAL R_g, S_g, Qa, Qb : STD_LOGIC;
    ATTRIBUTE KEEP : BOOLEAN;
    ATTRIBUTE KEEP OF R_g, S_g, Qa, Qb : SIGNAL IS TRUE;
BEGIN
    R_g <= R AND Clk;
    S_g <= S AND Clk;
    Qa <= R_g NOR Qb;
    Qb <= S_g NOR Qa;
    Q <= Qa;
END Structural;
END ARCHITECTURE;
```

### b. Waveform



### c. Result of RTL viewer



### 3. Understand D-latched circuit

#### a. Code

##### Exc3.vhdl

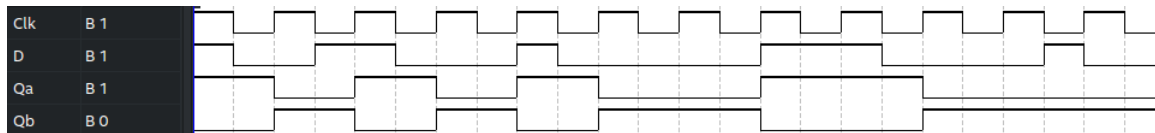
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Exc3 IS
    PORT (
        Clk, D : IN STD_LOGIC;
        Q : OUT STD_LOGIC
    );
END Exc3;

ARCHITECTURE Structural OF Exc3 IS
    SIGNAL R_g, S_g, Qa, Qb, S, R : STD_LOGIC;
    ATTRIBUTE KEEP : BOOLEAN;
    ATTRIBUTE KEEP OF R_g, S_g, Qa, Qb : SIGNAL IS TRUE;

BEGIN
    S <= D;
    R <= NOT(D);
    R_g <= R AND Clk;
    S_g <= S AND Clk;
    Qa <= R_g NOR Qb;
    Qb <= S_g NOR Qa;
    Q <= Qa;
END Structural;
```

#### b. Waveform



#### c. Result of RTL viewer

