HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY – VNU HCMC
OFFICE FOR INTERNATIONAL STUDY PROGRAM
FACULTY OF ELECTRICAL AND ELECTRONIC ENGINEERING

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DIGITAL SYSTEMS (LAB)
EXPERIMENTAL REPORT (Lab 0)

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Contents

Laboratory 0

VHDL Description

1. Write VHDL code to describe a digital circuit

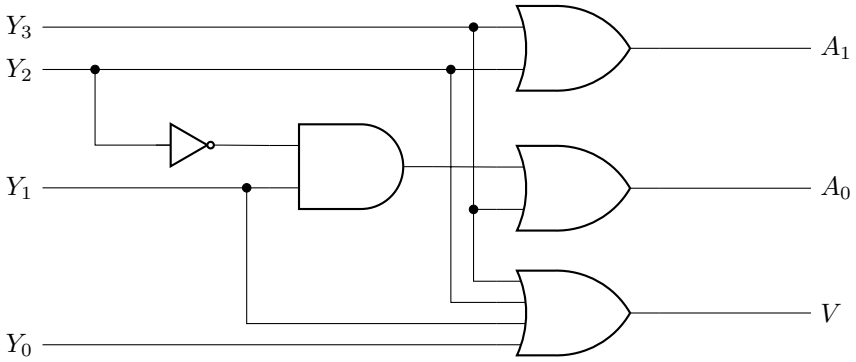
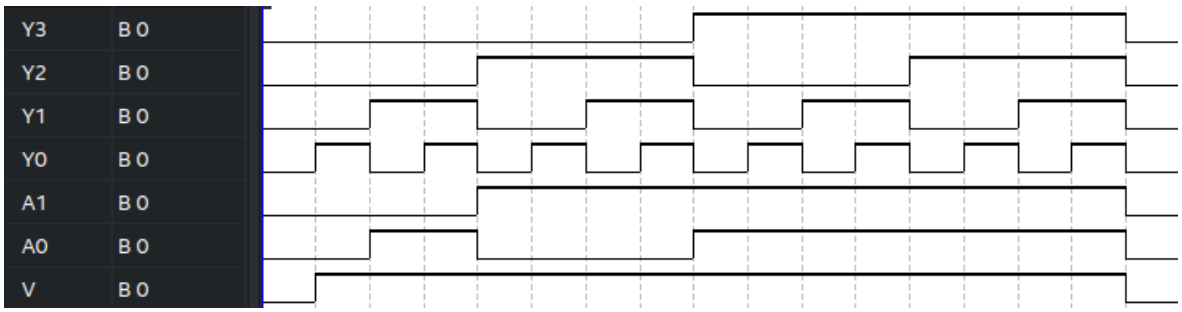


Figure 0.1.a: Circuit diagram

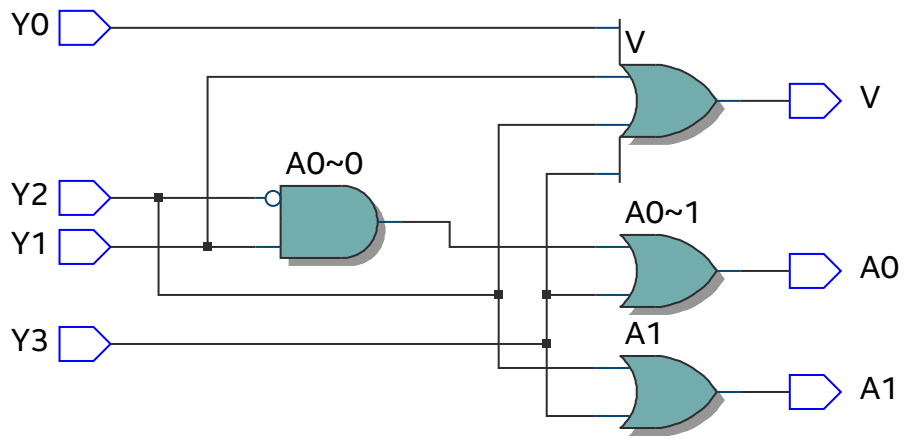
a. Code

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Exc1 IS
        PORT (
                Y3, Y2, Y1, Y0 : IN STD_LOGIC;
                A1, A0, V : OUT STD_LOGIC
        );
END Exc1;
ARCHITECTURE Logic OF Exc1 IS
BEGIN
        A1 <= Y3 OR Y2;
        A0 <= Y3 OR (NOT(Y2) AND Y1);
        V <= Y0 OR Y1 OR Y2 OR Y3;
END Logic;
```

b. Waveform



c. Result of RTL viewer



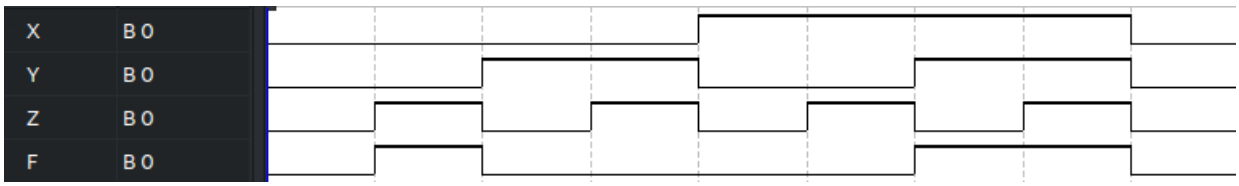
2. Write VHDL code to describe a truth table

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

a. Code

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Exc2 IS
        PORT (
                X, Y, Z : IN STD_LOGIC;
                F : OUT STD_LOGIC
        );
END Exc2;
ARCHITECTURE Logic OF Exc2 IS
        SIGNAL input : std_logic_vector(2 DOWNTO 0);
BEGIN
        input(2) <= X;
        input(1) <= Y;
        input(0) <= Z;
        WITH input SELECT
        F <= '1' WHEN "001",
             '1' WHEN "110",
             '1' WHEN "111",
             '0' WHEN OTHERS;
END Logic;
```

b. Waveform



c. Result of RTL viewer