HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY – VNU HCMC
OFFICE FOR INTERNATIONAL STUDY PROGRAM
FACULTY OF ELECTRICAL AND ELECTRONIC ENGINEERING

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DIGITAL SYSTEMS (LAB)
EXPERIMENTAL REPORT (Prelab 3)

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III Pre Laboratory 3

Adders, subtractors and multipliers

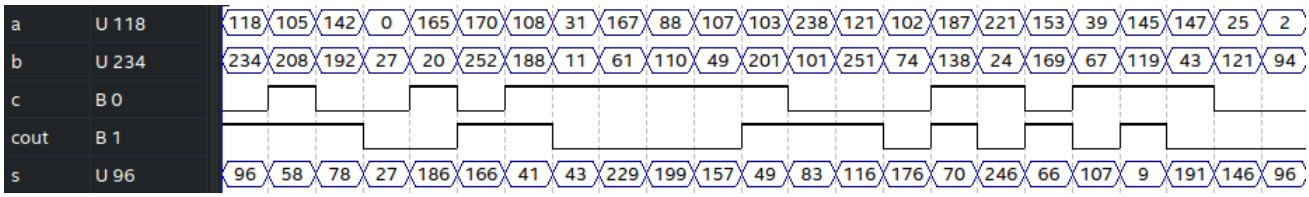
1. Known how to program an adder using '+' sign in VHDL

a. Code

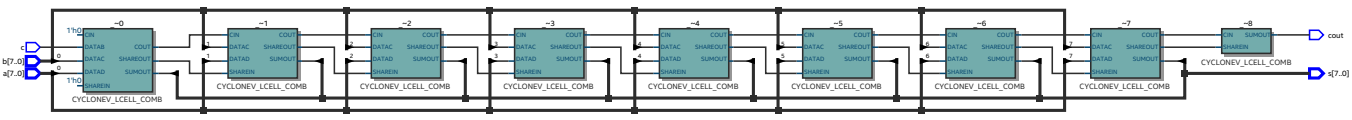
Exc1.vhdl

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.std_logic_signed.ALL;

ENTITY Exc1 IS
        PORT (
                a, b : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
                c : IN STD_LOGIC;
                s : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
                cout : OUT STD_LOGIC
        );
END Exc1;

ARCHITECTURE arch OF Exc1 IS
        SIGNAL sum : STD_LOGIC_VECTOR(8 DOWNTO 0);
BEGIN
        sum <= ('0' & a) + ('0' & b) + ("0000000" & c);
        s <= sum(7 DOWNTO 0);
        cout <= sum(8);
END ARCHITECTURE;
```

b. Waveform



c. Result of RTL viewer



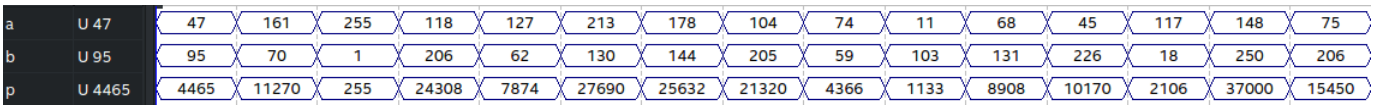
2. Known how to program a multiplier

a. Code

Exc2.vhdl

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Exc2 IS
        PORT (
                a, b : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
                p : OUT STD_LOGIC_VECTOR(15 DOWNTO 0)
        );
END Exc2;

ARCHITECTURE arch OF Exc2 IS
        SIGNAL a_padded, zero : STD_LOGIC_VECTOR(15 DOWNTO 0);
        TYPE ab_t IS ARRAY(0 TO 7) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
        SIGNAL ab : ab_t;
BEGIN

        zero <= "0000000000000000";
        a_padded <= "00000000" & a;

        ab(0) <= a_padded WHEN b(0) = '1' ELSE zero;
        sum : FOR i IN 1 TO 7 GENERATE
                ab(i) <= a_padded(15 - i DOWNTO 0) & zero(i - 1 DOWNTO 0) WHEN b(i) = '1' ELSE zero;
        END GENERATE;

        p <= ab(0) + ab(1) + ab(2) + ab(3) + ab(4) + ab(5) + ab(6) + ab(7);
END ARCHITECTURE;
```

b. Waveform



c. Result of RTL viewer