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DIGITAL SYSTEMS (LAB)
AN ENHANCED PROCESSOR

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Contents

I Introduction

In computing and computer science, a processor or processing unit is an electrical component (digital circuit) that performs operations on an external data source, usually memory or some other data stream. Based on the von Neumann architecture, they contain at least a control unit (CU), an arithmetic logic unit (ALU), and processor registers.

The world's first processor had introduced by Intel in the late 1971, named Intel 4004. It is a 4-bit processor with 12-bit address width. In 1975, a new game changer appreared, MOS Technology 6502, with 8-bit data width, 16-bit address width. It was 'the heart' of most consumer personal computers, game consoles in the late 70s and 80s, including the Apple I, Apple II, Atari 7800, Commodore 64, Commodore VIC-20, Nintendo Entertainment System (NES), etc.

After years of development, numerous of instruction set architectures (ISAs) have been created. In 2022, there are some popular ISAs which are in used and development, such as:

– x86-64: 2001, org. 1978, Intel/AMD
– MIPS: 1981
– PowerISA: 1990, PowerPC
– ARM: 1983, ARM/Raspberry/Qualcomm/...
– RISC-V: 2010
– ARM64: 2011, Apple/Nvidia/Qualcomm/Samsung/...

In this project, I will introduce two processors with two different ISAs.

– A nine-bit processor: followed Lab5, Lab6 instructions
    + 8 instructions ⇒ too few.
    + 9-bit data width ⇒ one bit more than a word (8 bits), awkward.
    + 7-bit address width ⇒ maximum of 128 addresses (16 bytes).
   ⇒ Inefficient.
– An eight-bit processor
    + 21 instructions, 8 reserved.
    + 8-bit data width.
    + 16-bit address width ⇒ up to 65536 addresses (8KB).

The source code for this project is rather large, I would not attached into this report. The link for the source code is present in the last chapter.

II An enhanced processor

A 9-bit processor

According to instructions of Lab5 and Lab6, the details of the ‘enhanced processor’ would be described in below.

1. Registers

Register	Width (bits)	Purpose
R0 - R6	9	General
R7	9	PC

2. Instruction types

Normal and Misc type of instruction requires only one instruction input.
Immediate type requires immediate value which successive with the instruction input.

a. Normal

	8 6	5 3	2 0
mv	000	DR	SR
add	010	RX	RY
sub	011	RX	RY
ld	100	DR	BaseR
st	101	SR	BaseR
mvnz	110	DR	SR

b. Immediate

	8 6	5 3	2 0	8 0
mvi	001	DR	any	imm9

c. Misc

	8 6	5 3	2 0
halt	111	any	any

3. Instruction details

Instruction	Opcode	Operation	Cycles	Assembler format
mv	000	`DR <= SR`	1	mv DR, SR
mvi	001	`DR <= imm9`	2	mv DR, imm9
add	010	`RX <= RX + RY`	3	add RX, RY
sub	011	`RX <= RX - RY`	3	sub RX, RY
ld	100	`DR <= mem[BaseR]`	2	ld DR, BaseR
st	101	`mem[BaseR] <= SR`	3	st SR, BaseR
mvnz	110	`DR <= SR if G /= 0`	2 or 3	mvnz DR, SR
halt	111	Halt the processor	∞	halt

4. Transition table

	T_1	T_2	T_3
mv	RY_{out} = '1' RX_{in} = '1' **done** = '1'		
mvi	incr = '1' $addr_{in}$ = '1' $R7_{in}$ = '1'	DIN_{out} = '1' RX_{in} = '1' **done** = '1'	
add	RX_{out} = '1' A_{in} = '1'	RY_{out} = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'
sub	RX_{out} = '1' A_{in} = '1'	RY_{out} = '1' G_{in} = '1' AddSub = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'
ld	RY_{out} = '1' $addr_{in}$ = '1'	DIN_{out} = '1' RX_{in} = '1' **done** = '1'	

st	RY_{out} = '1'
	$addr_{in}$ = '1'
		RX_{out} = '1'
		$Dout_{in}$ = '1'
			W = '1'
			done = '1'

mvnz	G_{out} = '1'	done = zero	RY_{out} = '1' RX_{in} = '1' **done** = '1'
halt	**halt** = '1'		

5. Note

A register contains 7 bits, while an address uses 7 bits to define, so source address of ld and destination address of st only uses BaseR[6:0].

In ld, Base[8:7] will define the load source, '00' for memory, '10' for KEY, '11' for SW.

In st, Base[8:7] will define the store destination, '00' for memory, '10' for LED.

6. Assembler

For ease of writing machine code for memory, I wrote a small program in Python assemble machine code.

Below is the example of a multiplier program which takes two inputs (address #50 and SW), after calculating the product, it will store into address #52 then output to LED.

I will use this to demo the processor in the next section.

Input assembly file

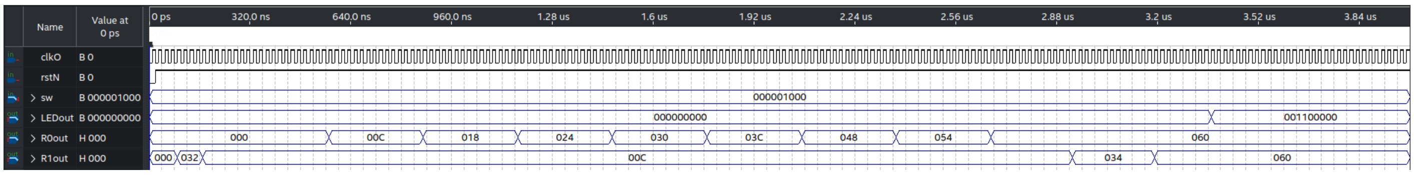
```
% R1 <= M[50]
mvi   R1, #50
ld    R1, R1

% R2 <= SW (600 in oct)
mvi   R4, #384
ld    R4, R4

% R0 <= R1 * R4
mvi   R2,#1
mv    R5,R7
add   R0, R1
sub   R4, R2
mvnz R7, R5

% M[52] <= R0
mvi R1, #52
st R0, R1

% R1 <= M[52]
mvi   R1, #52
ld    R1, R1

% LED (200 in oct) <= R1
mvi R6, #128
st R1, R6

halt

data 50, #12
```

Output memory file

```
WIDTH=9;
DEPTH=128;

ADDRESS_RADIX=UNS;
DATA_RADIX=OCT;

CONTENT BEGIN
        [0..127]        :         000;
        0        :        110;        -- mvi   R1, #50;
        1        :        062;
        2        :        411;        -- ld    R1, R1
        3        :        140;        -- mvi   R4, #384;
        4        :        600;
        5        :        444;        -- ld    R4, R4
        6        :        120;        -- mvi   R2,#1;
        7        :        001;
        8        :        057;        -- mv    R5,R7
        9          :          201;          -- add   R0, R1
        10          :          342;          -- sub   R4, R2
        11          :          675;          -- mvnz R7, R5
        12          :          110;          -- mvi R1, #52;
        13          :          064;
        14          :          501;          -- st R0, R1
        15          :          110;          -- mvi   R1, #52;
        16          :          064;
        17          :          411;          -- ld    R1, R1
        18          :          160;          -- mvi R6, #128;
        19          :          200;
        20          :          516;          -- st R1, R6
        21          :          700;          -- halt
        50          :          014;          -- data 50, #12
END;
```

7. Demonstration

According to the program above and the value of SW = 000001000 = 8, the expected output R0 = R1 = $96_{10} = 060_{16}$ = LED = 001100000_2



8. Conclusion

The processor can run simple programs, but it would be a hassle when dealing with more complex programs that require large memory (> 16 bytes), specialized instruction such as compare, branch, bitwise not, bitwise and,...

Thus, I came up with a better solution with describe in Chapter 3.

III A better approach

An 8-bit processor, but better

1. Registers

The processor has 10 local registers. Registers R5 and R6 are the high and low index registers, H contains first 8 bits of a 16 bits value, L contains last 8 bits of a 16 bits value, these registers use in HL required instructions.

Register	Width (bits)	Purpose
R0	8	General
R1	8	General
R2	8	General
R3	8	General
R4	8	General
R5/H	8	General/High index register
R6/L	8	General/Low index register
R7	8	General/in-out value
flags	4	less-equal-greater-carry
PC	16	Program counter

2. Input/output devices

devid (dd)	Input	Output
00	KEY	LED
01	SW	8-bit decimal output to 7-segment display
10	n/a	16-bit decimal output to 7-segment display
11	n/a	16-bit hexadecimal output to 7-segment display

3. Instruction types

a. RY-imm8

RY (mode 0)

	7 … 4	3	2 … 0	7 … 3	2 … 0
mv	0000	0	DR	00000	SR
add	0001	0	RX	00000	RY
sub	0010	0	RX	00000	RY
mul	0011	0	SR1	00000	SR2
cmp	0110	0	SR1	00000	SR2
and	1001	0	RX	00000	RY

imm8 (mode 1)

	7 4	3	2 0	7 0
mv	0000	1	DR	imm8
add	0001	1	RX	imm8
sub	0010	1	RX	imm8
mul	0011	1	SR1	imm8
cmp	0110	1	SR1	imm8
and	1001	1	RX	imm8

b. RY-HL

Instructions of this type require an 16-bit value as the source address of ld and destination address of st, br.

RY (mode 0)

In this mode, the source/destination address is the value of RX (8 bits), which select address in range of 0 to 255. To address full range of 8KB of memory, we need to use mode 1.

	7 4	3	2 0	7 3	2 0
ld	0100	0	DR	00000	BaseR
st	0101	0	SR	00000	BaseR
br	0111	0	l-e-g	00000	BaseR

HL (mode 1)

In this mode, the source/destination address is 16-bit wide, H (R5) is the first half of the address, L (R6) is the second half of the address.

	7 4	3	2 0
ld	0100	1	DR
st	0101	1	SR
br	0111	1	l-e-g

c. RX as dest and src

	7 4	3	2 0
not	1000	0	RX
tcpl	1000	1	RX
shl	1010	0	RX
shr	1010	1	RX
inc	1100	0	RX
dec	1100	1	RX
incc	1101	0	RX
decc	1101	1	RX

d. Misc

	7 … 4	3 … 2	1 … 0
in	1111	00	dd
out	1100	01	dd

	7 … 4	3 … 0
lda	1111	1110
halt	1100	1111

4. Instruction details

Instruction	Opcode	Mode	Operation	Cycles	Assembler format
mv	0000		`DR <= SR/imm8`	1	mv DR, SR/imm8
add	0001		`RX <= RX + RY/imm8`	5	add RX, RY/imm8
sub	0010		`RX <= RX - RY/imm8`	5	sub RX, RY/imm8
mul	0011		`HL <= RX * RY/imm8`	6	mul RX, RY/imm8
ld	0100		`DR <= mem[BaseR/HL]`	4 or 2	ld DR, BaseR/HL
st	0101		`mem[BaseR/HL] <= SR`	4 or 2	st SR, BaseR/HL
cmp	0110		`flags <= RX ? RY`	4	cmp RX, RY
br	0111		`PC <= BaseR/HL` if l-e-g	3 or 1	br leg, BaseR/HL
not	1000	0	`RX <= not(RX)`	3	not RX
tcpl	1000	1	`RX <= not(RX) + 1`	3	tcpl RX
and	1001		`RX <= RX AND RY`	5	and RX, RY
shl	1010	0	`RX <= RX << 1`	3	shl RX
shr	1010	1	`RX <= RX >> 1`	3	shr RX
reserved	1011				
inc	1100	0	`RX <= RX + 1`	3	inc RX
dec	1100	1	`RX <= RX - 1`	3	dec RX
incc	1101	0	`RX <= RX + 1` if carry	3 or 1	incc RX
decc	1101	1	`RX <= RX - 1` if carry	3 or 1	decc RX
reserved	1110				
misc	1111		Look at below table		

Instruction	Opcode	Misc code	Operation	Cycles	Assembler format
in	1111	00dd	`R7 <= dev[dd]`	1	in dd
out	1111	01dd	`dev[dd] <= R7/HL`	1	out dd
reserved	1111	1000			
reserved	1111	1001			
reserved	1111	1010			
reserved	1111	1011			
reserved	1111	1100			
reserved	1111	1101			
lda	1111	1110	`HL <- PC`	3	
halt	1111	1111	Halt the processor	∞	halt

5. Transition table

	T_1	T_2	T_3	T_4	T_5	T_6
mv (mode 0)	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	RY_{out} = ‘1’ **done** = ‘1’			
mv (mode 1)	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	DIN_{out} = ‘1’ **done** = ‘1’			
add (mode 0)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	add = ‘1’ RY_{out} = ‘1’ G_{in} = ‘1’ $carry_{in}$ = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	
add (mode 1)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	add = ‘1’ DIN_{out} = ‘1’ G_{in} = ‘1’ $carry_{in}$ = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	
sub (mode 0)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	sub = ‘1’ RY_{out} = ‘1’ G_{in} = ‘1’ $carry_{in}$ = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	
sub (mode 1)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	sub = ‘1’ DIN_{out} = ‘1’ G_{in} = ‘1’ $carry_{in}$ = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	
mul (mode 0)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	RY_{out} = ‘1’ $G16_{in}$ = ‘1’ $prod_{out}$ = ‘1’	$G16_{H_{out}}$ = ‘1’ $R5_{in}$ = ‘1’	$G16_{L_{out}}$ = ‘1’ $R6_{in}$ = ‘1’ **done** = ‘1’
mul (mode 1)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	DIN_{out} = ‘1’ $G16_{in}$ = ‘1’ $prod_{out}$ = ‘1’	$G16_{H_{out}}$ = ‘1’ $R5_{in}$ = ‘1’	$G16_{L_{out}}$ = ‘1’ $R6_{in}$ = ‘1’ **done** = ‘1’
ld (mode 0)	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	PC_{out} = ‘1’ $addr_{in}$ = ‘1’ RY_{out} = ‘1’	DIN_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’		
ld (mode 1)	$addr_{in}$ = ‘1’ HL_{out} = ‘1’	DIN_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’				
st (mode 0)	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	PC_{out} = ‘1’ $addr_{in}$ = ‘1’ RY_{out} = ‘1’	RX_{out} = ‘1’ $dout_{in}$ = ‘1’	W = ‘1’ **done** = ‘1’	
st (mode 1)	$addr_{in}$ = ‘1’ HL_{out} = ‘1’	RX_{out} = ‘1’ $dout_{in}$ = ‘1’	W = ‘1’ **done** = ‘1’			
cmp (mode 0)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	RY_{out} = ‘1’ cmp_{in} = ‘1’ **done** = ‘1’		
cmp (mode 1)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	DIN_{out} = ‘1’ cmp_{in} = ‘1’ **done** = ‘1’		
br (mode 0)	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’ **done** = $\overline{\text{brEn}}$	$IR2_{in}$ = ‘1’	RY_{out} = ‘1’ PC_{in} = ‘1’ **done** = ‘1’			
br (mode 1)	PC_{in} = brEn $PCmode$ = ‘1’ **done** = ‘1’					
and (mode 0)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	and = ‘1’ RY_{out} = ‘1’ G_{in} = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	
and (mode 1)	RX_{out} = ‘1’ A_{in} = ‘1’	incr = ‘1’ $addr_{in}$ = ‘1’ PC_{out} = ‘1’	$IR2_{in}$ = ‘1’	and = ‘1’ DIN_{out} = ‘1’ G_{in} = ‘1’	G_{out} = ‘1’ RX_{in} = ‘1’ **done** = ‘1’	

	T_1	T_2	T_3	T_4	T_5	T_6
not	RX_{out} = '1' A_{in} = '1'	not = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
tcpl	RX_{out} = '1' A_{in} = '1'	tcpl = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
shl	RX_{out} = '1' A_{in} = '1'	shl = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
shr	RX_{out} = '1' A_{in} = '1'	shr = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
inc	RX_{out} = '1' A_{in} = '1'	inc = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
dec	RX_{out} = '1' A_{in} = '1'	dec = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
incc	RX_{out} = '1' A_{in} = '1' **done** = $\overline{carry_{out}}$	inc = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
decc	RX_{out} = '1' A_{in} = '1' **done** = $\overline{carry_{out}}$	dec = '1' G_{in} = '1'	G_{out} = '1' RX_{in} = '1' **done** = '1'			
in	$devD_{sel}$ = '1' dev_{out} = '1' $R7_{in}$ = '1' **done** = 1					
out	$devD_{sel}$ = '1' dev_{in} = '1' **done** = 1					
lda	PC_{out} = '1' $G16_{in}$ = '1'	$G16_{H_{out}}$ = '1' $R5_{in}$ = '1'	$G16_{L_{out}}$ = '1' $R6_{in}$ = '1' **done** = '1'			
halt	halt = '1'					

6. Assembler

I also wrote a small program in Python assemble machine code for this 8-bit processor.

Below is the example of a multiplier program which takes two inputs (address #50 and SW), after calculating the product, it will store into address #52 then output to LED.

I will use this to demo the processor in the next section.

Input assembly file

```
% R1 <= M[50]
mv R1, #50
ld R1, R1

% R2 <= SW (dd = 01)
in 01
mv R4, R7

% R0 <= R1 * R4
lda
add R0, R1
sub R4, #1
cmp R4, #0
```

```
br g, HL

% M[52] <= R0
mv R1, #52
st R0, R1

% R1 <= M[52]
mv R1, #52
ld R1, R1

% LED (dd = 00) <= R1
mv R7, R1
out 00

halt

data 50, #12
```

Output memory file

```
WIDTH=8;
DEPTH=65536;

ADDRESS_RADIX=UNS;
DATA_RADIX=BIN;

CONTENT BEGIN
        [0..65535]        :        00000000;
        0        :        00001001;        --mv r1, #50
        1        :        00110010;
        2        :        01000001;        --ld r1, r1
        3        :        00000001;
        4        :        11110001;        --in 01
        5        :        00000100;        --mv r4, r7
        6        :        00000111;
        7        :        11111110;        --lda
        8        :        00010000;        --add r0, r1
        9        :        00000001;
        10        :        00101100;        --sub r4, #1
        11        :        00000001;
        12        :        01101100;        --cmp r4, #0
        13        :        00000000;
        14        :        01111001;        --br g, hl
        15        :        00001001;        --mv r1, #52
        16        :        00110100;
        17        :        01010000;        --st r0, r1
        18        :        00000001;
        19        :        00001001;        --mv r1, #52
        20        :        00110100;
        21        :        01000001;        --ld r1, r1
        22        :        00000001;
        23        :        00000111;        --mv r7, r1
        24        :        00000001;
        25        :        11110100;        --out 00
        26        :        11111111;        --halt
        50        :        00001100;        --data 50, #12
END;
```

Instead of using traditional method for multiplying, multiply using logic gates by mul instruction is a better option.

Input assembly file

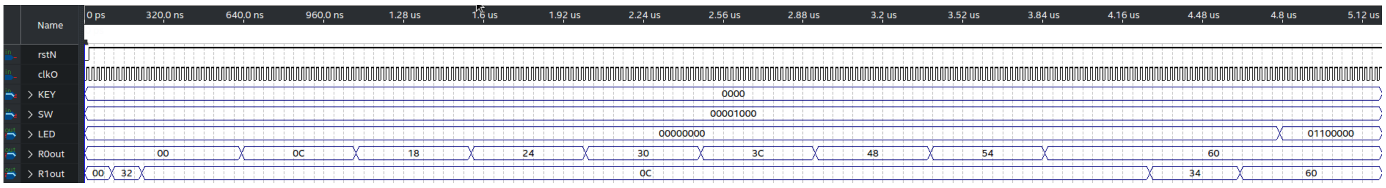
```
% R1 <= M[50]
mv   R1, #50
ld    R1, R1

% R2 <= SW (600 in oct)
in 01
mv R4, R7

mul R1, R4

% M[52] <= R0
mv R1, #52
st R6, R1

% R1 <= M[52]
mv   R1, #52
ld    R1, R1

% LED (200 in oct) <= R1
mv R7, R1
out 00

halt

data 50, #12
```

Output memory file

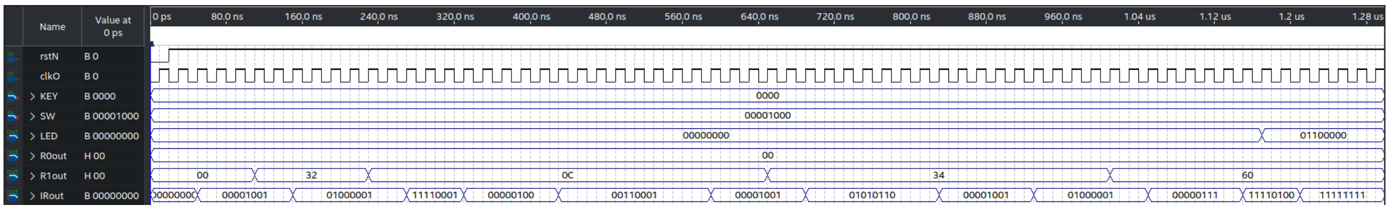
```
WIDTH=8;
DEPTH=65536;

ADDRESS_RADIX=UNS;
DATA_RADIX=BIN;

CONTENT BEGIN
        [0..65535]        :         00000000;
        0         :         00001001;         --mv   r1, #50
        1         :         00110010;
        2         :         01000001;         --ld    r1, r1
        3         :         00000001;
        4         :         11110001;         --in 01
        5         :         00000100;         --mv r4, r7
        6         :         00000111;
        7         :         00110001;         --mul r1, r4
        8         :         00000100;
        9         :         00001001;         --mv r1, #52
        10         :         00110100;
        11         :         01010110;         --st r6, r1
        12         :         00000001;
        13         :         00001001;         --mv   r1, #52
        14         :         00110100;
        15         :         01000001;         --ld    r1, r1
        16         :         00000001;
        17         :         00000111;         --mv r7, r1
        18         :         00000001;
        19         :         11110100;         --out 00
        20         :         11111111;         --halt
        50         :         00001100;         --data 50, #12
END;
```

7. Demonstration

According to the program above and the value of SW = 000001000 = 8, the expected output R0 = R1 = $96_{10} = 060_{16}$ = LED = 001100000_2



Multiplying by traditional method



Multiplying using logic gates

8. Conclusion

The processor is way better than the 9-bit processor with larger address width, more specialized instructions. But the tradeoff is the time spent, since most of instructions need two consecutive inputs.

IV Conclusion

Each processor has its own pros and cons. The 9-bit one can perform faster, but in return, it lack of instructions, small address width. Although the 8-bit processor is slower, it can be widely used thanks to a large set of instructions and the ability to handle large memory.

All of the source code of this subject will be upload on my Github repository, `https://github.com/superzeldalink/Digital-Systems-Lab-HCMUT-212`.

References

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