ICLAB 2023-Fall Midterm Project
AXI4 Introduction

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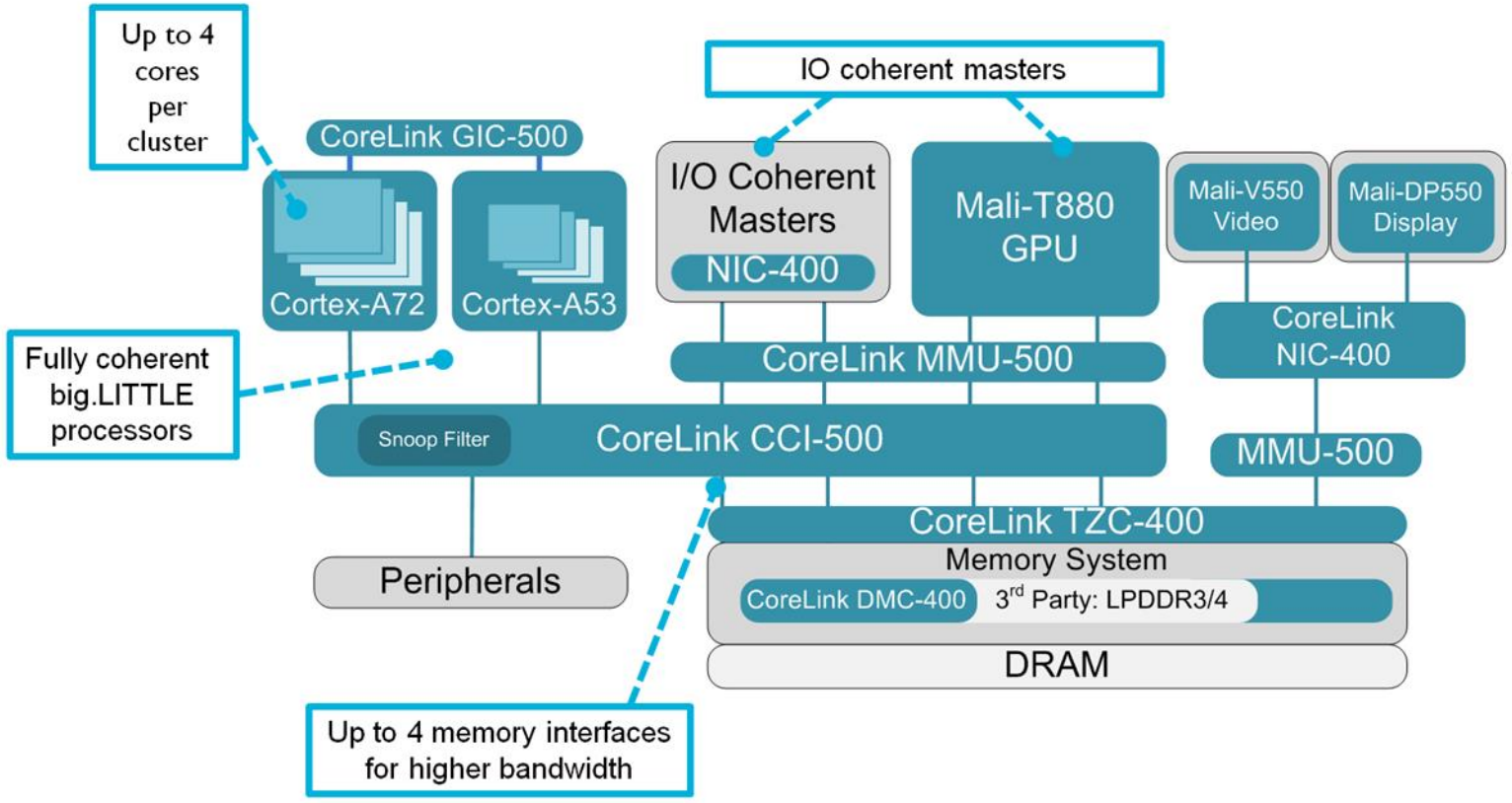
Outline

- **AMBA Brief History**
- **AXI 4 Introduction**
  - Handshake Process
  - AXI Signal Description in Midterm Project

AMBA Brief History

AMBA (Advanced Microcontroller Bus Architecture)

What is Bus Architecture ?



What is Bus Architecture ?

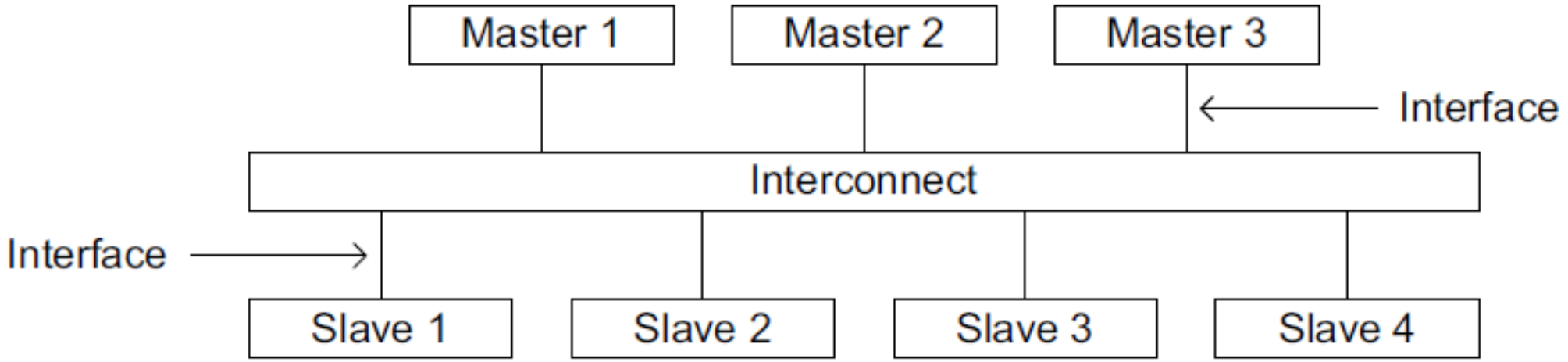


Figure A1-3 Interface and interconnect

AMBA

Evolution of the AMBA protocol family - Overview

AMBA 1
(ARM7)

1996

ASB™

- Only a single master can be active at a time
- Data element and burst transfers
- Bi-directional data bus
- Using both clock edges

AMBA 2
(ARM7/9)

5/1999

AHB™

- Split transactions with overlapping address and data phases of multiple masters
  Three stage pipelining
- Wider data bus options
- Using only uni-directional signals
- Using only the rising edge

AMBA 3
(ARM11, Cortex-A8/A9/A5)

6/2003

AXI3

- **Complete redesign**
- Burst based transactions
- Channel concept with 5 channels for reads and writes
- **Out-of-order transactions**
- Optional signaling for **low power operation**
- **Non-cache-coherent interconnects**

Main Focus
3/2010

AXI4

- Burst lengths of up to 256 beats
- **Quality of Service signaling (QoS)**

AMBA 4
(Cortex-A15/A7 ARM big.LITTLE)

10/2011

ACE™

Extension of the AXI4 i.f. by **3 channels to provide system wide cache coherency**

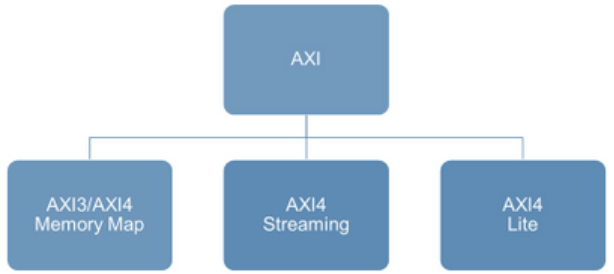
- Supporting both full and I/O coherency
- Coherency domains
- Memory barrier transactions
- Support of DVM (Distributed Virtual Memory)
- Snoop filters
- Cache coherent interconnects

AMBA 5
(Cortex A57/A53/A72/A35)

6/2013

CHI

- **Complete redesign**
- Layered architecture
- **Non blocking packet-based bus**
- Support of L3 Cache
- New node names



1995 — 2000 — 2010 — 2013

Ref [1]

AXI 4 Introduction

Handshake Process

2+3 Channel

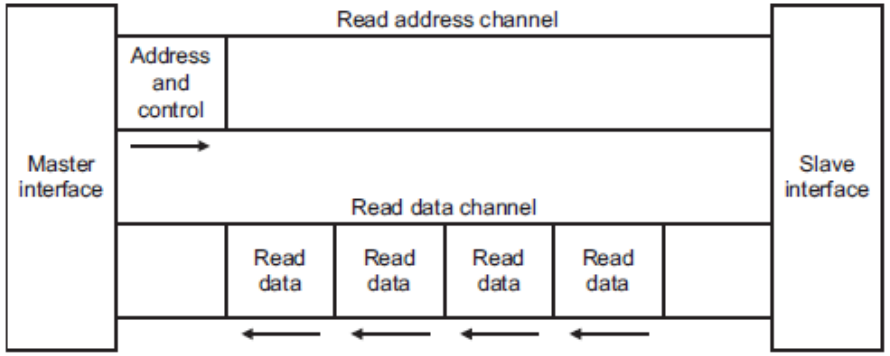
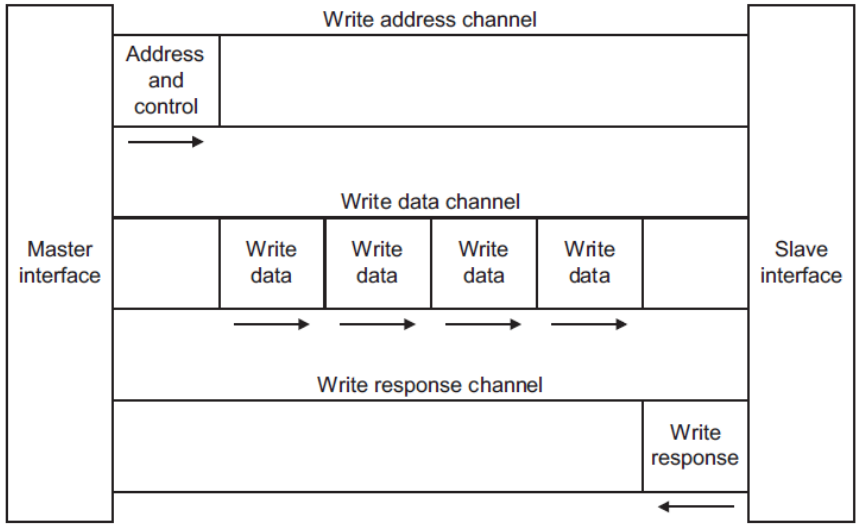
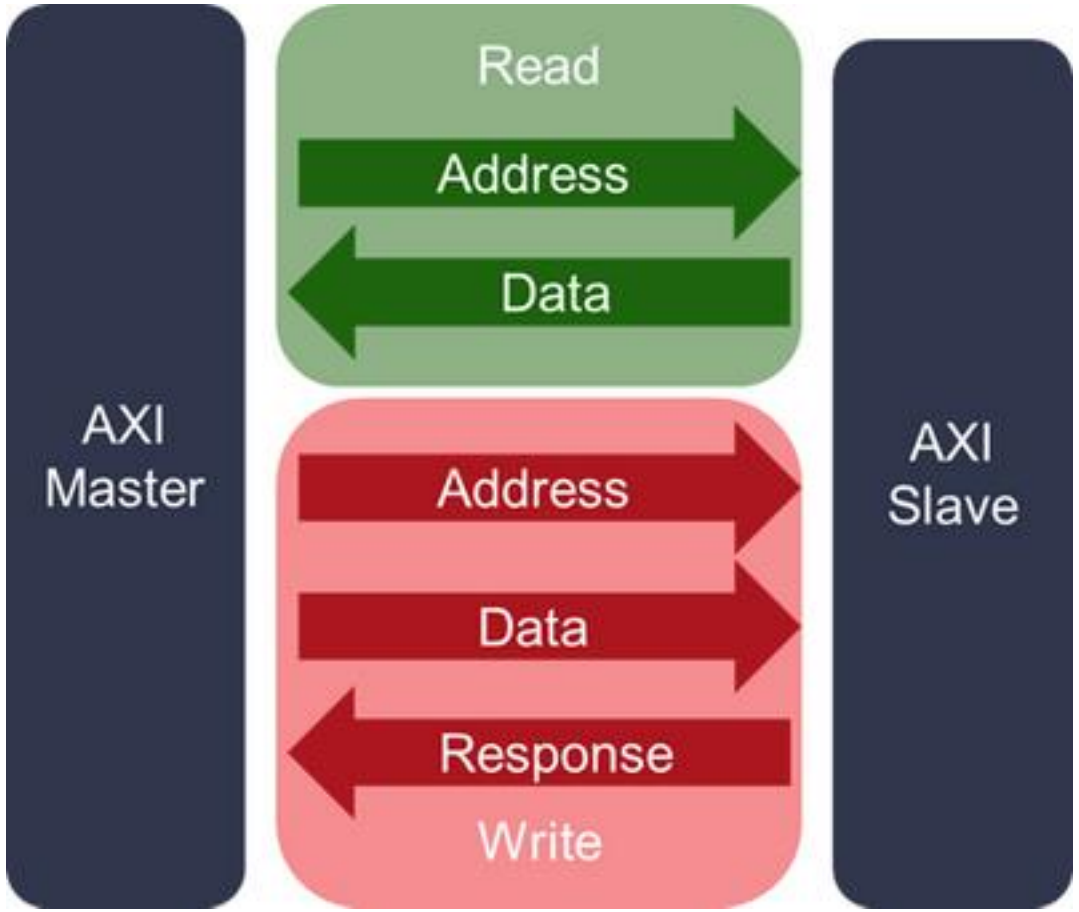


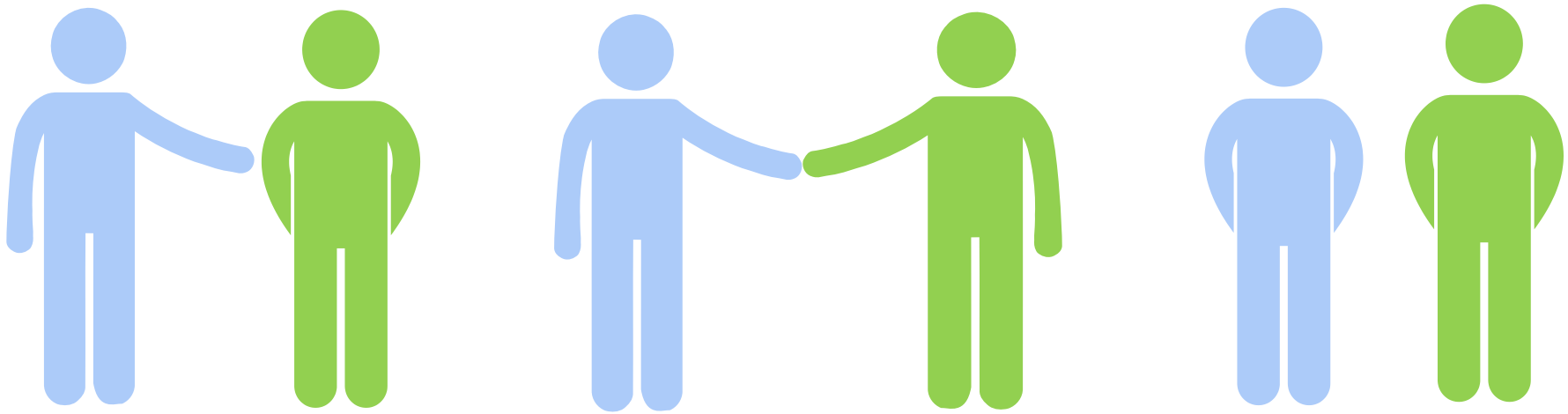
Figure 1-1 Channel architecture of reads





Handshake Process Scenario 1

- **Slave: Valid** **Master: Ready**



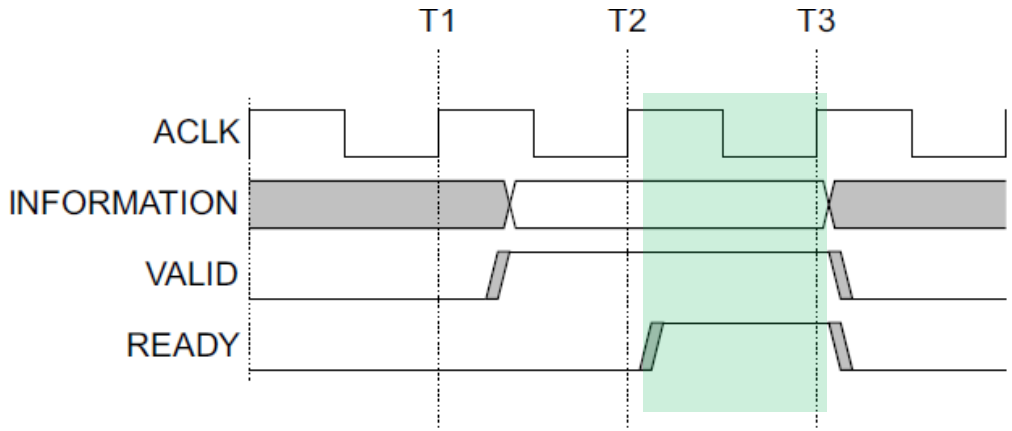
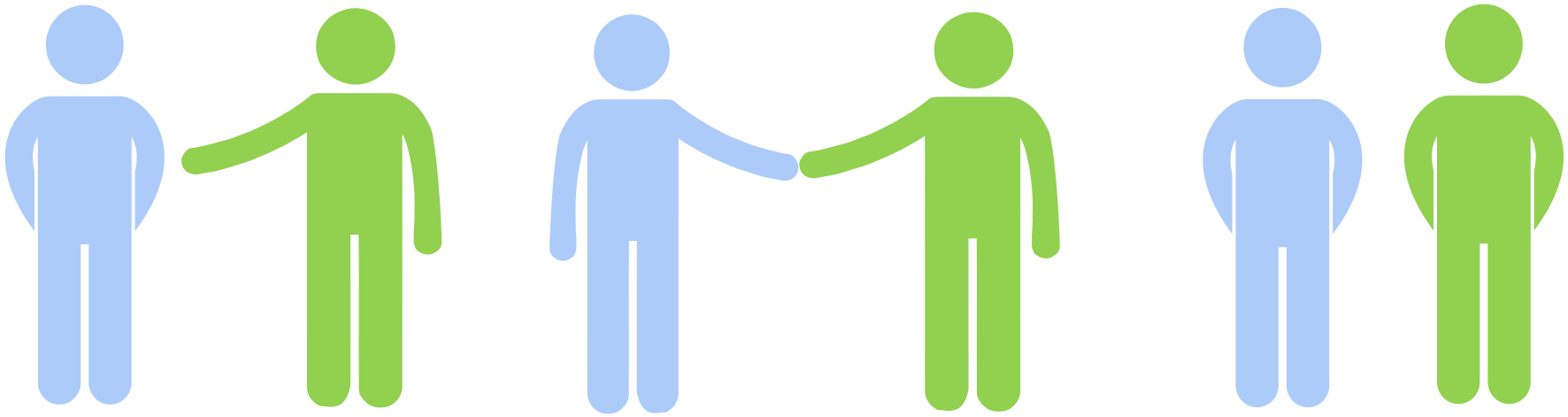


Figure A3-2 VALID before READY handshake

Handshake Process Scenario 2

- **Slave: Valid** **Master: Ready**



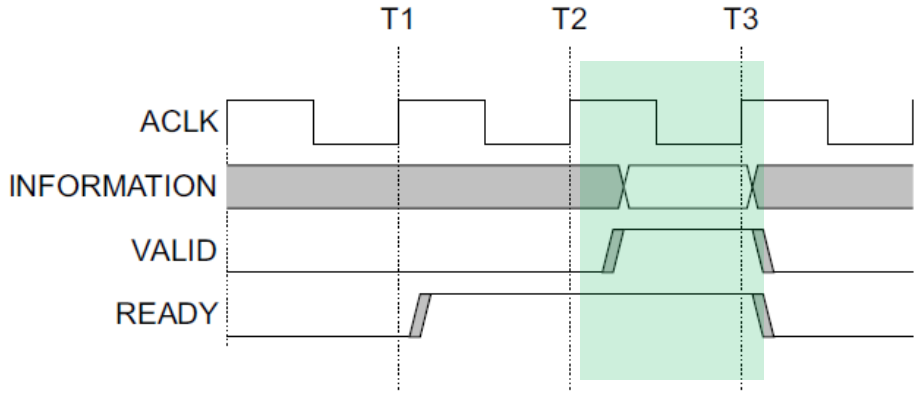
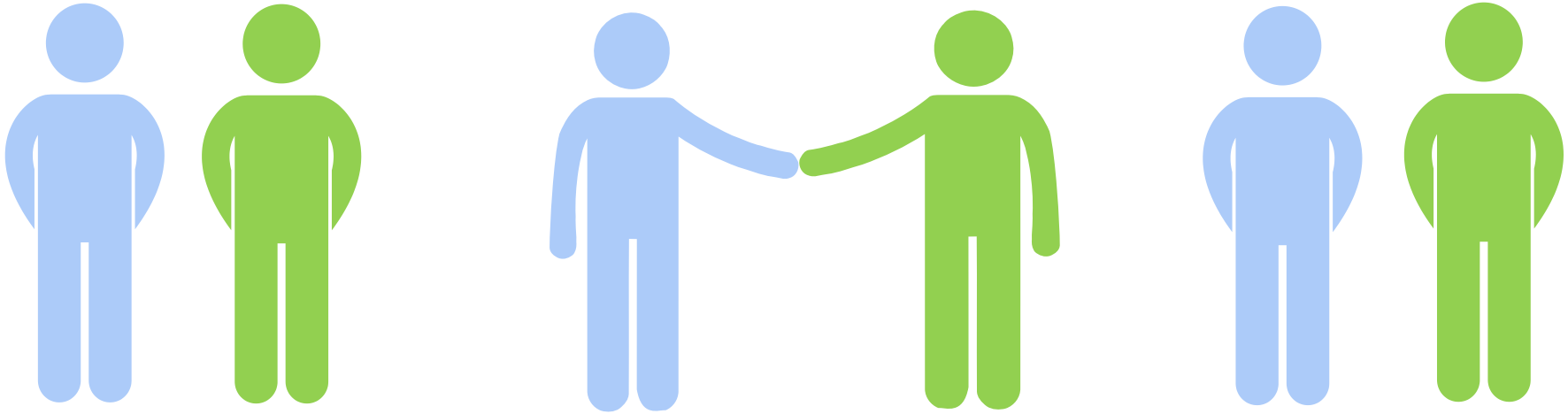


Figure A3-3 READY before VALID handshake

Handshake Process Scenario 3

- **Slave: Valid** **Master: Ready**



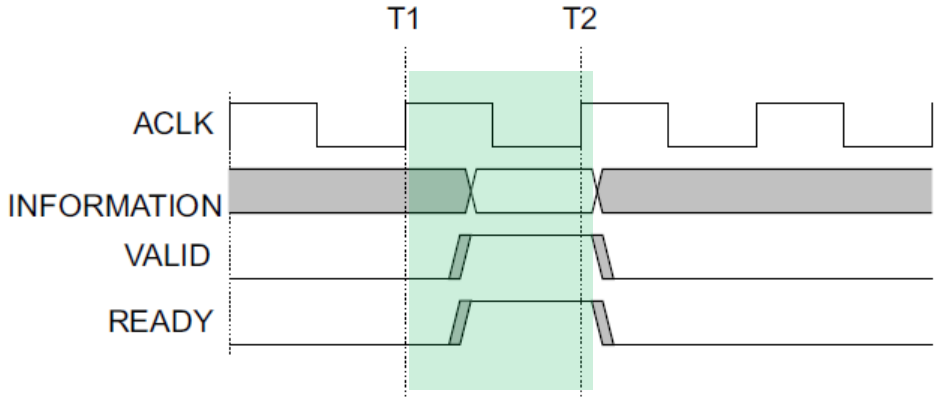


Figure A3-4 VALID with READY handshake

Handshake Dependencies

- The VALID signal of one AXI component must be independent on the READY signal of the other component in the transaction. (prevent deadlock)
- The READY signal can wait for assertion of the VALID signal.

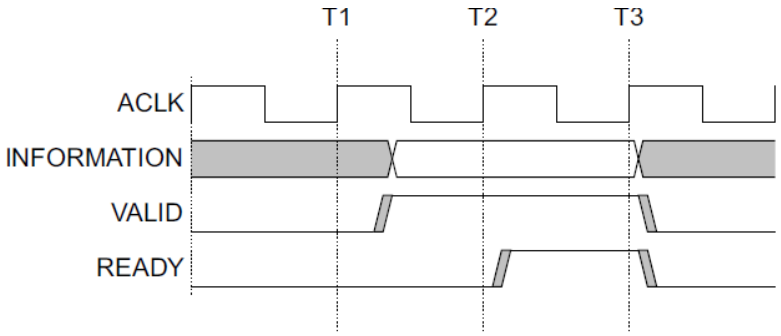


Figure A3-2 VALID before READY handshake

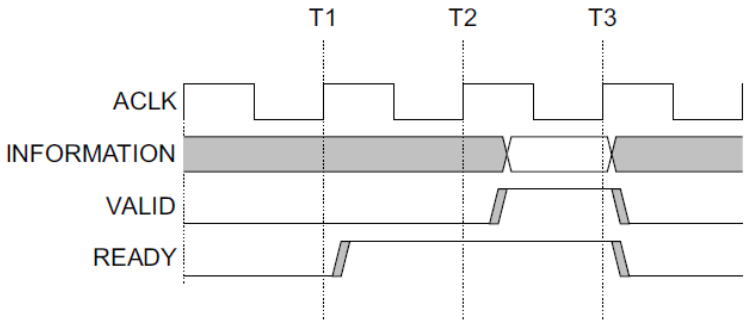


Figure A3-3 READY before VALID handshake

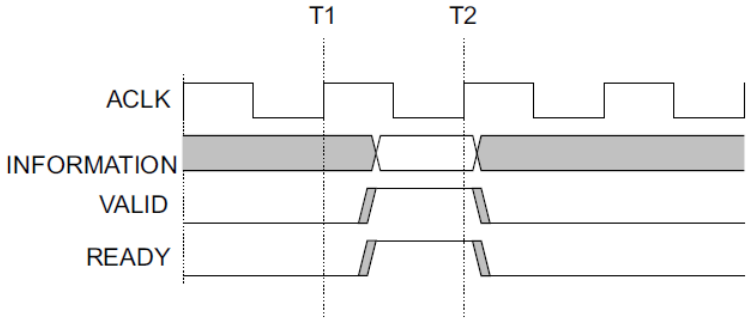


Figure A3-4 VALID with READY handshake

2+3 Channel

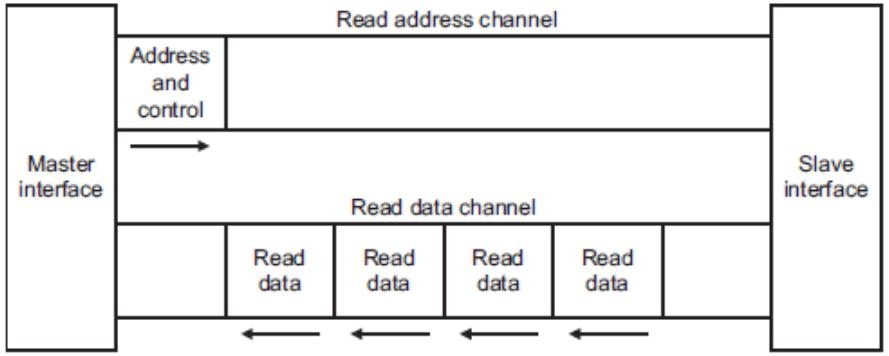


Figure 1-1 Channel architecture of reads

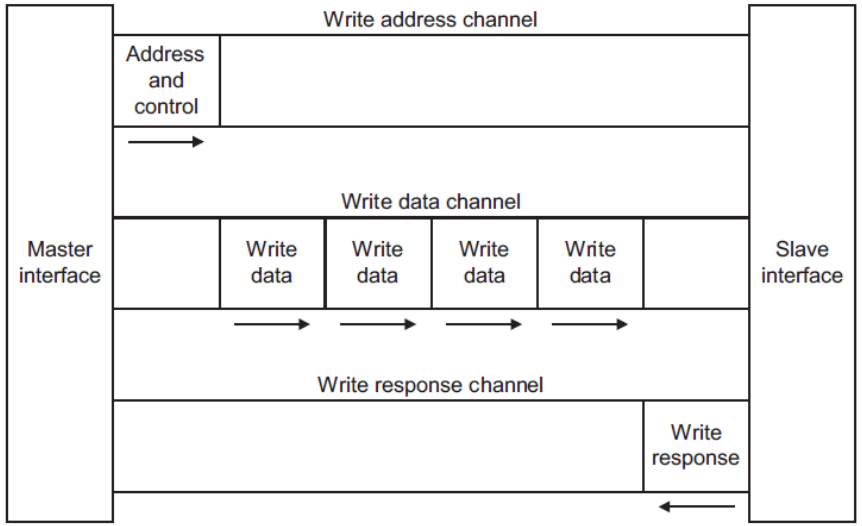


Table A3-1 Transaction channel handshake pairs

Transaction channel	Handshake pair
Write address channel	**AWVALID, AWREADY**
Write data channel	**WVALID, WREADY**
Write response channel	**BVALID, BREADY**
Read address channel	**ARVALID, ARREADY**
Read data channel	**RVALID, RREADY**

Table A3-1 Transaction channel handshake pairs

Transaction channel	Handshake pair
Write address channel	**AWVALID, AWREADY**
Write data channel	**WVALID, WREADY**
Write response channel	**BVALID, BREADY**
Read address channel	**ARVALID, ARREADY**
Read data channel	**RVALID, RREADY**

AXI 4 Introduction

AXI Signal Description(in this project)

AXI -- Burst-Based Protocol

- **AXI Transaction：the complete set of required operations on the AXI bus form the AXI Transaction**
- **AXI Burst：any required payload data is transferred as an AXI Burst**
- **AXI Beats：a burst can comprise multiple data transfers, or AXI Beats**
  - AXI Transaction =M*AXI Burst ,M >= 1
    AXI Burst = N * AXI Transfer（AXI beat） ,N >= 1
    Burst_Length(N) = AxLEN[7:0]+1 ;

Table A3-3 Burst type encoding

AxBURST[1:0]	Burst type
0b00	FIXED
0b01	INCR
0b10	WRAP
0b11	Reserved

Table A3-2 Burst size encoding

AxSIZE[2:0]	Bytes in transfer
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

ARLEN	Master	Burst length. This signal indicates the exact number of transfers in a burst. This changes between AXI3 and AXI4. See *Burst length* on page A3-44.
ARSIZE	Master	Burst size. This signal indicates the size of each transfer in the burst. See *Burst size* on page A3-45.
ARBURST	Master	Burst type. The burst type and the size information determine how the address in each transfer within the burst is calculated. See *Burst type* on page A3-45.

AXI 4 Basic Transaction

Read Transaction

- Read Address Channel
- Read Data Channel

$$Address_i = StartAddress + i \cdot TransferSize$$

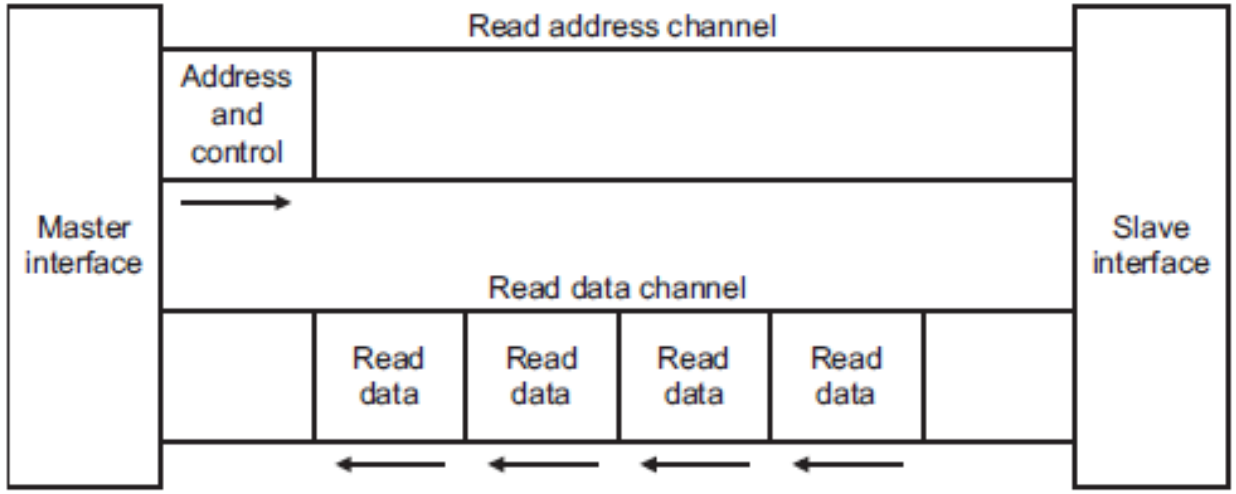


Figure 1-1 Channel architecture of reads

Each channel have valid-ready pair for handshaking process

Ref [2]

AXI 4 Basic Transaction

Write Transaction

- Write Address Channel
- Write Data Channel
- Write Response Channel

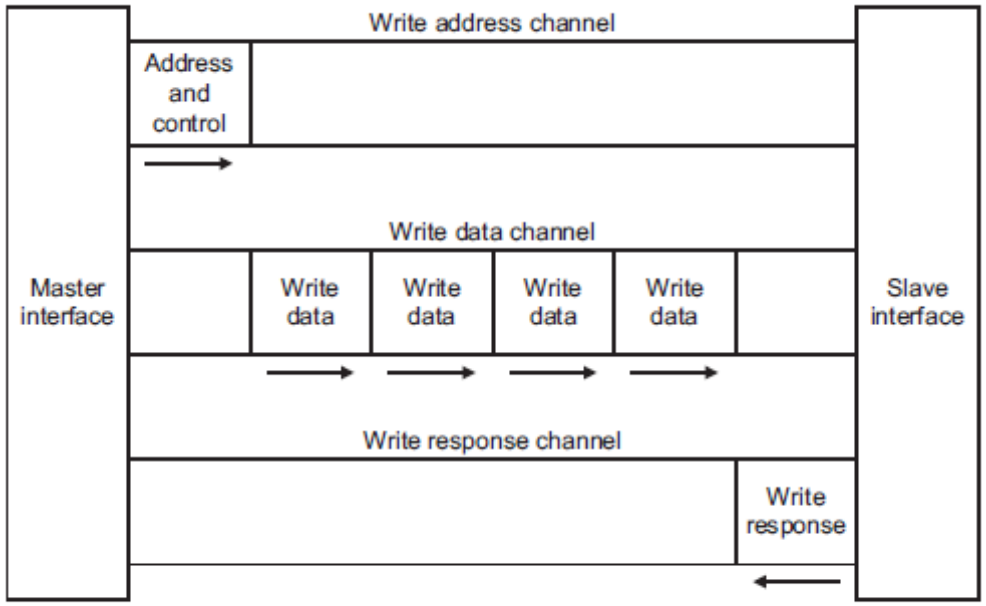


Figure 1-2 Channel architecture of writes

Each channel have valid-ready pair for handshaking process

Ref [2]

Global Signals

Signal	Source	Description
clk	Clock source	Global clock signal. All signals are sampled on the rising edge of the global clock.
rst_n	Reset source	Global reset signal. This signal is active LOW.

Write Address Channel

Signal	Source	Description
AWID[3:0]	Master	Write address ID. This signal is the identification tag for the write address group of signals. (In this project, we only use this to recognize master, reordering method is not supported)
AWADDR[31:0]	Master	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst transaction.
AWLEN[7:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
AWSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. (We only support 3b'100 which is 16 Bytes (matched with Data Bus-width) in each transfer)
AWBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. (only INCR(2'b01) support in this Project)
AWVALID	Master	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, **AWREADY**, goes HIGH.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

Write Data Channel

Signal	Source	Description
WDATA	Master	Write data. The write data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide. (This project only support 128-bit data width: WDATA[127:0])
WLAST	Master	Write last. This signal indicates the last transfer in a write burst.
WVALID	Master	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available 0 = write data and strobes not available.
WREADY	Slave	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready 0 = slave not ready.

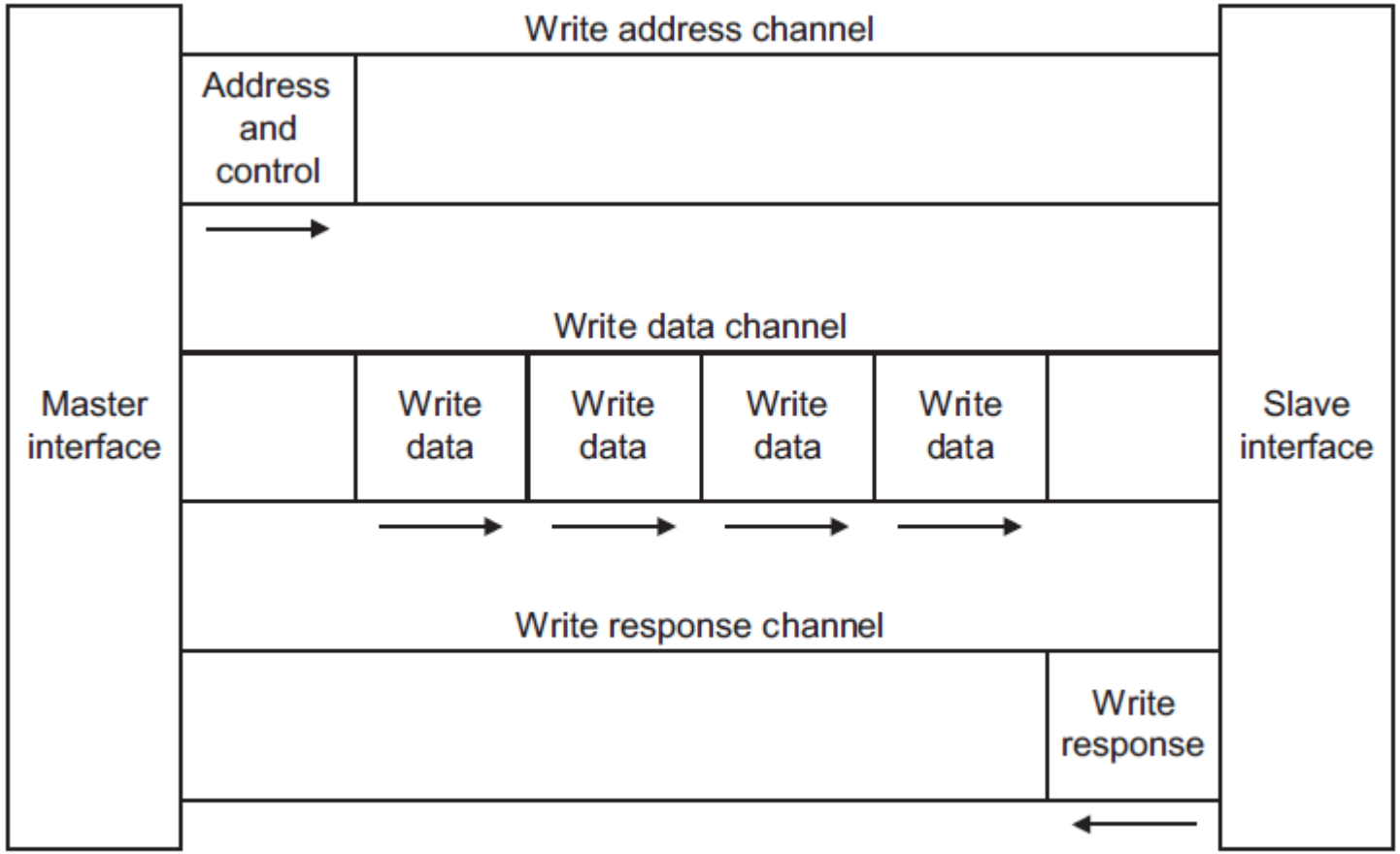
Write Response Channel

Signal	Source	Description
BID[3:0]	Slave	Response ID. The identification tag of the write response. The **BID** value must match the **AWID** value of the write transaction to which the slave is responding.
BRESP[1:0]	Slave	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (In this project we only issue OKAY(2'b00))
BVALID	Slave	Write response valid. This signal indicates that a valid write response is available: 1 = write response available. 0 = write response not available.
BREADY	Master	Response ready. This signal indicates that the master can accept the response information. 1 = master ready. 0 = master not ready.

Table A3-4 RRESP and BRESP encoding

RRESP[1:0] BRESP[1:0]	Response
0b00	OKAY
0b01	EXOKAY
0b10	SLVERR
0b11	DECERR

Write Transaction



Waveform of Write Transaction

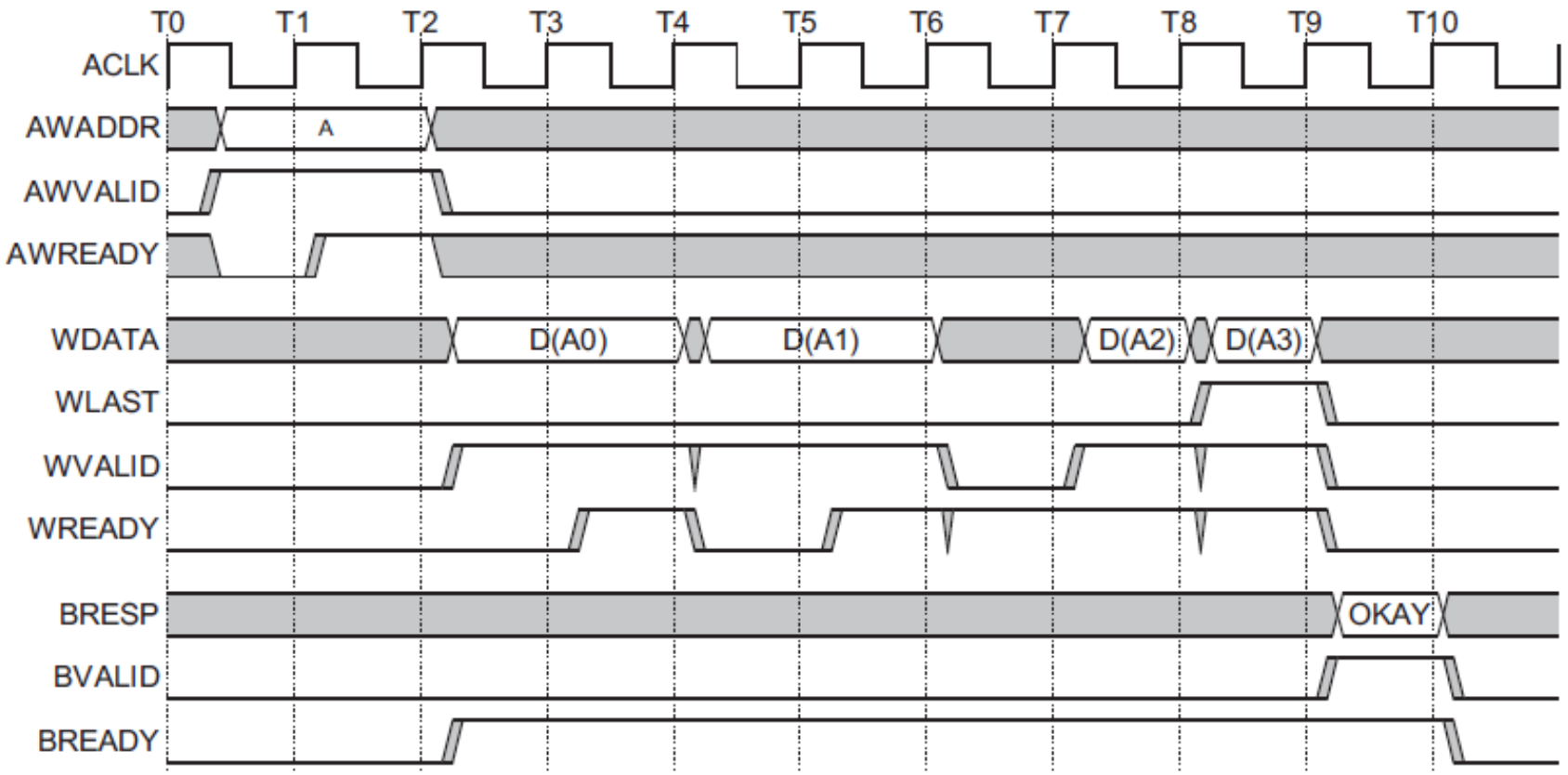


Figure 1-6 Write burst

Read Address Channel

Signal	Source	Description
ARID[3:0]	Master	Read address ID. This signal is the identification tag for the read address group of signals. (In this project, we only use this to recognize master, reordering method is not supported)
ARADDR[31:0]	Master	Read address. The read address gives the address of the first transfer in a read burst transaction.
ARLEN[7:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
ARSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. (We only support 3b'100 which is 16 Bytes (matched with Data Bus-width) in each transfer)
ARBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. (only INCR: 2b'01 support in this Project)
ARVALID	Master	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledge signal, **ARREADY**, is high. 1 = address and control information valid 0 = address and control information not valid.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

Read Data Channel

Signal	Source	Description
RID[3:0]	Slave	Read ID tag. This signal is the ID tag of the read data group of signals. The **RID** value is generated by the slave and must match the **ARID** value of the read transaction to which it is responding.
RDATA	Slave	Read data. (This project only support 128 bit data width: RDATA[127:0])
RRESP[1:0]	Slave	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (In this project we only issue OKAY)
RLAST	Slave	Read last. This signal indicates the last transfer in a read burst.
RVALID	Slave	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available 0 = read data not available.
RREADY	Master	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready 0 = master not ready.

Read Transaction

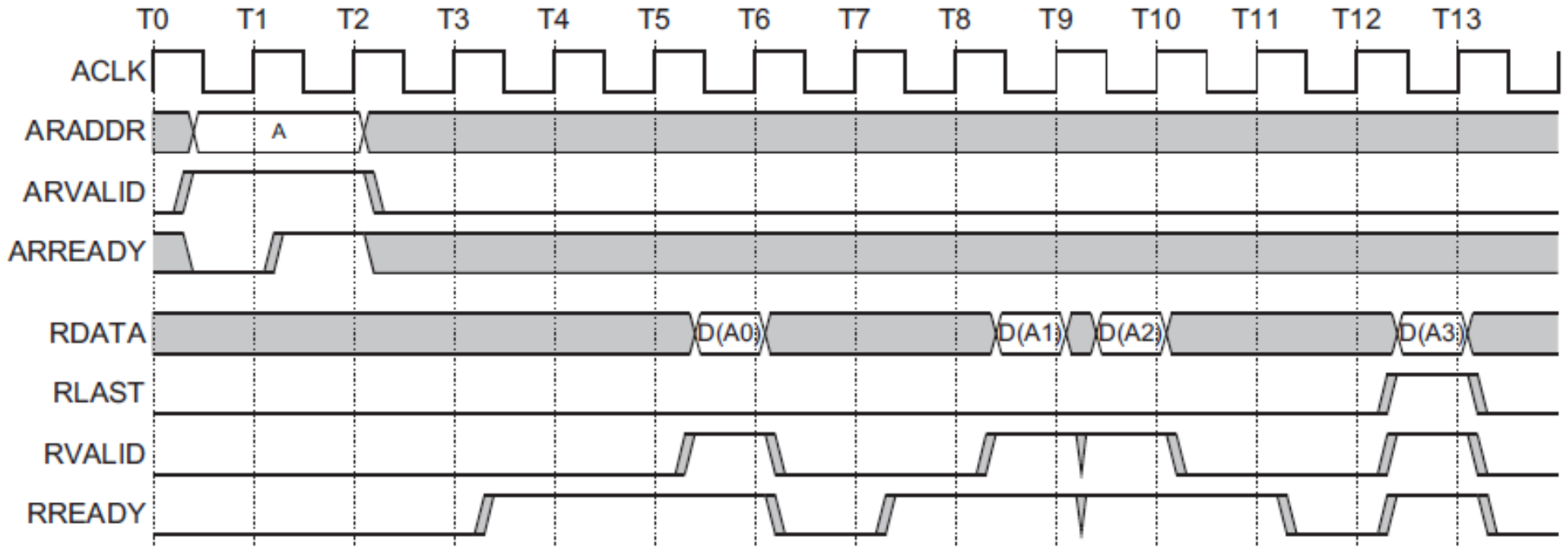


Figure 1-4 Read burst

Ref

- https://en.wikipedia.org/wiki/Advanced_eXtensible_Interface
- http://www.gstitt.ece.ufl.edu/courses/fall15/eel4720_5721/labs/refs/AXI4_specification.pdf

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