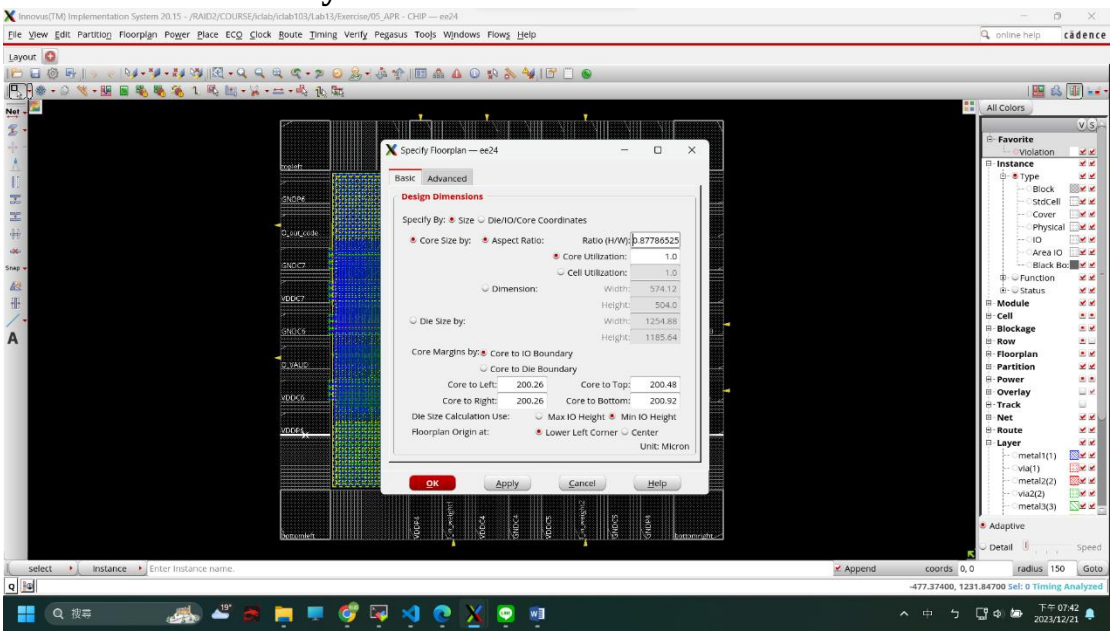
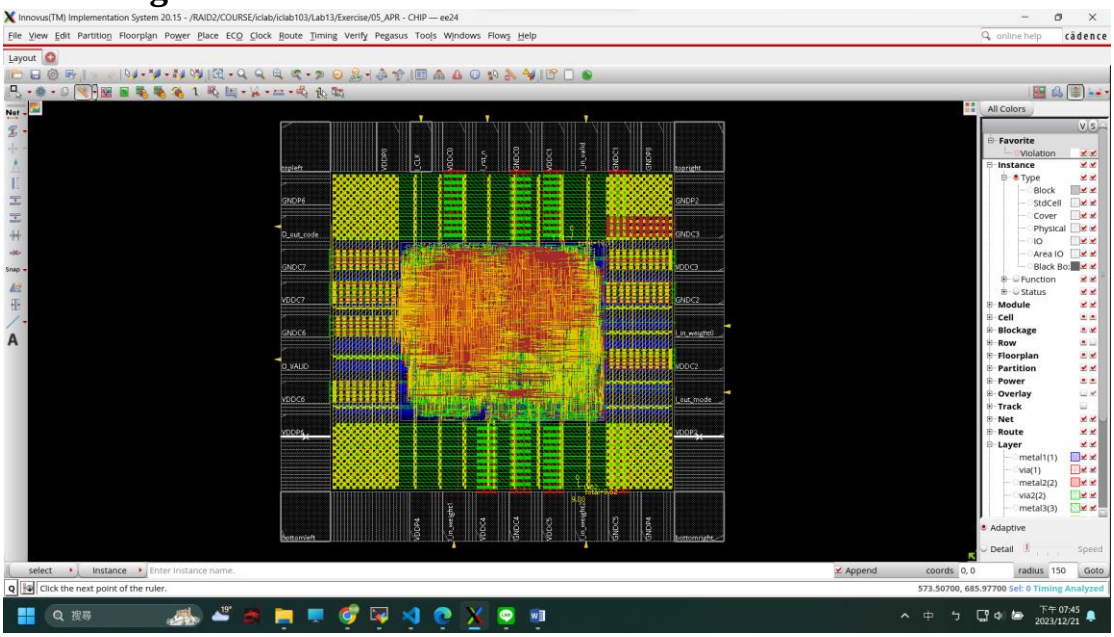
Report

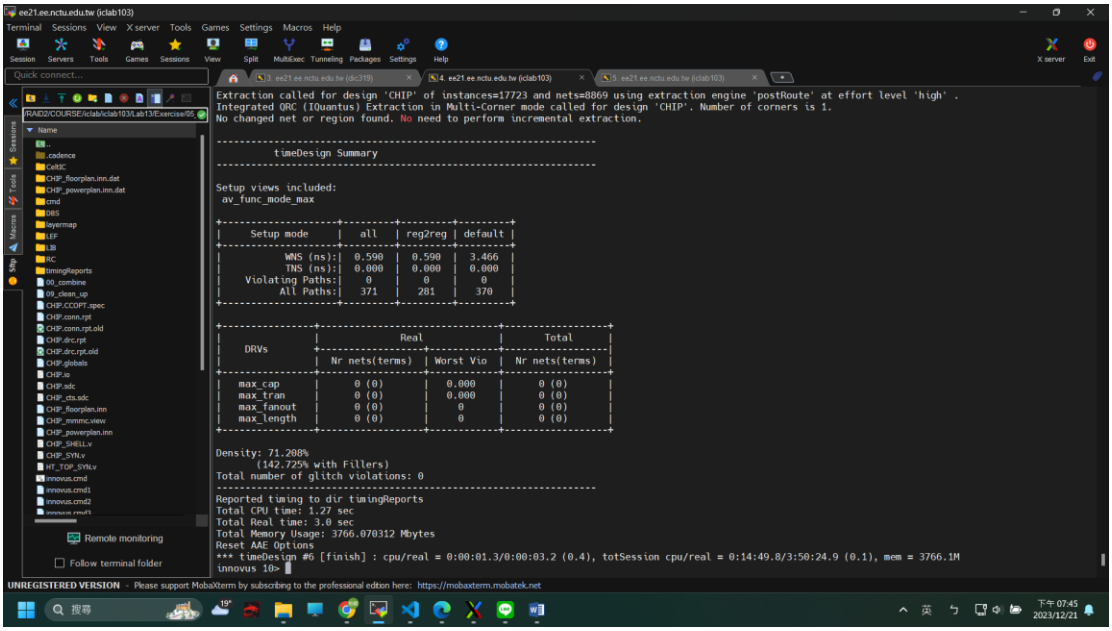
1. Core to IO boundary :



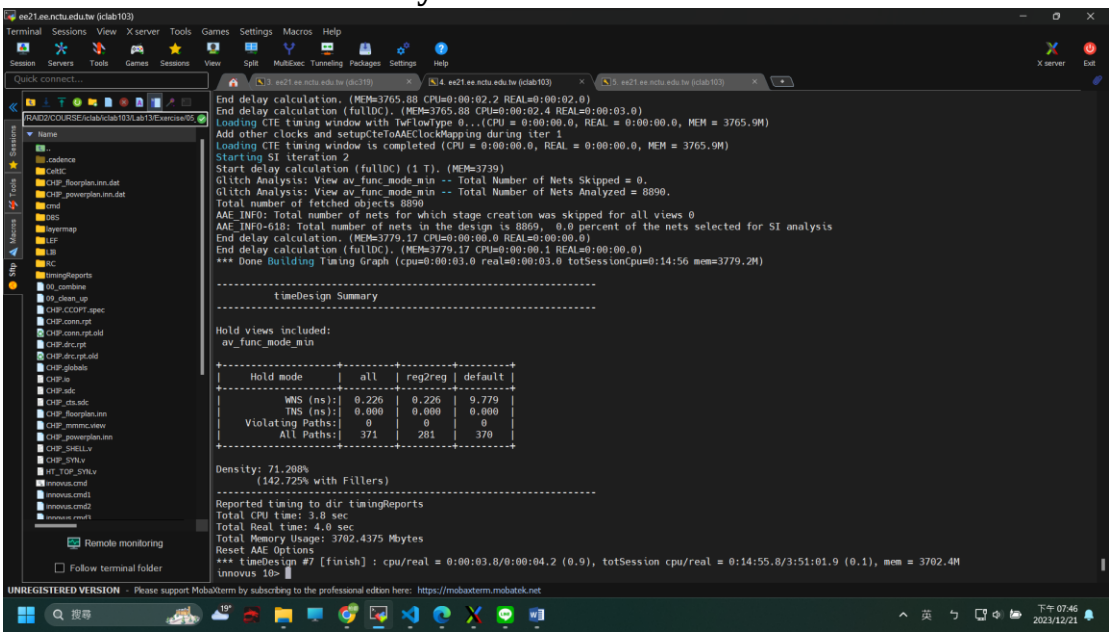
2. Core Ring :



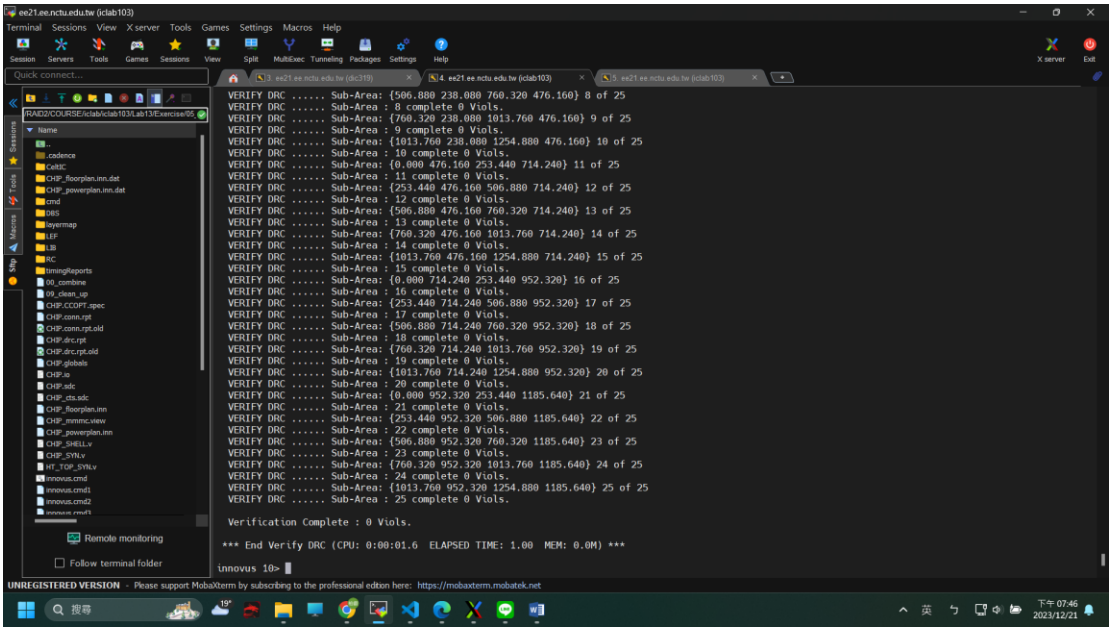
3. Post-Route setup time analysis :



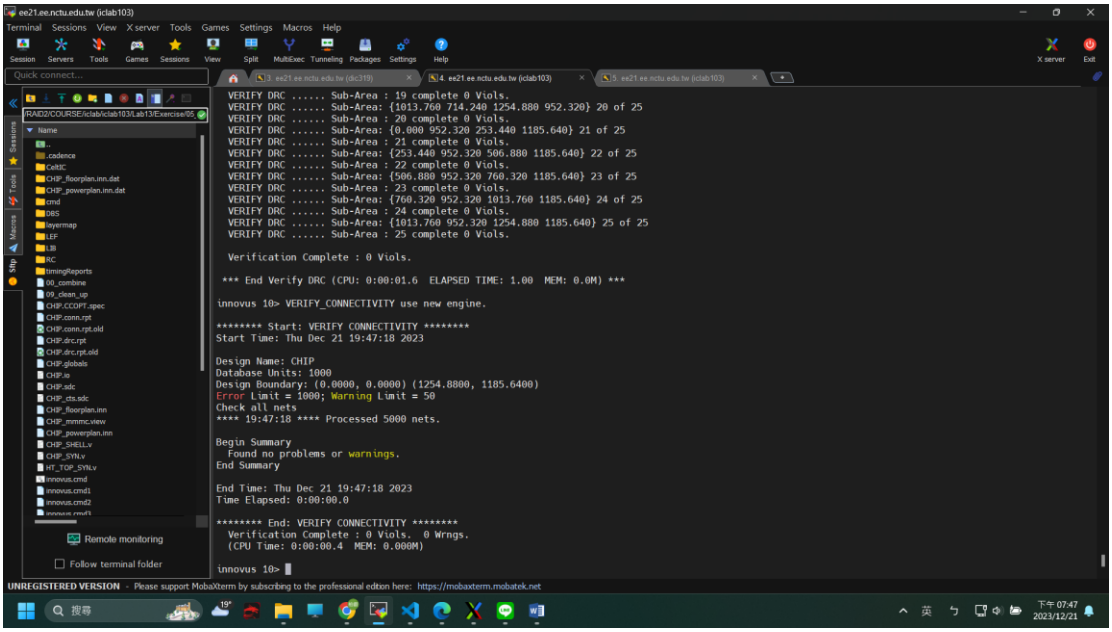
4. Post-Route hold time analysis :



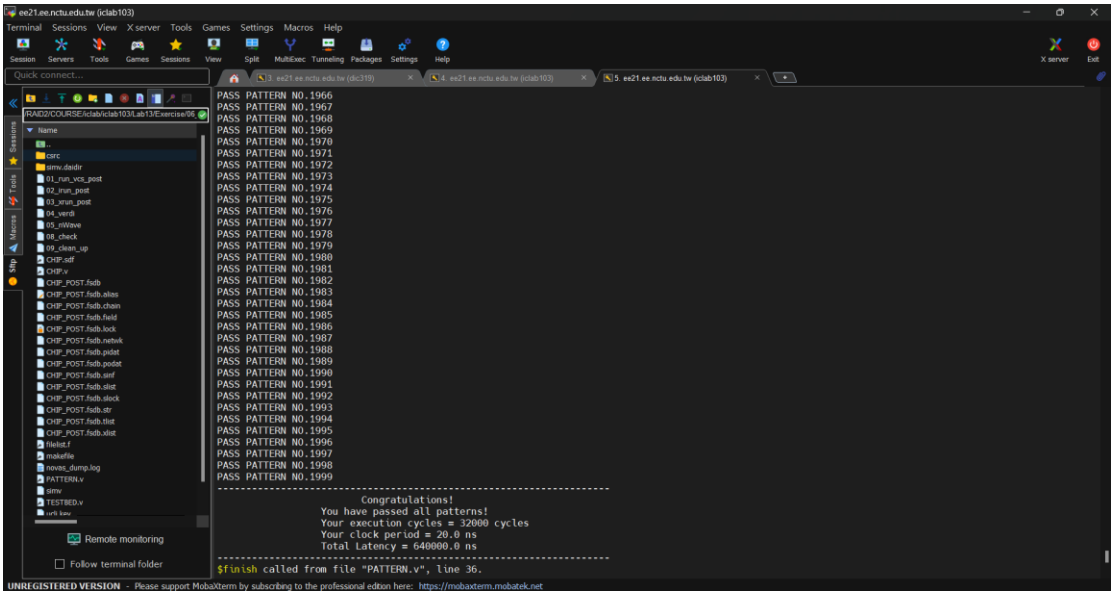
5. DRC result :



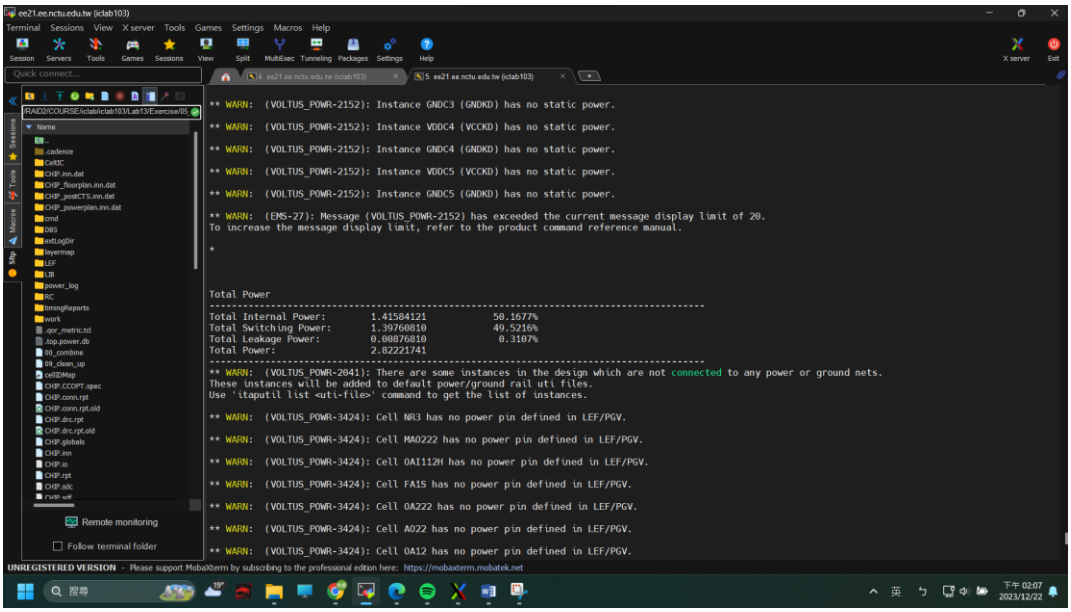
6. LVS result :



7. Post Layout simulation result :

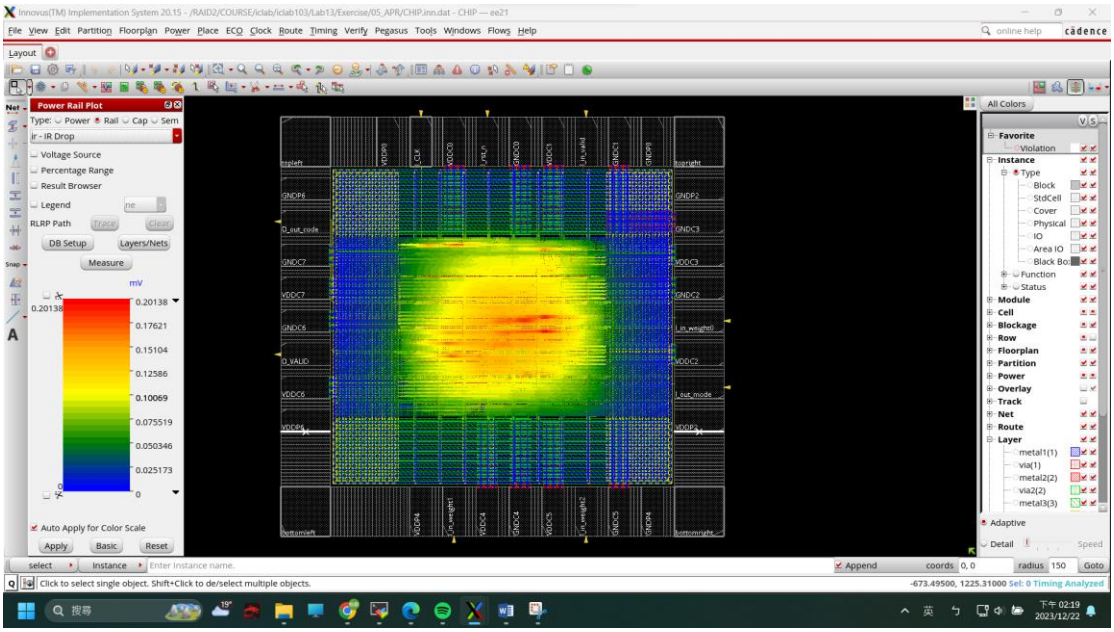


8. Power result :



9. IR Drop Results :

把utilization調小，調到50%，多加一點core power pad，每邊各兩組，共8組core power pad，Stripe的數量調多。


Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/iclab/iclab103/Lab13/Exercise/05_APR/CHIP.inn.dat - CHIP — ee21
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
online help
cadence
Layout
Power Rail Plot
Type: Power Rail Cap Sem
IR - IR Drop
Voltage Source
Percentage Range
Result Browser
Legend
RLRP Path
Trace
Clear
DB Setup
Layers/Nets
Measure
mV
0.20138
0.17621
0.15104
0.12586
0.10069
0.075519
0.050346
0.025173
0
Auto Apply for Color Scale
Apply
Basic
Reset
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
metal1(1)
via(1)
metal2(2)
via2(2)
metal3(3)
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
-673.49500, 1225.31000 Sel: 0 Timing Analyzed
搜尋
下午 02:19
2023/12/22