```
; **** USART Module : Polling Transmission
;=================================================
; DEFINITIONS
;=================================================
        PROCESSOR PIC16F628
        #include <P16F628.INC>
        __CONFIG    _CP_OFF & _MCLRE_ON & INTRC_OSC_NOCLKOUT & _LVP_OFF
        & _WDT_OFF
#define NL  0x0A    ; New Line
#define FF  0x0C    ; Form feed
#define CR  0x0D    ; Carriage return

;=================================================
; VARAIBLES
;=================================================
        cblock  0x20
            count
            count0
            count1
            count2
            temp
            buffer
            index
        endc
;=================================================
; RESET and INTERRUPT VECTORS
;=================================================
        ORG     0x00
        goto    main
        ORG     0x04
        retfie

Main:   call    init
Message_loop:
        movlw   0x00
        movwf   index
        call    send_message

        movlw   .250
        call    DelaymS

        goto    Message_loop

; this subroutine sends a string of many characters from a look-up table
'message'
send_message:
        movf    index,w
        call    message     ; get character from the message table
        movwf   buffer
        movlw   0xFF
        subwf   buffer,w    ; check if we are at the end of message?
        btfsc   STATUS,Z
        return
        incf    index,f
TX:     btfss   PIR1,TXIF   ; TXIF='1' if the TXREG is empty
        goto    TX
        movf    buffer,w
        movwf   TXREG
        goto    send_message ; go back and do it again

message:
        addwf   PCL,f
        DT      NL,"EEGE 380 Microprocessors",NL,CR
        DT      "Learning PIC16F628 is fun :=)",NL,CR,0xFF

init:
        ;Initialization of USART module
        banksel CMCON
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67          movlw   .7
68          movwf   CMCON   ; disable analog comparator
69          banksel TRISA
70          movlw   0x00
71          movwf   TRISA
72  ; Bits 1 and 2 of Port B are multiplexed as TX/CK and RX/DT for USART
    operation.
73  ; These bits must be set to input in the TRISB register.
74          bcf     TRISB,2 ; RB2 as output (Tx pin)
75          bsf     TRISB,1 ; RB1 as input (Rx pin)
76
77  ; The asynchronous baud rate(ABR) is calculated as follows:
78  ;   ABR = Fosc/{S*(x+1)}
79  ; x is value in SPBRG register.
80  ; S is 64 if high baud rate select bit(BRGH) in the TXSTA control register
    is clear (slow-speed baud rate).
81  ; S is 16 if the  BRGH bit is set (high-speed baud rate).
82  ; For setting to 9600 baud rate using a 4MHz oscillator at a high-speed
    baud rate the formula is:
83  ; At high speed (BRGH=1)
84  ; 9600 = 4,000,000/{16*(x+1)}
85  ; x = 25.041 -> use x=25
86  ; calculate baud rate from x=25 to find %error
87  ; baud rate = 4,000,000/{16*(25+1)} = 9,615 (0.16% error)
88  ; At slow speed (BRGH=0)
89  ; baud rate = 4,000,000/{64*(25+1)} = 2,403.85 (0.16% error)
90  ;
91
92          banksel SPBRG
93          movlw   .25     ; 2400 baud rate at 4MHz crystal
94          movwf   SPBRG   ; Place in baud rate generator
95  ; TXSTA (Transmit Status and Control Register) bit map:
96  ;   7   6   5   4   3   2   1   0   <== bits
97  ;   |   |   |   |   |   |   |   |______ Tx9D 9nth data bit on
98  ;   |   |   |   |   |   |   |           (used for parity)
99  ;   |   |   |   |   |   |   |__________ TRMT Transmit Shift Register
100 ;   |   |   |   |   |   |               1 = TSR empty
101 ;   |   |   |   |   |   |             * 0 = TSR full
102 ;   |   |   |   |   |   |_____________ BRGH High Speed Baud Rate
103 ;   |   |   |   |   |                   (Asynchronous mode only)
104 ;   |   |   |   |   |                   1 = high speed (*4)
105 ;   |   |   |   |   |                 * 0 = low speed
106 ;   |   |   |   |   |_________________ NOT USED
107 ;   |   |   |   |_____________________ SYNC USART Mode Select
108 ;   |   |   |                         1 = synchronous mode
109 ;   |   |   |                       * 0 = asynchronous mode
110 ;   |   |   |_________________________ TXEN Transmit Enable
111 ;   |   |                           * 1 = transmit enable
112 ;   |   |                             0 = transmit disable
113 ;   |   |_____________________________ TX9 Enable 9-bit Transmit
114 ;   |                                 1 = 9-bit transmission mode
115 ;   |                               * 0 = 8-bit mode
116 ;   |_______________________________ CSRC Clock Source Select
117 ;                                     Not used in asynchronous mode
118 ;                                     Synchronous mode:
119 ;                                        1 = Master Mode (internal clock)
120 ;                                      * 0 = Slave Mode (external clock)
121 ; Setup value = 0010 0000 = 0x20
122         banksel TXSTA   ; TXEN = '1', BRGH = '0'
123         movlw   0x20    ; Enable transmission and low speed baud rate
124         movwf   TXSTA
125 ; RCSTA (Receive Status and Control Register) bit map:
126 ;   7   6   5   4   3   2   1   0   <== bits
127 ;   |   |   |   |   |   |   |   |______ RX9D 9th data bit received
128 ;   |   |   |   |   |   |   |           (can be parity parity)
129 ;   |   |   |   |   |   |   |__________ OERR Overrun error
130 ;   |   |   |   |   |   |               1 = error clear by software
131 ;   |   |   |   |   |   |_____________ FERR Framing error
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;    |   |   |   |   |                  1 = error
;    |   |   |   |   |_____________ NOT USED
;    |   |   |   |_________________ CREN Continuous Receive Enable
;    |   |   |                        Asynchronous mode
;    |   |   |                         * 1 = Enable continuous receive
;    |   |   |                           0 = Disable continuous receive
;    |   |   |                        Synchronous mode
;    |   |   |                           1 = Enables until CREN cleared
;    |   |   |                           0 = Disables continuous receive
;    |   |   |_____________________ SREN Single Receiver Enable
;    |   |                            Asynchronous mode = don't care
;    |   |                            Synchronous mode
;    |   |                               1 = Enables single receiver
;    |   |                               0 = Disables single receiver
;    |   |_________________________ RX9  9-bit Receive Enable
;    |                              1 = 9-bit reception
;    |                             * 0 = 8-bit reception
;    |_____________________________ SPEN Serial Port Enable
;                                   * 1 = RX/DT and TX/CK are serial pins
;                                     0 = Serial port disable
; Setput value: 1001 0000 = 0x90
        banksel RCSTA   ; Bank 0
        movlw   0x90    ; Enable Serial port and continous reception
        movwf   RCSTA

        return

DelaymS:
        movwf   count2
        incf    count2,f
        decfsz  count2,f
        goto    $+2
        goto    $+3
        call    Delay1mS
        goto    $-4
        return

Delay1mS:
        movlw   .50         ; 1 cyc
        movwf   count1      ; 1 cyc
outterloop:
        movlw   .5          ; 1 cyc * count1
        nop                 ; 1 cyc * count1
        movwf   count0      ; 1 cyc * count1
innerloop:
        decfsz  count0,F    ; 1 cyc * count1 * count0
        goto    innerloop   ; 2 cyc * count1 * count0
        decfsz  count1,F    ; 1 cyc * count1
        goto    outterloop  ; 2 cyc * count1
        return              ; 1 cyc
        ; total = 3 + (6+3.count0).count1
        ; count0 = 5 , count1 = 50, total = 1053 cyc ??
;================================================
        END
```