EXPERIMENT NO: 04

Aim: Study and verification of the truth table of different logic gates.

Objectives:

i. Study of all gates and their pin description.
ii. Use of universal gate.

Apparatus Required: IC 7408 (AND Gate), IC 7432 (OR Gate), IC 7404 (NOT Gate), IC 7400 (NAND Gate), IC 7402 (NOR Gate), IC 7486(XOR Gate), Bread Board, Power Supply, Connecting Wires, LED.

Theory:

Objective: To verify truth table of all logic gates

Logic Gates: A logic gate is an elementary building block of a digital circuit. most logic gates have two inputs and one output. at any given moment, every terminal is in one of the two binary conditions: LOW (0) or HIGH (1), represented by different voltage levels. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).

AND, OR and NOT are basic gates. XOR and XNOR are derived gates. NAND and NOR gate are universal gatesas any logic can be implemented using only NAND or only NOR.

a) **AND Gate** gives logic 1 as output only if all of its inputs are at logic 1.

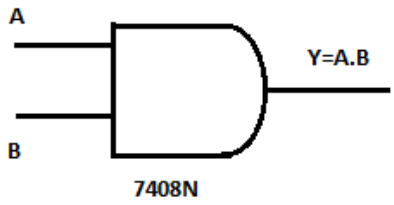

Figure 3.1: Symbol of AND gate

Truth Table of AND Gate:

A	B	A•B

0	0	0
0	1	0
1	0	0
1	1	1

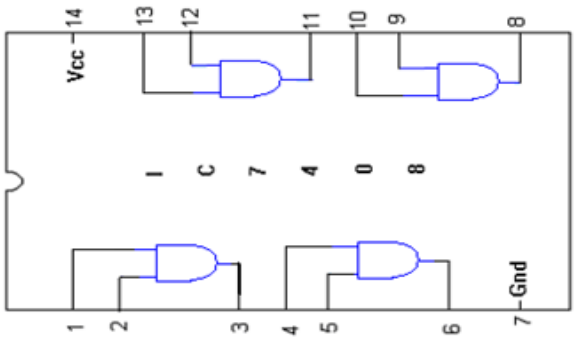

Figure 3.2: Pin Diagram of AND gate

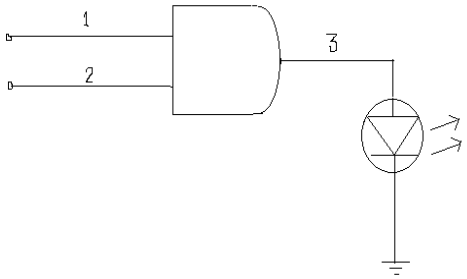

Figure 3.3: AND gate with LED as load

b) OR Gate gives logic 0 as output only if all of its inputs are at logic 0.

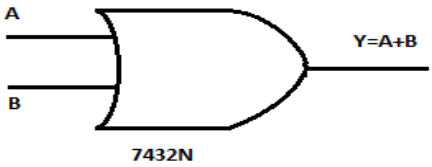

Figure 3.4: Symbol of OR gate

Truth Table of OR Gate:

A	B	A+B
0	0	0

0	1	1
1	0	1
1	1	1

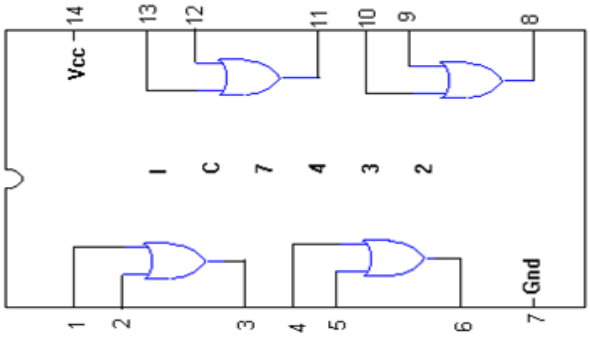

Figure 3.5: Pin Diagram of OR gate

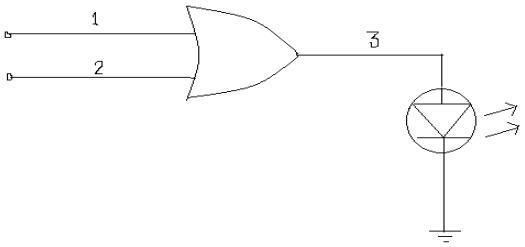

Figure 3.6: OR gate with LED as load

c) NOT Gate complements the input.

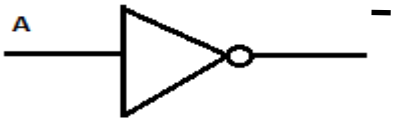

Figure 3.7: Symbol of NOT gate

Truth Table of NOT Gate:

A	Y

0	1
1	0

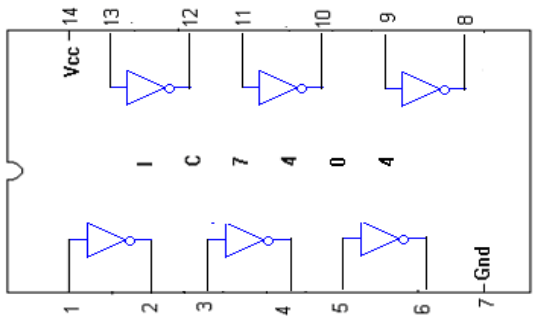

Figure 3.8: Pin Diagram of NOT gate

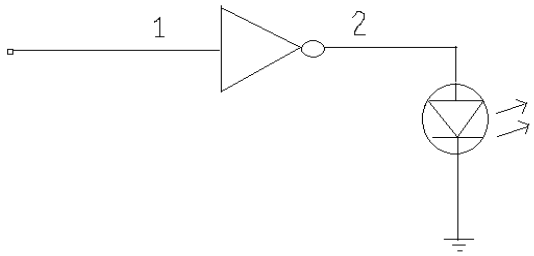

Figure 3.9: NOT gate with LED as load

d) XOR Gate gives logic 1 output if the two inputs are dissimilar.

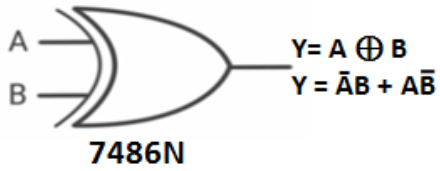

Figure 3.10: Symbol of XOR gate

Truth Table of XOR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1

1	1	0

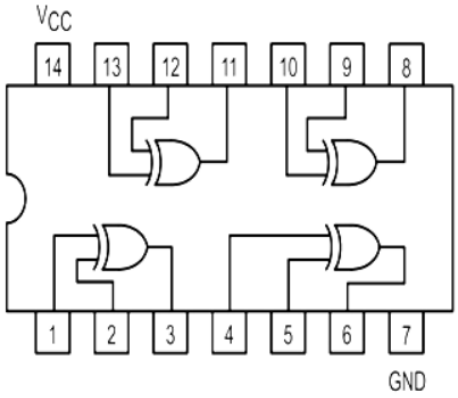

Figure 3.11: Pin Diagram of XOR gate (7486N)

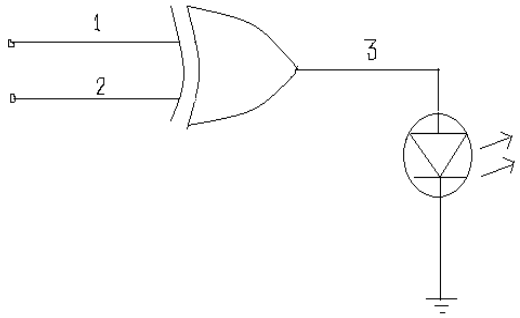

Figure 3.12: XOR gate with LED as load

e) XNOR Gate gives high output (logic 1) only if both inputs are same.

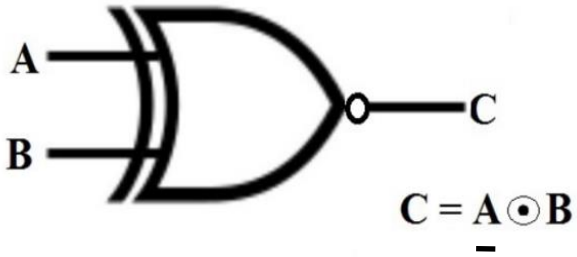

Figure 3.13: Symbol of XNORgate

Truth Table of XNOR Gate:

A	B	C
0	0	1

0	1	0
1	0	0
1	1	1

f) **NAND Gate** gives logic 0 as output only if all of its inputs are at logic 1.NAND gate is a contraction of AND-NOT.

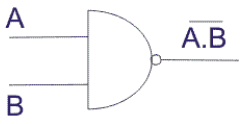

Figure 3.14: Symbol of NAND gate

Truth Table of NAND Gate:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

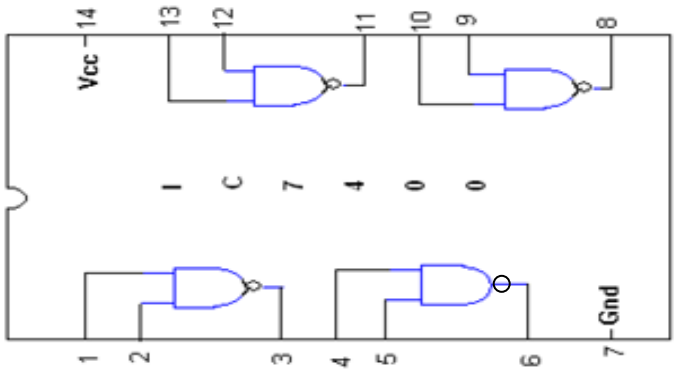

Figure 3.15: Pin Diagram of NAND gate

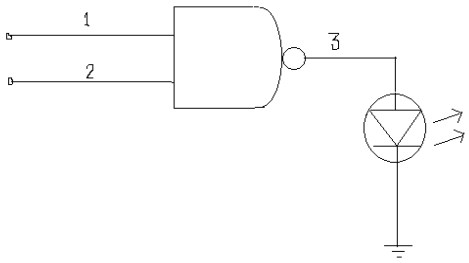

Figure 3.16: NAND gate with LED as load

g) NOR Gate gives logic 1 as output only if all of its inputs are at logic 0.NOR gate is a contraction of OR-NOT.

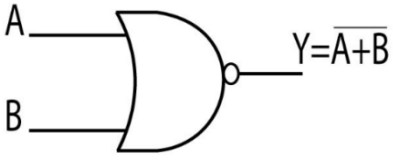

Figure 3.17: Symbol of NOR gate

Truth Table of NOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

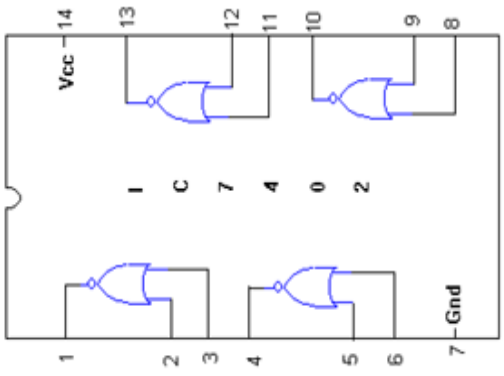

Figure 3.18: Pin Diagram of NOR gate

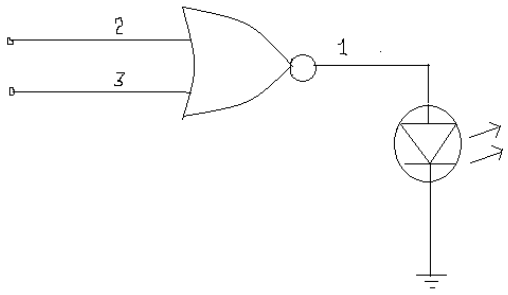

Figure 3.19: NOR gate with LED as load

Experimental Procedure:

1. Turn the power (Trainer Kit) off during circuit implementation.
2. Connect the +5V and ground (GND) leads of the power supply to the power and ground bus strips on your breadboard.
3. Point all the chips in the same direction with pin 1 at the upper-left corner on breadboard. (Pin 1 is often identified by a dot or a notch next to it on the chip package).
4. Select a connection and place a piece of hook-up wire between corresponding pins of the chips on breadboard. It is better to make the short connections before the longer ones. Mark each connection of schematic in steps, so as not to try to make the same connection again at a larger stage.
5. If an error is made and not spotted before you turn the power on, turn the power off immediately before reconstructing the circuit.
6. Verify the truth table of given circuit.

Result: The truth tables of all gates AND, OR, NOT, XOR, XNOR, NAND and NOR gates have been verified. all gates have been realized by universal gates (NAND and NOR).

Result Analysis & Discussion: This section should be written individually by each student.

Inferences & Conclusion: This section should be written individually by each student.

Learning Outcomes:

1. Depth knowledge of basic gates ICs.
2. Learning the pin description of ICs.

Applications:

1. NOT gates are used in oscillators to generate clock signals.

2. AND gate is used in the measurement of frequency of a pulsed waveform.
3. EX-OR gates are used in parity generation, checking units and comparators.

Precautions:

1. Turn the power off before making any connection.
2. Make connections carefully.