Legend:
- Inst. Mem data
- Inst. Mem Addr
- Data. Mem Data
- Data. Mem Addr
- Control

Inst. Mem 4K

DataMem 4K

CONTROL/STATUS_REG

Register File

rd_data_1
rd_data_0
Wr_dat

Target Addr

PC

mux

1

Add

Next Addr

src_0

PC Addr[11:0]

rd_sel_1

rd_sel_0

src_0

8bit Inst. Data Bus

branch

Control Unit [FSM]

Execute_en

Fetch_en

wr_sel

rd_dat_1

final

ALU

result

MUX

8 bit Data Bus

m_data

ifetch_reg

Decode

Imm_dat

MUX

src_1

do_alu

load

rd

wr

en

Imm_vld

exec_ctrl

exec_ctrl_decoder

Addr[11:0]

Execute

ifetch

3 Stage Pipeline - CPU