SUPREETA VENKATESAN

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OBJECTIVE

To develop my skills in the field of VLSI Design through an Internship/ Co-op starting May 2020.

EDUCATION

University of Southern California, Los Angeles **Dec 2020**
Master of Science (M.S.), Electrical and Computer Engineering **CGPA: 3.38/4**
Coursework: MOS VLSI Circuit Design (EE477L), VLSI System Design I – Advanced Circuit Design (EE577a), Diagnosis and Design of Reliable Digital System- DFT (EE658), Solid State Processing and Integrated Circuits Laboratory (EE504L), Computer Systems Organization (EE457).

SSN College of Engineering, Anna University **May 2018**
Bachelor of Engineering (B.E.), Electronics and Communication Engineering **CGPA: 8.62/10**
Coursework: Circuit Theory, Electronic Devices, Digital Electronics, OOPS and Data Structures, Microprocessors and Microcontrollers, Computer Architecture, VLSI Design.

TECHNICAL SKILLS

Languages	C, C++, Python
Hardware Languages	Basics of System Verilog, Verilog, TCL Scripting
EDA Tools	Cadence Virtuoso, Cadence Spectre, Xilinx ISE, Questa Sim, Cadence Indago, Tanner EDA, P-Spice
Hardware Platforms	Arduino IDE, Intel 8051 and 8086, TI MSP 430, FPGA Trainer Kit, R-Pi

EXPERIENCE

Edveon Inc. Chennai, India
Design Verification Intern **Aug-Dec 2018**

- Worked on developing the technical course content of programming languages like C++, System Verilog for Edveon's online learning platform.
- Understood the DUT Specification, built test cases to check its functionality and documented the implementation. Developed testbench using SystemVerilog for a Data Transmitter, ALU and Data Bus.

Data Patterns Pvt. Ltd. Chennai, India
Internship Trainee **Dec 2016**

- Learnt the hardware and software life cycles, basics of FPGA Programming and circuit design.
- Understood the implementation of technologies such as SMT for PCBs and manually soldered of the components as per the part list and inspected the same.

PROJECTS

Full Custom Design of a 16-bit MAC – Multiplier and Accumulator Circuit **March 2018**

- Designed a Wallace Tree Multiplier using Carry Save Adders and Ripple carry Adder to perform 6-bit x 6-bit multiplication followed by accumulation using RESET and ENABLE signals as control inputs.
- Schematic and Layout were designed, and its functionality was verified. DRC and LVS match were performed and the design was optimized to reduce the power*delay product.

Fabrication of Integrated Circuits **May 2019- July 2019**

- Fabricated 66 ICs on a 3-inch Wafer having discrete devices such as capacitors, resistors, CMOS Transistor and diodes in a class 100 clean room.
- Electrical characterization of the devices was performed using a microscope and LabView and the results were analyzed to understand the electrical properties of the fabricated devices.

CMOS Reverse Engineering **May 2019**

- Cross section of a fabricated CMOS Transistor was analyzed mask by mask through reverse engineering, studying and understanding the fabrication of the same.

Design of Five Stage Pipelined CPU **Feb-April 2019**

- Designed a five stage (IF, ID, EX, MEM, WB) pipelined CPU which supports instructions such as ADD, SUB, MOV, DIV, LW and SW. The designed is capable of being modified to support fewer stages.
- Implemented a Hazard Detection Unit (HDU) and Forwarding Unit (FU) to remove data dependencies and hazards and thus reducing the number of stalls.

Cloud Based Secure Parking System **Oct 2017-April 2018**

- Modelled and built a cloud-based parking management system which provides the users the option of pre-booking the parking slots and access to the parking lot with RFID and fingerprint.

CERTIFICATIONS

'Kaizen Robotics Program Level-1' & 'Level-2', by Lema Labs.
'Printed Circuit Board Design' by SSN College of Engineering.
'TCL Programming- From novice to expert' Course on Udemy.

LEADERSHIP

Secretary - Association of Electronics and Communication Engineers - SSN College of Engineering
Organized **INVENTE'17** - A National level technical Symposium.

WORK AUTHORIZATION

Eligible to work in the United States of America under Curricular Practical Training (CPT).