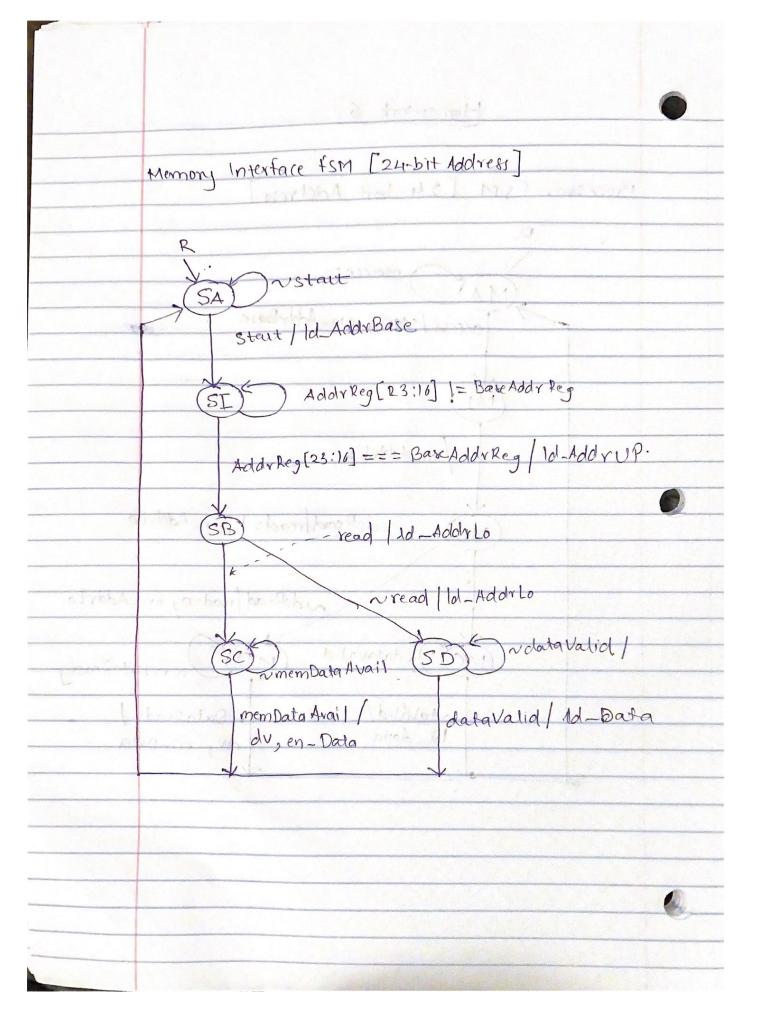
Homework-6 reaches a fine ] that a other of examine Processor FSM [24-bit Adolvers] R access / start, en-Addr Base MI en\_AddrUp -- do Read | read = 1, en-Addr Lo ~ doRead read=0, en\_Addr Lo MD NW Data Ready ) adata Valid dataValid/ nDatoReady/ lol-data dv, en-Data



& Additions to the FSM: Processor side: (1 state) to en\_Addr Bax: enable bus drivers to drive upper 8 bits [23:16] of Addr Reg onto bus address line Memory side: (1 State) 10-Addr Base: enable tous upper 8 bits [23:18] of Addr Reg to be loaded from bus address lines Base Add v Reg [7:0]: An internal x logic block to store check w/ Add rpeg [23:16] to make sense as to which memory interface will load the data.