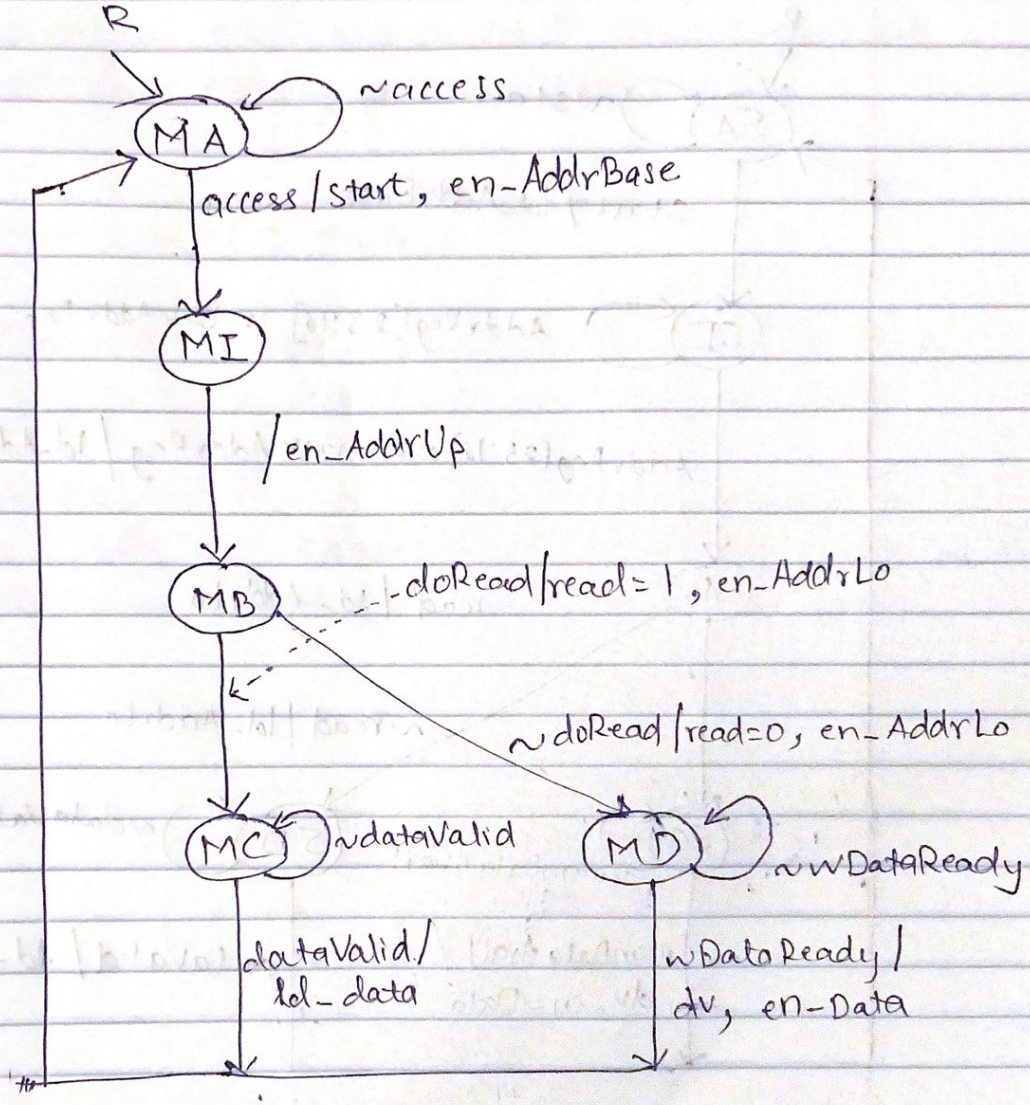
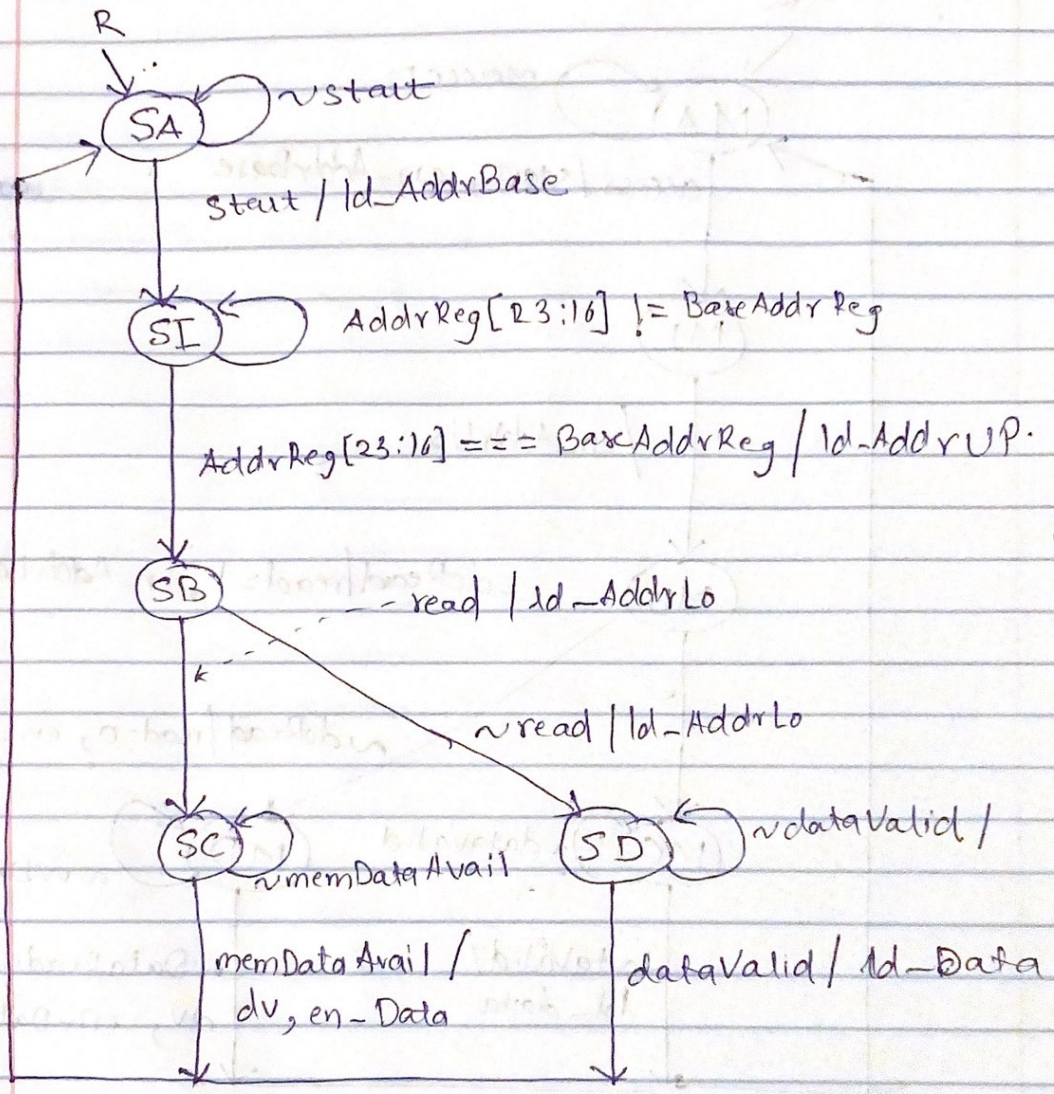
Homework - 6

Processor FSM [24-bit Address]



Memory Interface fsm [24-bit Address]



£ Additions to the FSM:

Processor side: (1 state)

☆ en_AddrBase: enable bus drivers to drive upper 8 bits [23:16] of AddrReg onto bus address line.

Memory side: (1 state)

ld_AddrBase: enable ~~bus~~ upper 8 bits [23:16] of AddrReg to be loaded from bus address lines

BaseAddrReg [7:0]: An internal ~~x~~ logic block to ~~store~~ check w/ AddrReg [23:16] to make sense as to which memory interface will load the data.