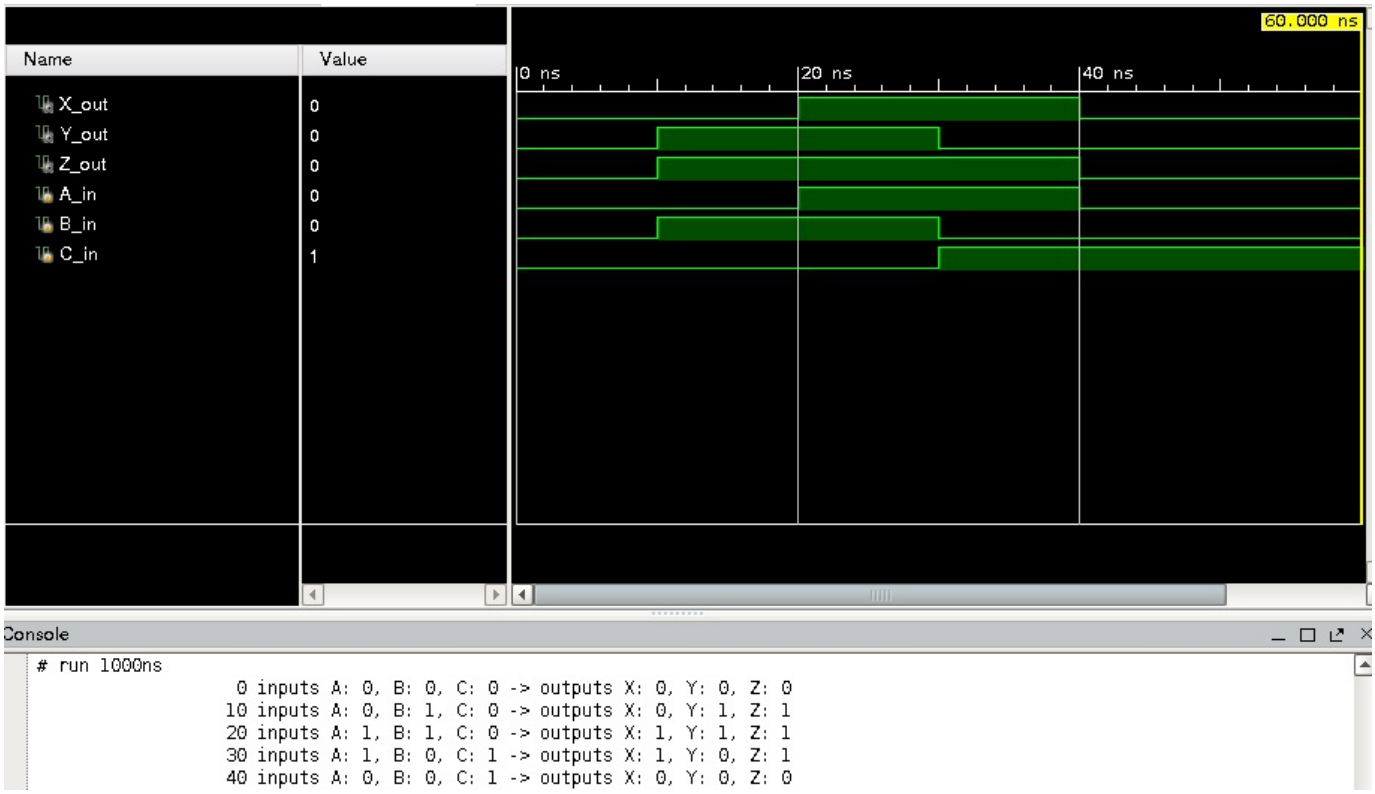
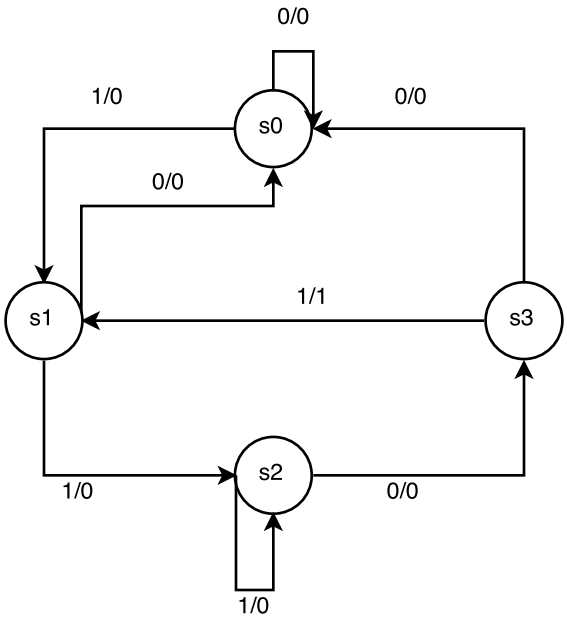
1.



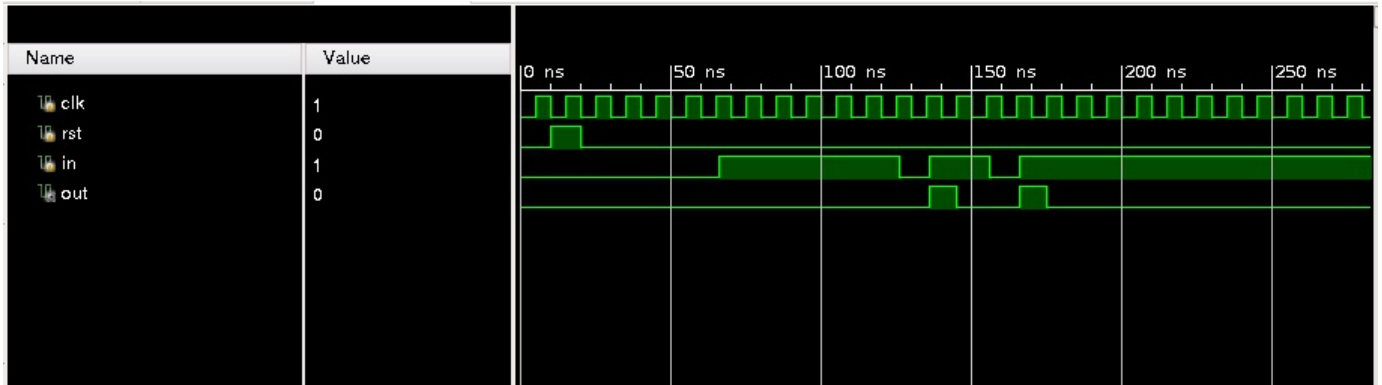
waveform of three different implementation are exactly the same, here I only attached one, others were include in the folder

2.

FSM



s0: any other states
s1: 1
s2: 11
s3: 110

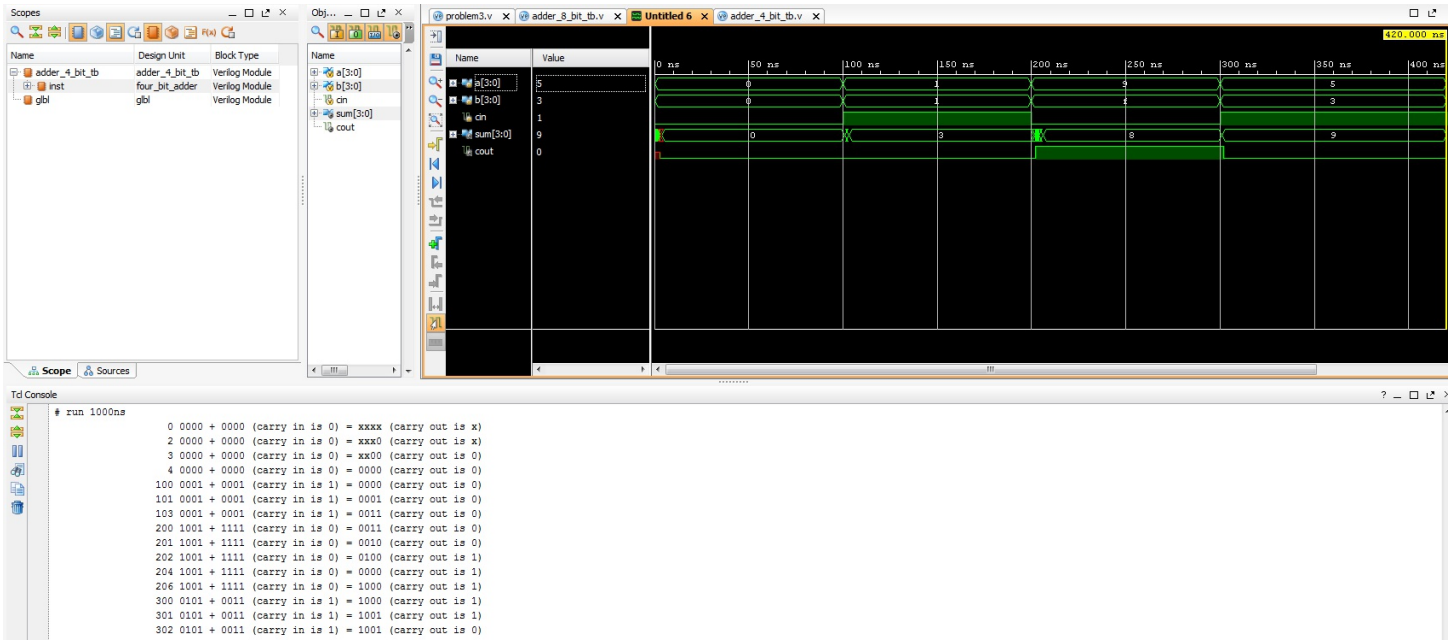


3.

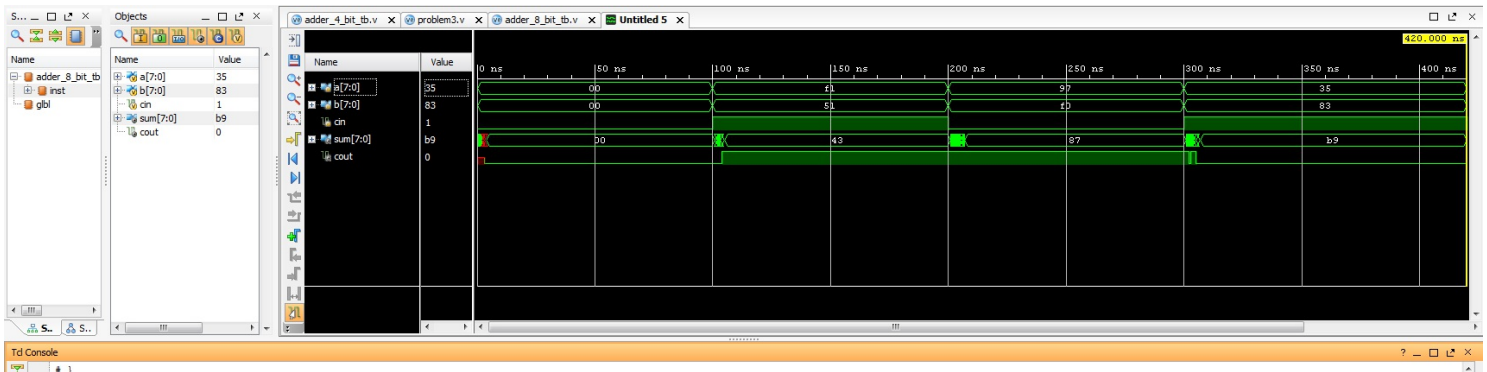
in the 4-bit ripple adder, at time 100, the two inputs change to 0001, the carry in is 1
the correct output was produced at time 103
in the 8-bit ripple adder, at time 100, the two inputs change to 11110001 and 01010001, the carry in is 1
the correct output was produced at time 105

the delay was produced when the output of XOR / AND / OR gate changed, the delay time is depend on inputs and carry in.

4-bit ripple adder

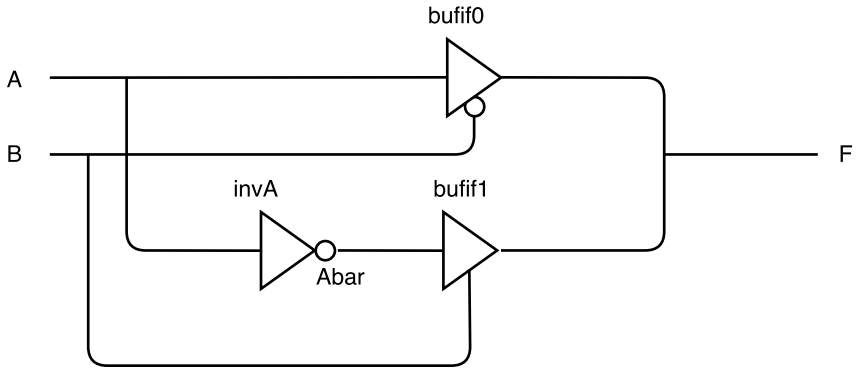


8-bit ripple adder



```
# run 1000ns
                0 00000000 + 00000000 (carry in is 0) = xxxxxxxx (carry out is x)
                2 00000000 + 00000000 (carry in is 0) = xxxxxxx0 (carry out is x)
                3 00000000 + 00000000 (carry in is 0) = xxxxxx00 (carry out is 0)
                4 00000000 + 00000000 (carry in is 0) = 00000000 (carry out is 0)
              100 11110001 + 01010001 (carry in is 1) = 00000000 (carry out is 0)
              101 11110001 + 01010001 (carry in is 1) = 00000001 (carry out is 0)
              102 11110001 + 01010001 (carry in is 1) = 10100001 (carry out is 0)
              103 11110001 + 01010001 (carry in is 1) = 00000011 (carry out is 0)
              104 11110001 + 01010001 (carry in is 1) = 00000011 (carry out is 1)
              105 11110001 + 01010001 (carry in is 1) = 01000011 (carry out is 1)
              200 10010111 + 11110000 (carry in is 0) = 01000011 (carry out is 1)
              201 10010111 + 11110000 (carry in is 0) = 01000010 (carry out is 1)
              202 10010111 + 11110000 (carry in is 0) = 10000101 (carry out is 1)
              203 10010111 + 11110000 (carry in is 0) = 00000111 (carry out is 1)
              204 10010111 + 11110000 (carry in is 0) = 10000011 (carry out is 1)
              205 10010111 + 11110000 (carry in is 0) = 10000111 (carry out is 1)
              206 10010111 + 11110000 (carry in is 0) = 10001111 (carry out is 1)
              207 10010111 + 11110000 (carry in is 0) = 10000111 (carry out is 1)
              300 00110101 + 10000011 (carry in is 1) = 10000111 (carry out is 1)
              301 00110101 + 10000011 (carry in is 1) = 10000110 (carry out is 1)
              302 00110101 + 10000011 (carry in is 1) = 01010111 (carry out is 0)
              303 00110101 + 10000011 (carry in is 1) = 01110101 (carry out is 1)
              304 00110101 + 10000011 (carry in is 1) = 11110101 (carry out is 1)
              305 00110101 + 10000011 (carry in is 1) = 10110001 (carry out is 0)
```

4.



The functionality of my design is to control outputting the input value or its reverse.