Design And Implementation of 4x4 RAM

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Contents

1 Abstract

A memory unit is a device to which binary information is transferred for storage and from which information is retrieved when needed for data processing.There are two types of memories that are used in digital systems: random-access memory (RAM) and read-only memory (ROM). RAM can perform both write and read operations. ROM can perform only the read operation. In this project,a 4x4 RAM circuit design is implemented on Magic VLSI Layout tool and simulated on IRSIM.

2 Introduction

Random-access memory is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code.RAM contains multiplexing and de-multiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. RAM is normally associated with volatile types of memory (such as dynamic random-access memory (DRAM) modules), where stored information is lost if power is removed, although non-volatile RAM has also been developed.

3 Circuit Diagram

In this section, we present the internal construction of a RAM. To be able to include the entire memory in one diagram, the memory unit presented here has a small capacity of 16 bits, arranged in four words of 4 bits each.The internal construction of a RAM of 4 words and 4 bits per word consists of 4 * 4=16 binary storage cells and associated decoding circuits for selecting individual words. The binary storage cell is the basic building block of a memory unit. During the read operation, the four bits of the selected word go through OR gates to the output terminals. The OR gates are drawn according to the array logic as in Fig 3.1.

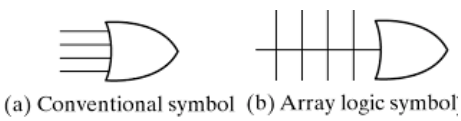


Figure 3.1: OR Gate Diagram

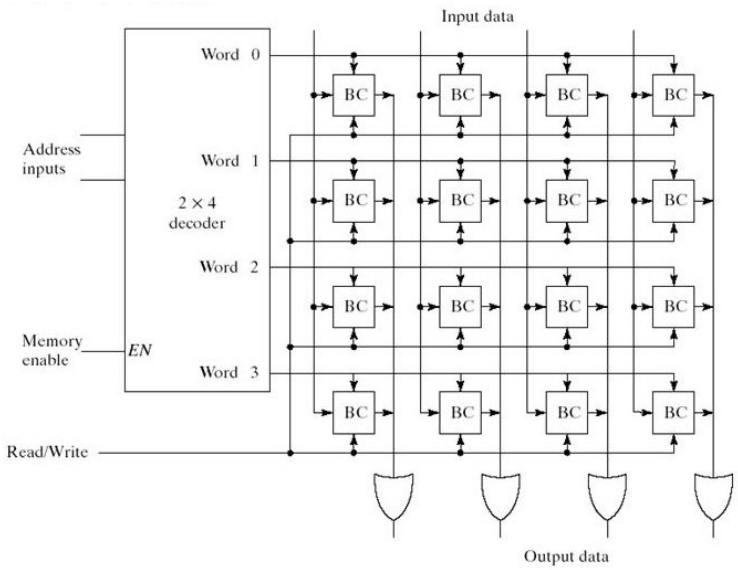


Figure 3.2: 4x4 RAM Circuit Diagram

4 Design And Implementation

The Layout is designed using MAGIC Layout tool.All the gates used in the design are taken from vsclib standard cell library. The Simulation of the Layout is done on IRSIM. All the gates used are of Drive strength 1 and version 1 from vsclib.

4.1 SR Latch

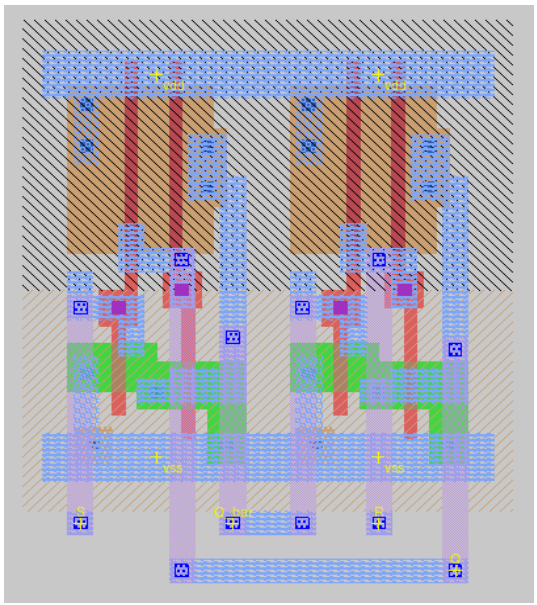
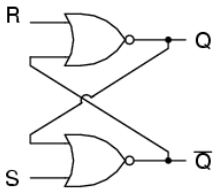


Figure 4.1: Layout of SR Latch



S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

Figure 4.2: Circuit Diagram of SR Latch

The SR latch is implemented with NOR Gates as for Inputs $S = 0$ and $R = 0$ the latch gives same output as for previous inputs,i.e the output is latched to previous output.

Test Bench for SR Latch

```
1  stepsize 25
2  h vdd
3  l vss
4  vector SR S R
5  vector OUT Q Q_bar
6  analyzer SR OUT
7  setvector SR 10
8  s
9  setvector SR 00
10 s
11 setvector SR 01
12 s
13 setvector SR 00
14 s
15 setvector SR 11
16 s
17 setvector SR 01
18 s
19 setvector SR 00
```

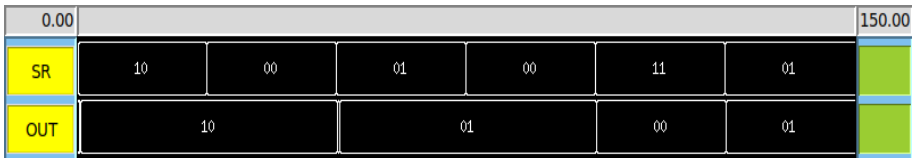


Figure 4.3: Analyzer Plot from IRSIM Simulation of SR Latch Layout

4.2 Memory Block

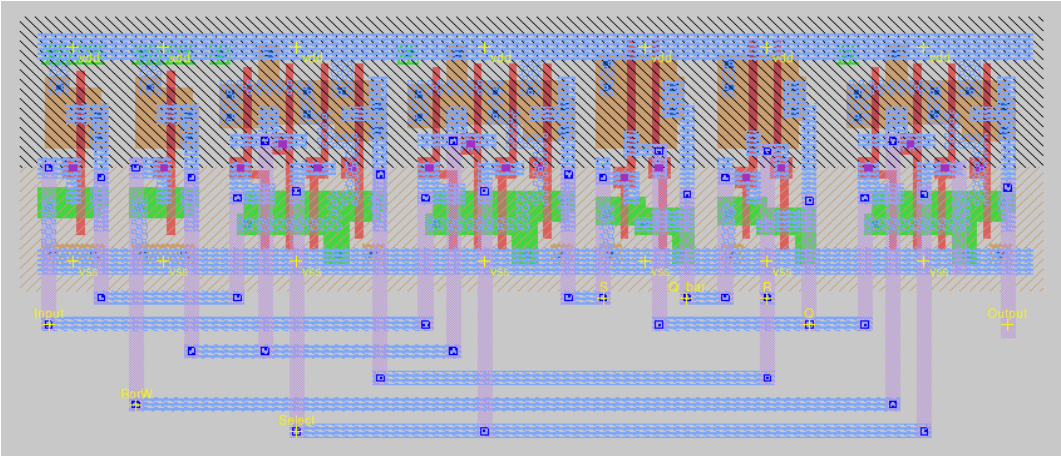


Figure 4.4: Layout of Memory Block

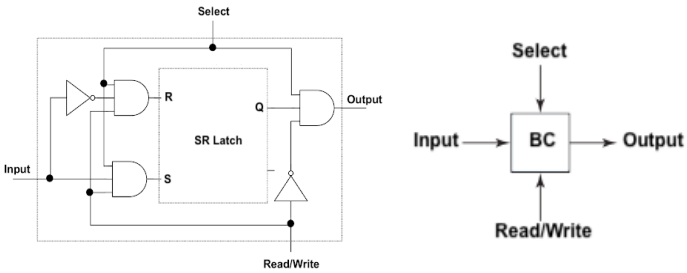


Figure 4.5: a.Circuit Diagram b. Block Diagram of Memory Block

The Select line enables the cell for reading or writing, and the read/write line(RorW Node in Layout) determines the operation of the cell when it is selected. A 1 in the read/write line provides the read operation by forming a path from the latch to the output terminal. A 0 in the read/write line provides the write operation by forming a path from the input terminal to the latch.The Input line will contain the bit to be written into the Memory block when the block is in write mode, and the output line will contain the bit to be read when the block is in write mode.

Test Bench for Memory Block

```
1 stepsize 25
2 h vdd
3 l vss
4 h Select
5 analyzer Input Output RorW
```

```
6  l RorW
7  h Input
8  s
9  h RorW
10 s
11 l RorW
12 l Input
13 s
14 h RorW
15 s
```

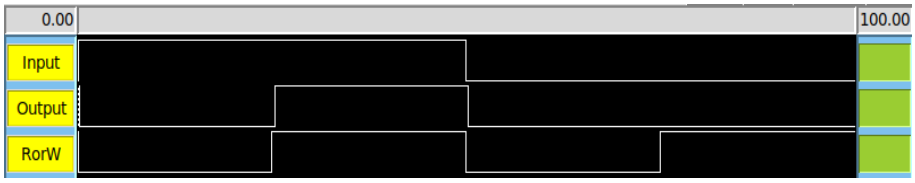


Figure 4.6: Analyzer Plot from IRSIM Simulation of Memory Block Layout

4.3 2-4 Decoder

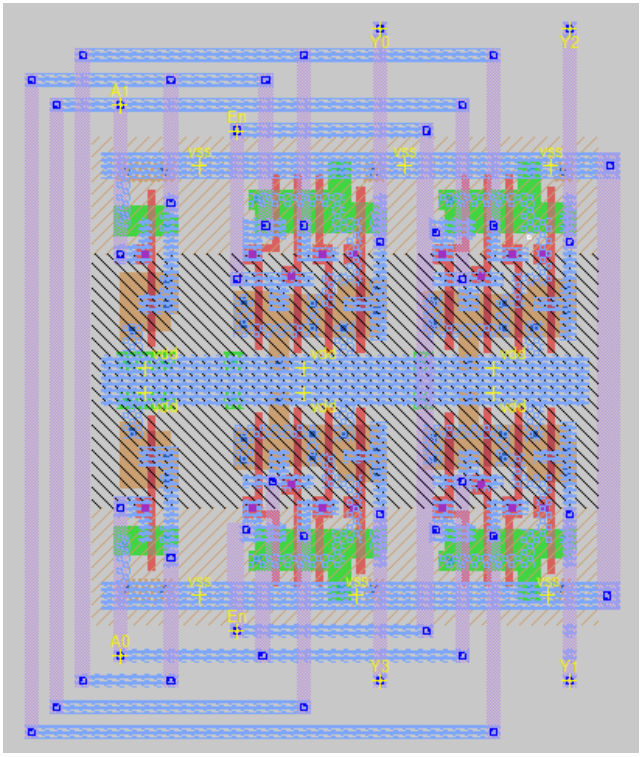


Figure 4.7: Layout of 2-4 Decoder

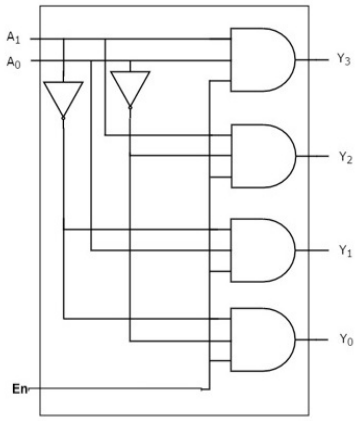


Figure 4.8: Circuit Diagram of 2-4 Decoder

A conventional 2-4 line decoder is used to select a word from the 2 bit address input for Read/Write opertaion.

Test Bench for Decoder

```
1  stepsize 25
2  h vdd
3  l vss
4  h En
5  vector in A1 A0
6  vector out Y3 Y2 Y1 Y0
7  analyzer in out En
8  setvector in 10
9  s
10 setvector in 00
11 s
12 setvector in 01
13 s
14 setvector in 00
15 s
16 setvector in 11
17 s
18 l En
19 s
20 setvector in 01
```

```
21 s
22 setvector in 00
23 s
```

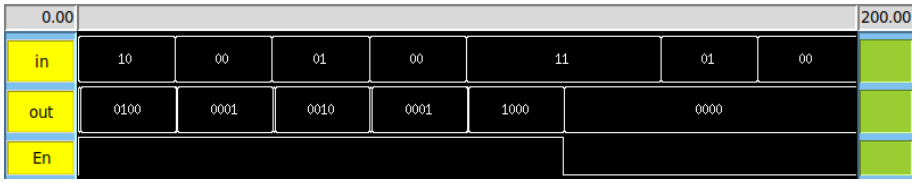


Figure 4.9: Analyzer Plot from IRSIM Simulation of Decoder Layout

4.4 4x4 RAM

The final 4x4 RAM layout is achieved using all the blocks as shown in Fig 3.2. Moving from left to right, the words are as Word 2,Word 3,Word 1 and Word 0 respectively,likewise the individual bits are arranged top to bottom as D3,D2,D1 and D0 respectively in the layout as shown in figure. The VDD lines of Word 0 and Word 1 abut each other, likewise VDD lines Word 2 and Word 3 of abut each other.

Test Bench for Memory Block

```
1  stepsize 25
2  h vdd
3  l vss
4  h En
5  vector in In3 In2 In1 In0
6  vector out D3 D2 D1 D0
7  vector adr A1 A0
8  analyzer in out adr RorW
9  l RorW
10 setvector adr 00
11 setvector in 1010
12 s
13 l En
14 s
15 setvector adr 01
16 setvector in 1100
```

```
h En
s
l En
s
setvector adr 10
setvector in 0110
h En
s
l En
s
setvector adr 11
setvector in 0100
h En
s
h RorW
setvector in 0000
s
setvector adr 00
s
setvector adr 01
s
setvector adr 10
s
setvector adr 11
s
```

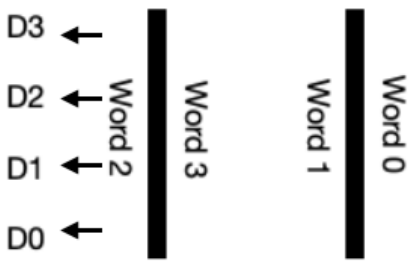


Figure 4.10: Word and Bit Arrangement in RAM Layout

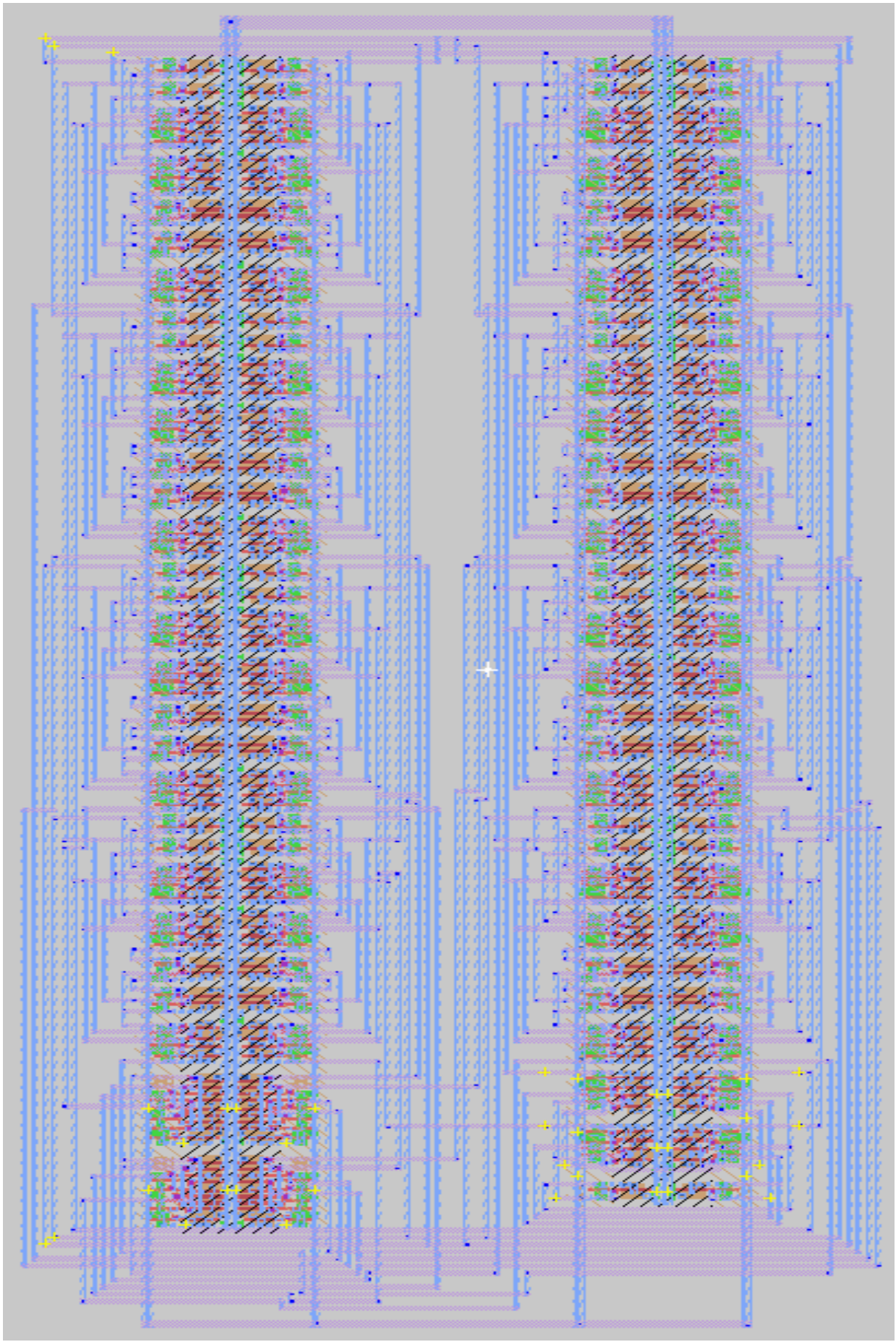


Figure 4.11: Layout of 4x4 RAM

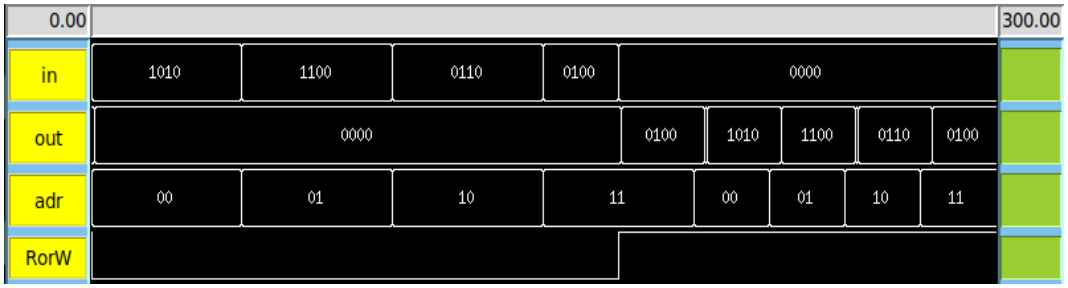


Figure 4.12: Analyzer Plot from IRSIM Simulation of RAM Layout

The binary values of 1010,1100,0110,0100 are stored in address location of 0x00, 0x01, 0x10, 0x11 respectively. The reading and writing operation of RAM is thus verified.

5 Conclusion

A total of 122 gates are used in the design. All the individual blocks of the 4x4 RAM are designed and simulated. From the output generated by IRSIM simulation, it is clear that the 4x4 RAM circuit works as expected.