Towards Cell-Aware Test For Small Delay Faults

Study Project

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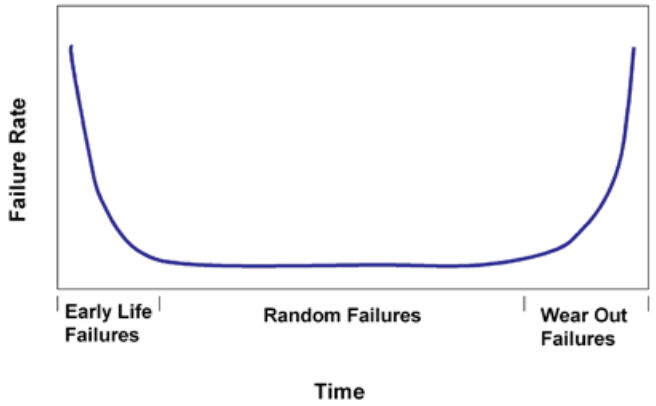
- **What is the problem ?**
  - Manufacturing test - nominal frequency set
  - Small delays - escapes this test

- **Result of the problem**
  - Early life failure of the device



- **Solution**
  - Inserting defects with high probability, resulting in small delay
  - Efficient & realistic defect model generation, helping in analysis of small delay

Outline

- Introduction
- Preliminaries
- Tool Overview & Results
- Conclusion

- **Introduction**
- Preliminaries
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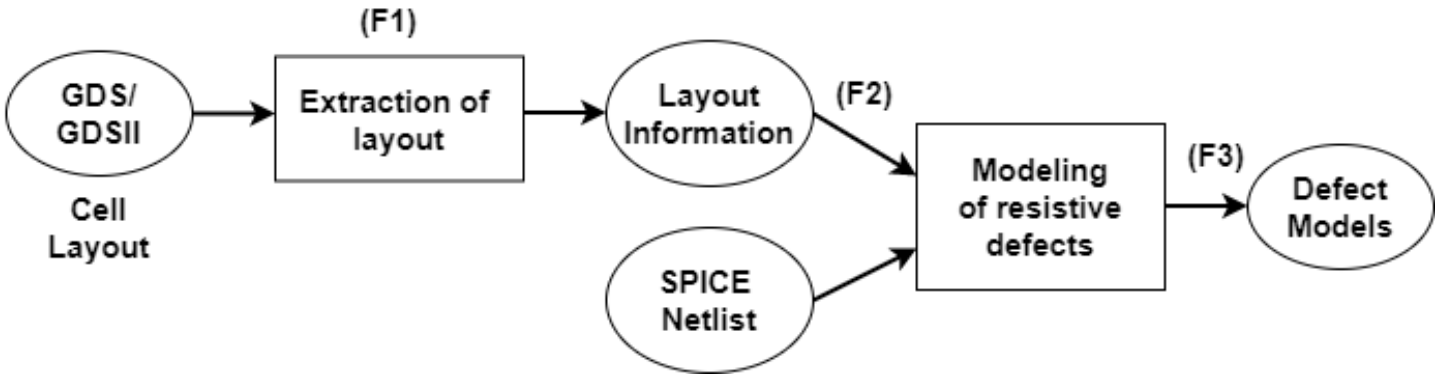
Motivation

- Transistors Count - doubles every two years
  - Thousands in 1970's to billions at present
- Increase in transistors → increase in defects
  - Solution: demand for higher quality tests
- Technology scaling down from 10µm (1971) to 5 nm (2020)
  - One of the results: a lot of timing-related defects
- Small delay defects - extra small delay in circuit
- Increases at field level → resulting in early life failure of the device

Cell-Aware Test

- Timing-related defects found in standard cell library
  - Cell internal defects are the most predominant
- Cell-Aware Test (CAT)
  - Testing the cell using layout information
- New era in defect modeling and defect circuit analysis

Focus of Study Project



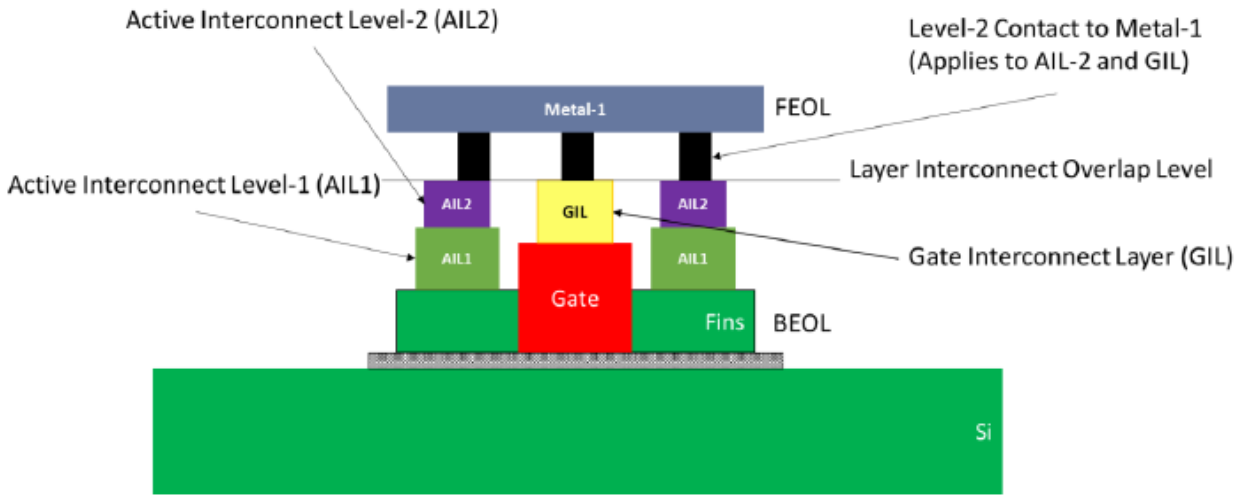
Flow of Study Project

- Introduction
- **Preliminaries**
- Tool Overview & Results
- Conclusion

Open Cell Library

- Based on FinFET FreePDK 15nm technology
- Package of standard cells
  - Includes OR, AND, inverter etc at different drive strenghths
- Information of cell available
  - GDSII files
  - SPICE netlist
- Most used library in universities and research institutions
  - Independent EDA flow testing
  - Development of cell-based design flows

FinFET Technology



Cross-section of FinFET

GDS/GDSII Files

- In OCL, information about the layout of the cell/circuits

- GDS/GDSII files
  - Platform independent
  - Text labels, planar geometric shapes in hierarchial form
  - Binary format - difficult to read

Record

- Sequential list of variable length records
- Record - record type, data type, data

Bit No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word1	Total record length in bytes															
Word 2	Record Type								Data Type							
Word 3	Data															

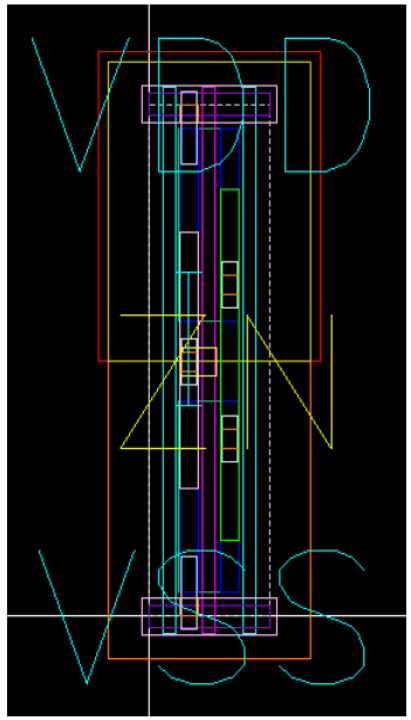
Record Header

Record Fields

- 57 different record types
  - Libname, Boundary, Layer ...
- 7 different data types
  - INT2, INT4, ASCII ...

Example: Inverter Cell

Cadence Virtuoso Tool



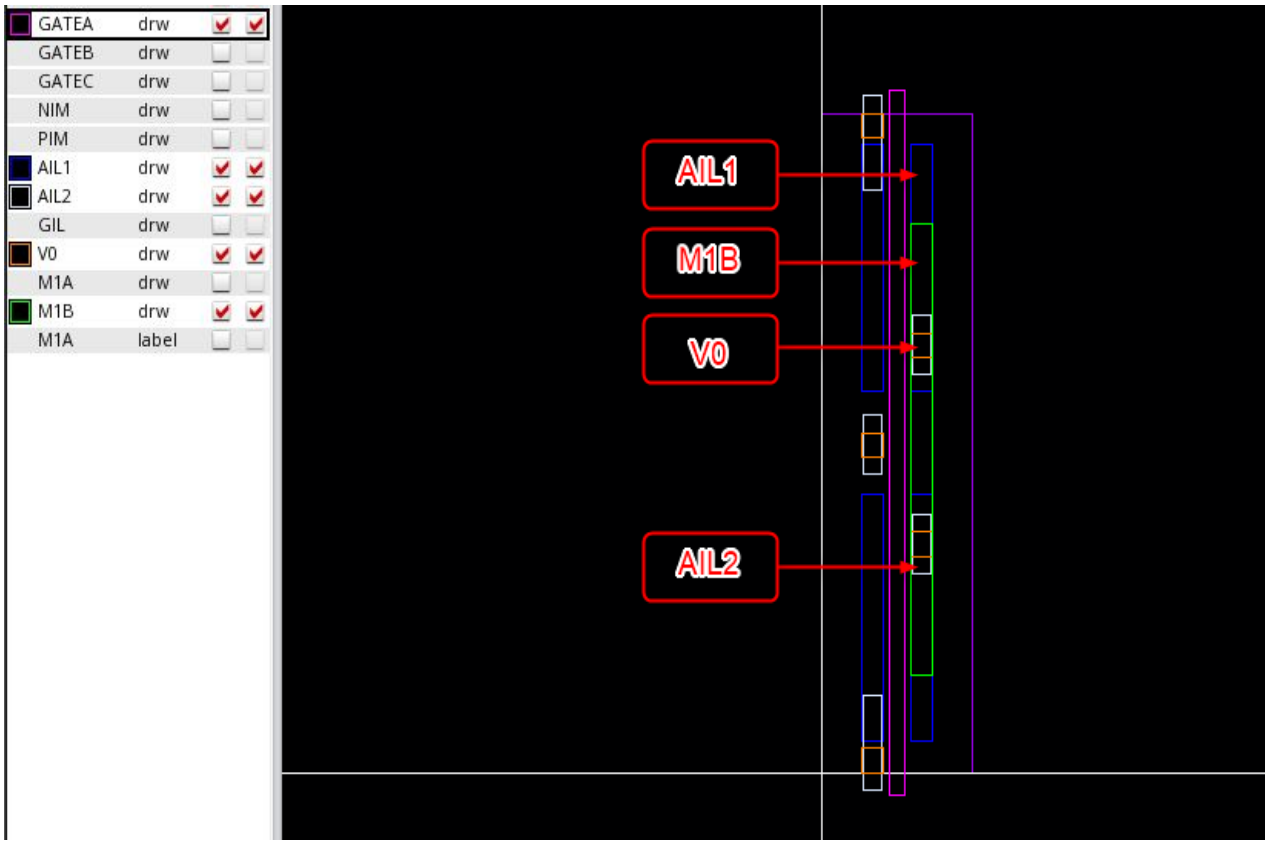
Layout of Inverter

Layer Information

Layer Name	Layer No.
NW	0
ACT	1
GATEA	7
GATEB	8
GATEC	9
NIM	5
PIM	6

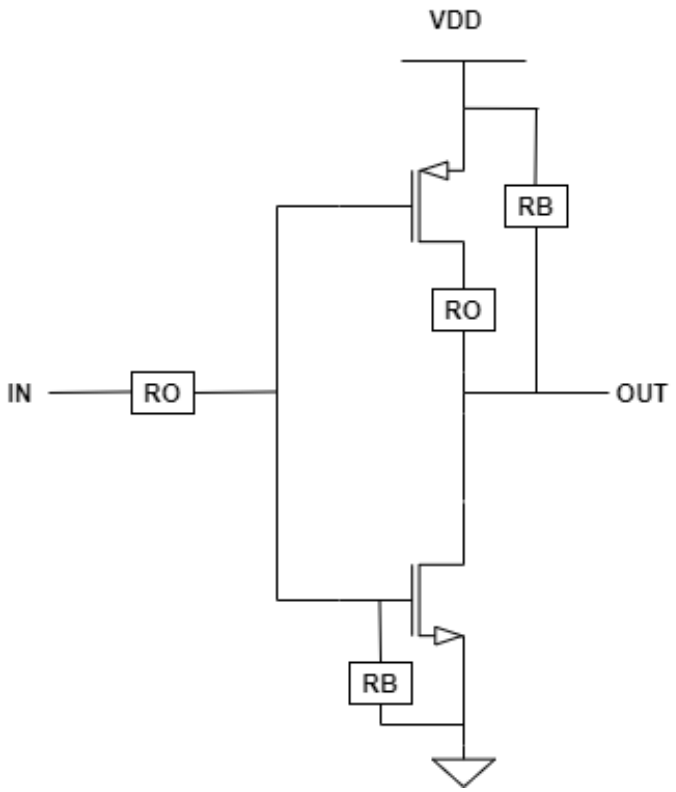
Layer Name	Layer No.
AIL1	11
AIL2	12
GIL	13
V0	14
M1A	15
M1B	16
prBoundary	200

Interconnect Layers - GDS File



Small Delay Defects

- Small delay defects - small extra delay
- Resistive defects
  - Resistive bridge
    - Examples: shorts between gates and source, neighboring wires
  - Resistive open
    - Examples: open on gate, thin wires



Resistive Bridge / Open : Inverter

- Introduction
- Preliminaries
- **Tool Overview & Results**
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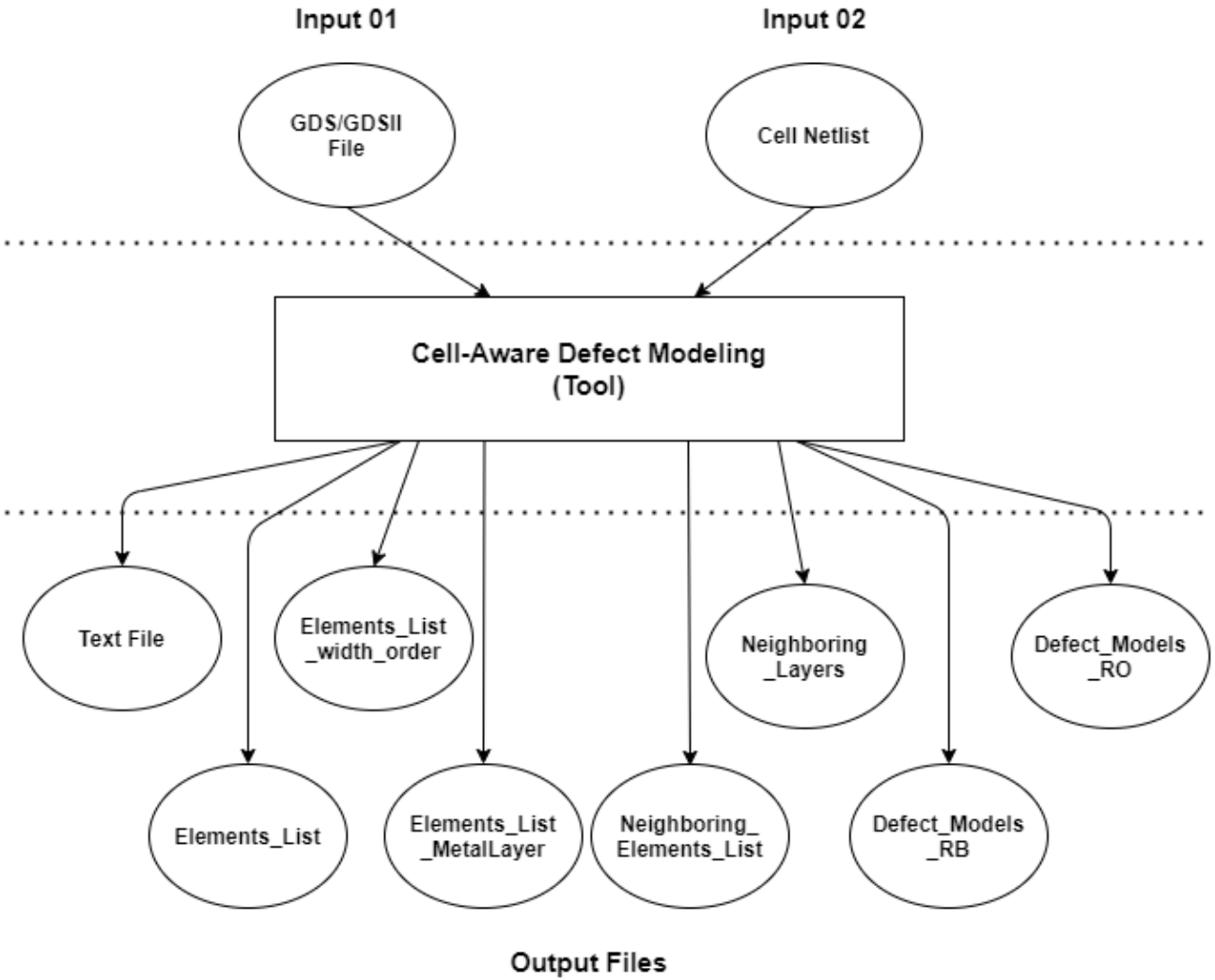
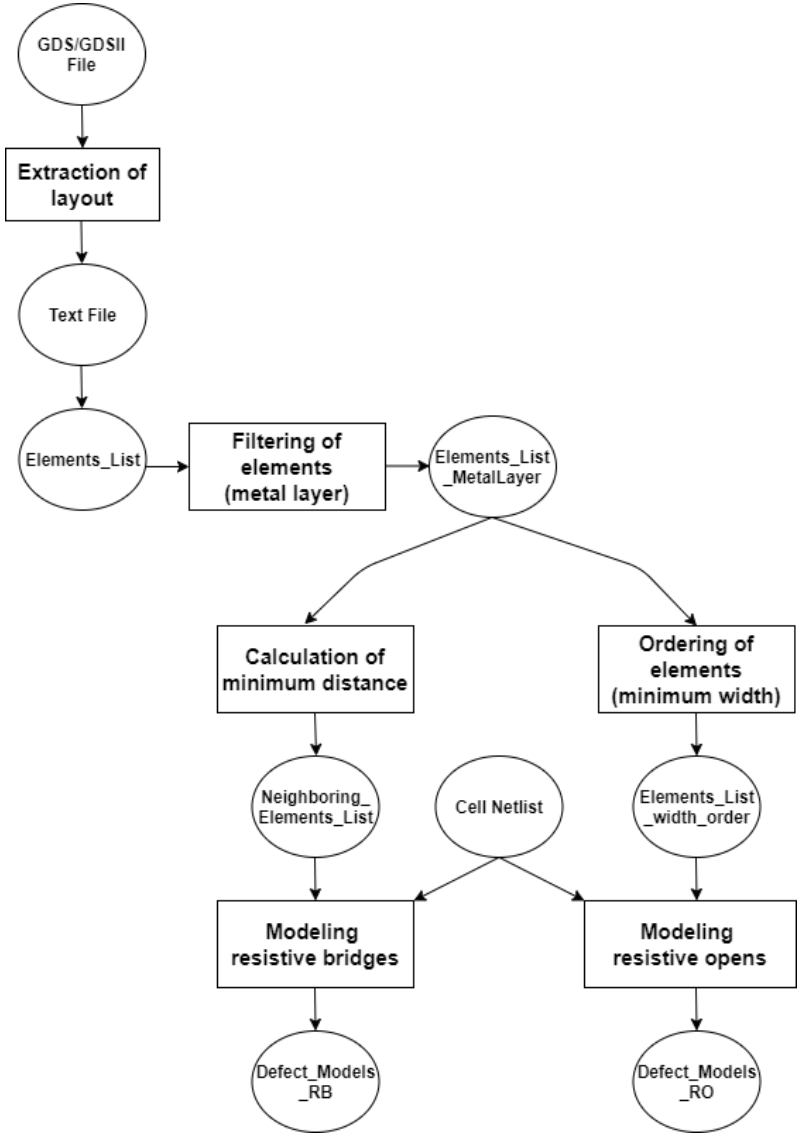
Tool Overview



Flow Chart


GDS/GDSII File
Extraction of layout
Text File
Elements_List
Filtering of elements (metal layer)
Elements_List _MetalLayer
Calculation of minimum distance
Ordering of elements (minimum width)
Neighboring_ Elements_List
Cell Netlist
Elements_List _width_order
Modeling resistive bridges
Modeling resistive opens
Defect_Models _RB
Defect_Models _RO

Layout Information Extraction

- GDS/GDSII file → text file
- Python gdsii library
  - Create, read, modify,save gds files
- Based on datatypes - records can be differentiated
- Initial information: name of standard cell, library etc
- Useful information: boundary and text elements in different layers

Boundary Element

- Boundary element - particular layer, rectangular shape

  Properties (records) :
- Layer: number
- XY: position
- XY = (x1y1, x2y2, x3y3, x4y4, x5y5)

- ENDEL: element finished with ENDEL

Boundary Element

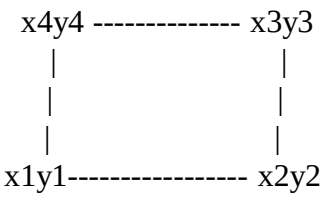
TEXT FILE

RecordType:BOUNDARY
DataType:NODATA
Data:None

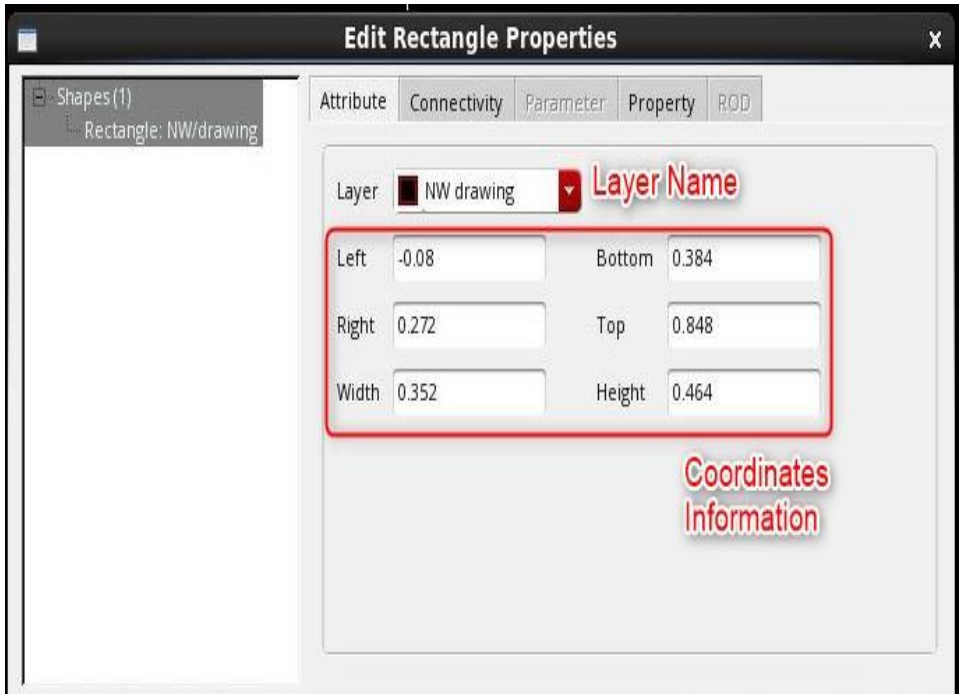
RecordType:LAYER
DataType:INT2
Data:(0,)
LayerNumber:0
Layer Name: NW

RecordType:XY
DataType:INT4
Data:(-80, 384, 272, 384, 272, 848, -80, 848, -80, 384)
Minimum Value: 352.0nm

RecordType:ENDEL
DataType:NODATA
Data:None



CADENCE TOOL



Text Element

- Text element - text/string displayed

  Properties (records):
- LAYER: number the text is found
- XY: position of the text
- STRING: text to be displayed
- ENDEL: element finished with ENDEL

Text Element

TEXT FILE

RecordType:TEXT
DataType:NODATA
Data:None

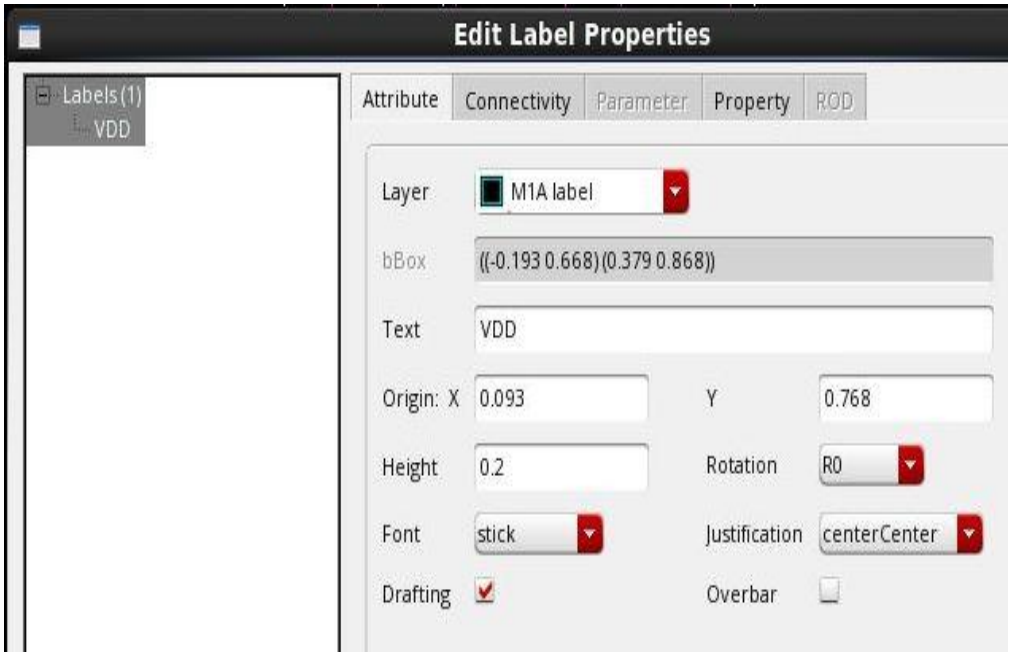
RecordType:LAYER
DataType:INT2
Data:(15,)
LayerNumber:15
Layer Name: M1A

RecordType:XY
DataType:INT4
Data:(93, 768)

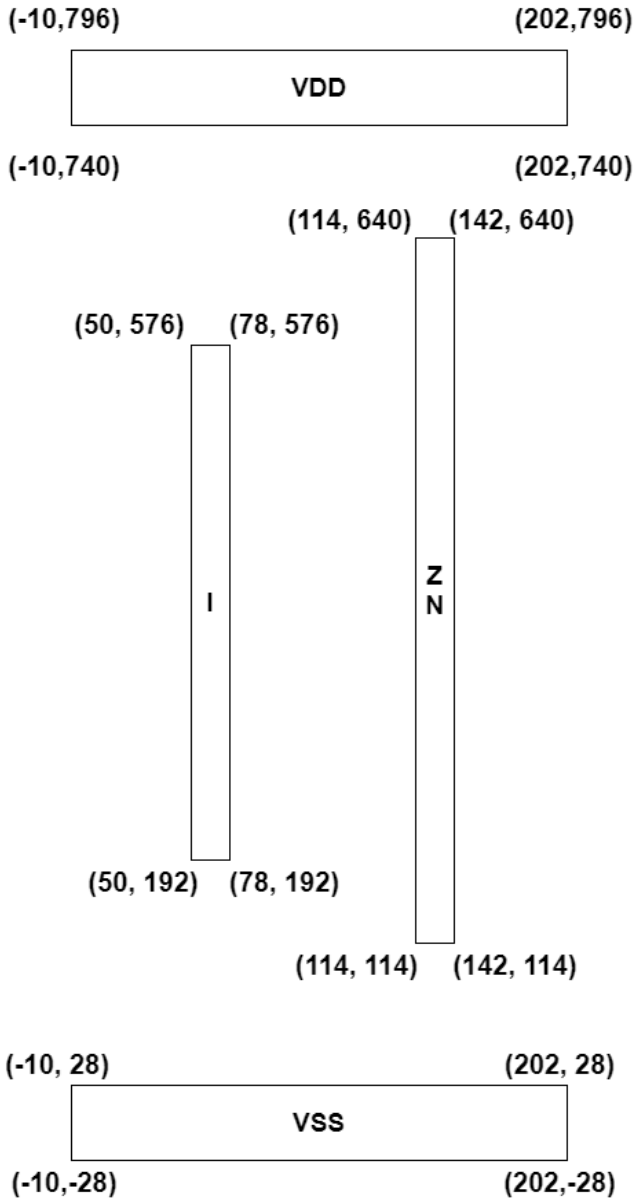
RecordType:STRING
DataType:ASCII
Data:VDD

RecordType:ENDEL
DataType:NODATA
Data:None

CADENCE TOOL



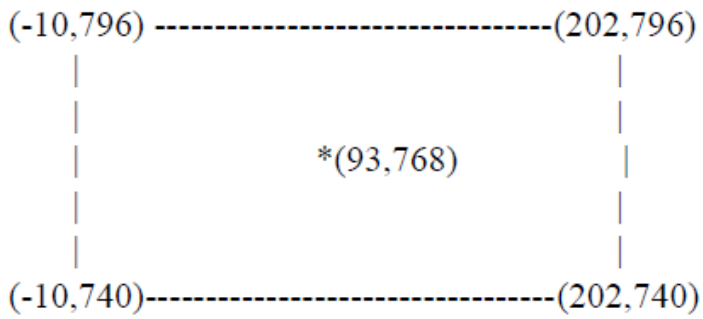
Minimum Width



- Example:
  Minimum width [VDD]
  minimum(796 - 740, 202 - (-10)) = 56

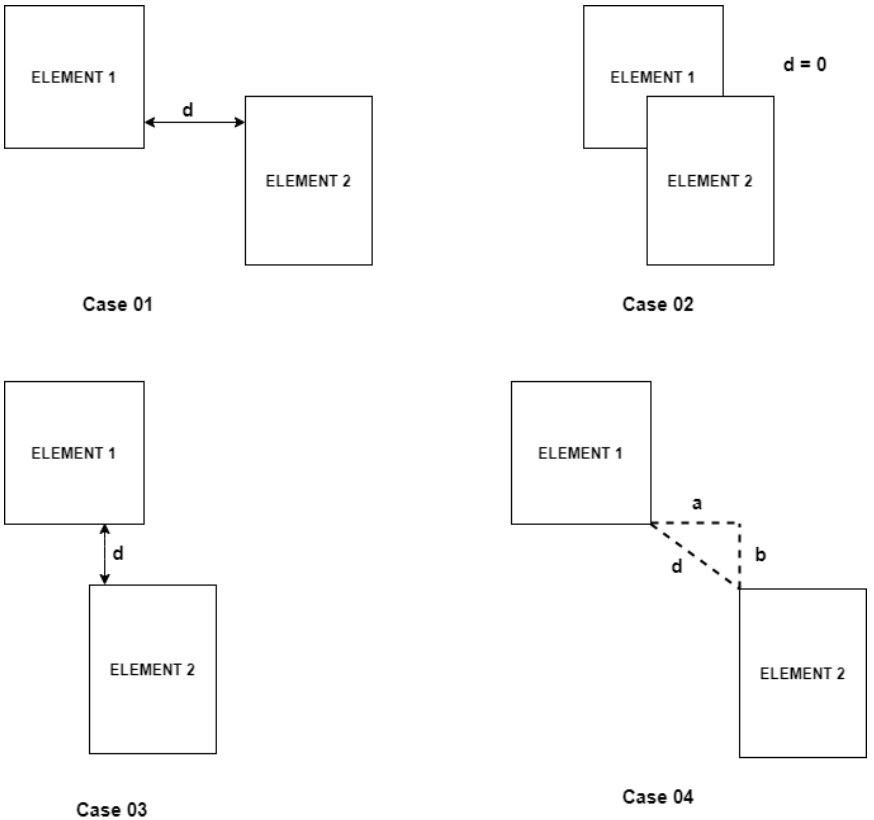
Element List Metal Layer

- Resistive bridge and resistive open - elements (metal layer)
- Element list - M1A: 15: 56.0: [’-10’,’-28’,’202’,’-28’,’202’,’28’,’-10’,’28’,’-10’,’-28’]
- Mapping between boundary and text element.
  Example:



Boundary element: (-10, 740, 202, 740, 202, 796, -10, 796, -10, 740)
Text element: (93, 768), STRING: VDD

Minimum Distance

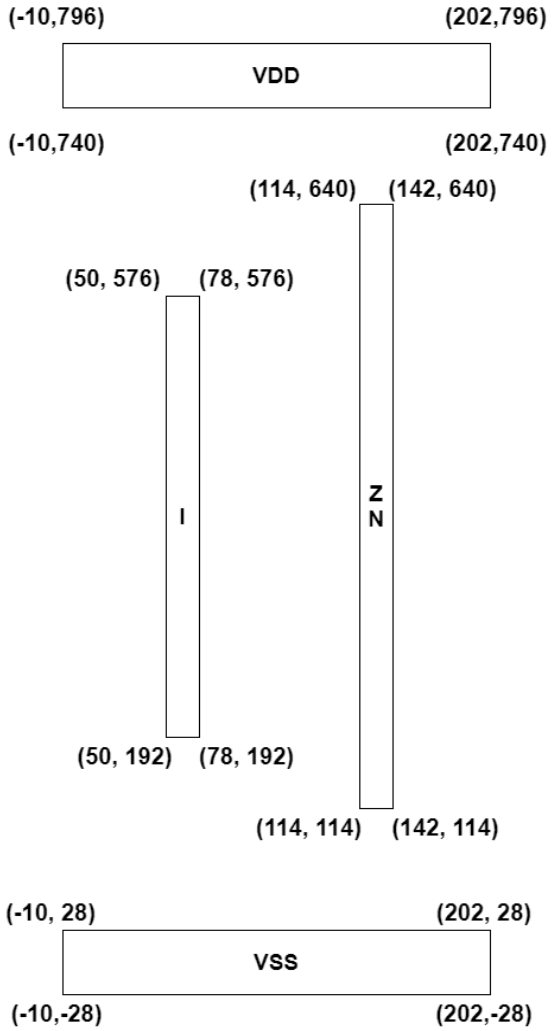


- Case 1 & 3: Minimum distance = d
- Case 2: Minimum distance = d = 0
- Case 4: Minimum distance = d = sqrt (a^2 + b^2)

Neighboring Elements List

- Contains information - distance between elements and the closest element to each element

- Example:
  For the input (I) of an Inverter:
  - I and ZN is 36.0 nm
  - I and VSS is 164.0 nm
  - I and VDD is 164.0 nm
  - Closest Element to I-ZN



Defect Models Generation

- Resistive bridge → neighboring elements & netlist - closest element
- Resistive open → minimum width & netlist - user input
- Default resistance “x0 = 1000” in .SUBCKT line - cell instantiation

Resistive Bridge

- Inverter - 4 defect models with resistive bridge

- Example:
  I - ZN

```
.SUBCKT INV_X1 I ZN VDD VNW VPW VSS x0=1000
*.PININFO I:I ZN:O VDD:P VNW:P VPW:P VSS:G
*.ORDERING_0_PUP M_i_1 VDD ZN
*.ORDERING_0_PDN M_i_0 VSS ZN
*.EQN ZN_0 =!I
M_i_0 ZN_0 I VSS VPW nfet W=0.288000U L=0.020000U nfin=7
M_i_1 ZN_0 I VDD VNW pfet W=0.288000U L=0.020000U nfin=7
RB1 I ZN_0 x0
RO1 ZN_0 ZN 50
.ENDS
```

Resistive Open

- Inverter - 2 defect models with resistive open , user input - 40 nm

- Example:
  I - 28 nm

```
.SUBCKT INV_X1 I ZN VDD VNW VPW VSS x0=1000
*.PININFO I:I ZN:O VDD:P VNW:P VPW:P VSS:G
*.ORDERING_0_PUP M_i_1 VDD ZN
*.ORDERING_0_PDN M_i_0 VSS ZN
*.EQN ZN=!I
M_i_0 ZN I VSS VPW nfet W=0.288000U L=0.020000U nfin=7
M_i_1 ZN I VDD VNW pfet W=0.288000U L=0.020000U nfin=7
RO1 I N1 x0
.ENDS
```

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Summary

- Small delay defects increases at field level → results in early life failure
  - One of the sources : physical defects like resistive bridge, resistive open
- Demand for higher quality tests
- Cell-Aware Test
  - Testing the cell using the layout information
- Tool developed - to generate efficient & realistic defect models with resistive bridge & resistive open

Future Work

- Analysis of small delays
- Running transient analysis
  - Cell instantiation with defect models
  - Different resistance values

THANK YOU