Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: III**
Title of the Course	**: Digital Electronics**	**Course Code**	**: ECB 202**
Time: 3 Hours		**Maximum Marks: 50**	

Note: 1. Do not write anything on the question paper except Roll number.
2. Attempt the question as per the order of section as well as question number.

Section A: Answer the 10 multiple choice questions. Each question carries 01 mark. **[10×1=10]**

A1. Each term in the standard SOP form is called a

a) minterm b) maxterm c) don't care d) literal

A2. The dual of a Boolean expression is obtained by

a) interchanging all 0s and 1s
b) interchanging all 0s and 1s, all + and '.' signs
c) interchanging all 0s and 1s, all + and '.' signs and complementing all the variables
d) interchanging all + and '.' signs and complementing all the variables

A3. In BCD addition, 0110 is required to be added to the sum for getting the correct result, if

a) the sum of two BCD numbers is not a valid BCD number
b) the sum of two BCD numbers is not a valid BCD number or a carry is produced
c) a carry is produced
d) none of the above is true

A4. The logic gate used in parity checkers is

a) NOR b) NAND c) X-OR d) X-NOR

A5. When a flip-flop is reset, its output will be

a) $Q = 0, \overline{Q} = 0$ c) $Q = 0, \overline{Q} = 1$
b) $Q = 1, \overline{Q} = 1$ d) $Q = 1, \overline{Q} = 0$

A6. A mod-2 counter followed by a mod-5 counter is

a) the same as a mod-5 counter followed by a mod-2 counter
b) a decade counter
c) a mod-7 counter
d) none of the above

A7. The characteristic equation of a J-K flip-flop is

a) $Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$ c) $Q_{n+1} = \overline{J}Q_n + \overline{K}Q_n$
b) $Q_{n+1} = JQ_n + K\overline{Q}_n$ d) $Q_{n+1} = \overline{J}\overline{Q}_n + KQ_n$
e)

A8. A combinational PLD with fixed OR array and programmable AND array is called a

a) PROM b) PAL c) PLA d) EPROM

A9. The decimal equivalent of the highest possible address for an 8-bit address bus is

a) 8 b) 128 c) 255 d) 127

A10. The output of a clocked sequential circuit is independent of the input. The circuit can be represented by

a) Mealy model
b) Moore model
c) Either Mealy or Moore model
d) Neither Mealy or Moore model

Section B: Answer any 4 questions. Each question carries 05 mark. **[4×5=20]**

B1. Design a 4- bit binary to gray code converter using a PLA.

B2. Explain the mealy and moore model of FSM with the help of an example.

B3. Design a combinational circuit using basic logic gates which accepts a 3-bit binary number and generates an output binary number equal to the square of the input number.

B4. Implement a full subtractor using PROM.

B5. Convert the S-R flip-flop into J-K flip-flop.

Section C: Answer any 2 questions. Each question carries 10 mark. **[2×10=20]**

C1. Design a 4-bit Bi-Directional shift register. Explain its working with the help of an example.

C2. Design a synchronous MOD-6 binary up counter using J-K Flip-flop.

C3. A staircase light is controlled by two switches; one is at the top of the stairs and the other at the bottom of the stairs.

a) Make a truth table for this system.
b) Write the logic equation in the SOP form.
c) Realize the circuit using AOI logic.
d) Realize the circuit using minimum number of NAND gates.

********** END OF THE QUESTION PAPER **********