Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech (Make Up)

Branch	**: ECE**	**Semester**	**: IV**
Title of the Course	**: Analog Electronics**	**Course Code**	**: ECB 252**

Time: 3 Hours **Maximum Marks: 50**

Note:

- **Questions are printed on BOTH sides. Answers should be CLEAR AND TO THE POINT.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**

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1. If a Si transistor used in the circuit (Figure 1) has minimum value of $\beta = h_{fe} = 30$ then determine whether the transistor is in cutoff, active or saturation region for $V_1 = 12V, V_2 = -12V, V_{cc} = 12V, R_1 = 15K, R_2 = 100K, R_c = 2.2K$. Also find output V_0. **[5]**

2. Figure 2, shows the CB hybrid model. Find, h_{re} in terms of CB h parameter. **[5]**

3. Find the voltage gain (A_{vsf}) with feedback by taking source and load resistances in account of the circuit in figure 3. Also find R_{if} for the same circuit as well. Draw the small equivalent circuit model of the circuit given. **[2+2]** **[2]**

4. Write short notes on following:
   (a) Transistor switching times **[2]**
   (b) Graphical analysis of transistor biasing **[4]**
   (c) Collector- Emitter feedback bias circuit **[3]**

5. (a) What do you mean by feedback? **[2]**
   (b) What are the advantages of negative feedback? **[1]**
   (c) Define in details the four different classifications of basic amplifier. **[4x2=8]**

6. In the circuit shown in Fig. 4, V_{CC}= 24V, R_C= 10 KΩ and R_E= 270 Ω. If a Si transistor is used with β =45 and at quiescent condition, V_{CE}= 5V, determine (a) value of R (b) stability factor. **[2+2]**

7. **Put *"Tick (√)" Marks* or Write T/ F on the write option wherever applicable (Bold).** **[10]**

(a) A capacitor stores, **charge/energy/current.**

(b) The **blocking/coupling/bypass** capacitor prevents the flow of dc current from the collector circuit to load resistance.

(c) In a transistor, if the impedance between collector and emitter terminal is viewed as finite then the transistor is in **saturation/cutoff/ideal** region.

(d) Usually in a transistor, $R_b \approx 10R_c$ will drive into **weak saturation/hard cut off/hard saturation** region.

(e) Turn-on-time for a transistor = delay time + storage time. **(T/F)**

(f) Alloy is made up of compound semiconductors. **(T/F).**

(g) White noise provides variation over BW. **(T/F)**

(h) Stability factor of self-bias circuit is worst among other biasing circuits. **(T/F)**

(i) Sensistor has negative temperature coefficient. **(T/F)**

(j) Cascading and cascoding are same arrangement of transistor configurations. **(T/F)**

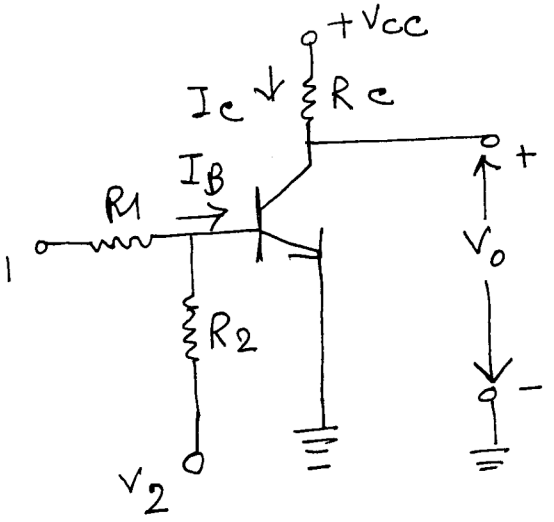

Figure 1.

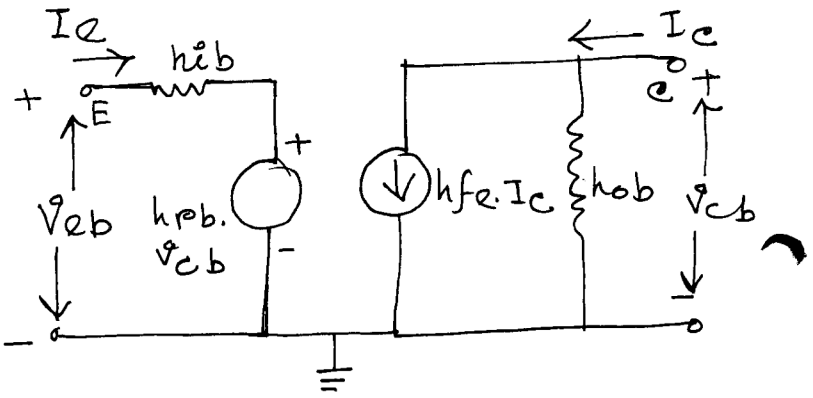

Figure 2

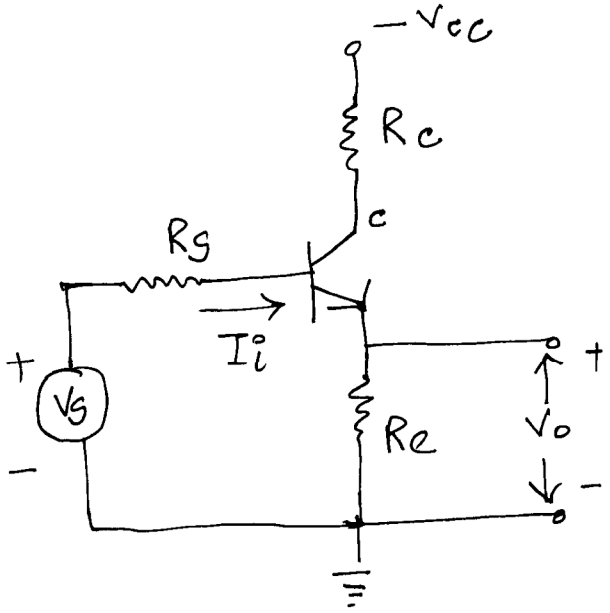

Figure 3

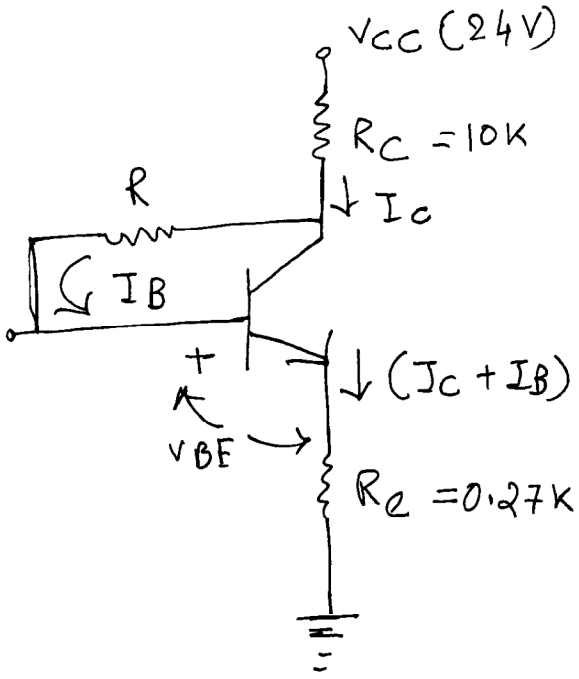

Figure 4