Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Mid-Semester Examination March, 2019

Branch	**: ECE**	**Semester**	**: 3rd**
Title of the Course	**: Basics of VLSI**	**Course Code**	**: ECB 351**

Time: 2 Hours **Maximum Marks: 25**

Note : Write appropriate answer only.

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1. Draw a CMOS inverter circuit. In this circuit, it is seen that the transistors operate in various region of operations. Draw voltage-transfer characteristics (VTC) of the inverter and show portions of the characteristics (say, for example, A, B, C, D, and E) along with region of operations for both transistors. Justify the region of operation of the transistors while V_{in}=0 and V_{out}=V_{DD} using output characteristics of PMOS and NMOS. **1+1+1+2=5**
2. What do you understand by noise margins of an inverter circuits? Show how V_{IL}, V_{OL}, V_{OH} and V_{IH} are depicted on VTC of a CMOS inverter. If V_{OH}=5 V, V_{IH}=4.25 V, V_{OL}=0.25 V, NM_L=1V, Find NM_H and V_{IL}. **2+1+2=5**
3. Write down the advantages of Pseudo NMOS logic circuits over its CMOS counterparts. Implement $f = \overline{ABC + DE}$ using Pseudo NMOS and CMOS circuit technique. **1+2+2=5**
4. Write the expression for threshold voltage of the NMOS transistor. Explain each and every terms involved therein. What is the body effect? An NMOS transistor has parameters V_{TN0}= 0.75 V, γ =0.5 $V^{1/2}$ and Φ_f=0.25 V. Find the value of V_{SB} at which the threshold voltage becomes 1V. **1+1+1+2=5**
5. Find the Boolean expression for output f. Implement whole circuit using either (1) DCVSL or (2) CPTL or (3) Transmission gate logic or (4) any other such technology that have been taught in the class. Assume that all inputs and their complement's form are available. **1+4=5**