(36)

Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: IV**
Title of the Course	**:Analog Electronics**	**Course Code**	**: ECB252**
Time: 1.5 Hours		**Maximum Marks: 25**	

- **Answers should be CLEAR ANDTO THE POINT.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**

01. For the circuit shown in Fig. 1, measurement indicates that V_B = -1.5 V. **[4 +1 + 2]**

(a) Assuming V_{BE} = 0.7 V, calculate V_E, α, β, and V_C.
(b) In which mode transistor is operating?
(c) If a transistor is used with $\beta = \infty$, what values of V_B, V_E, and V_C will result?

02. Determine the minimum value of the current gain β required to put the transistor in saturation mode, as shown in Fig. 2., when, V_{in} = +5 V, V_{BE} (sat) = 0.8 V and V_{CE} (sat) = 0.12 V. **[3]**

03. In CE mode of transistor operation, the dc current gain is defined as, $\beta dc = I_C/I_B = h_{fE}$ and the small signal forward current gain is defined as, $\beta_{ac} = \beta' = \frac{\delta I_C}{\delta I_B}|V_{CE} = h_{fe}$. Now β_{ac} and βdc are related as, $\beta' = \beta + (I_{CBO} + I_B)\frac{\delta\beta}{\delta I_B}$, where symbols have their usual meaning: **[2+2]**

At what condition the following relation will hold:

$$\frac{h_{fe} - h_{fE}}{h_{fe}} = \frac{I_C}{h_{FE}} \cdot \frac{\delta h_{FE}}{\delta I_C}$$

04. For a self-bias circuit, as shown in Fig. 3., the Q-point is assumed to be exactly at the middle of the dc loaded line. **[2+4]**

(a) What will be expression for the total combination of R_c and R_e, in terms of V_{CC} and power dissipation at Q-point P_{DQ}.
(b) In the circuit, the ac-dynamic resistance r_e' appears in series with R_e. For any collector bias voltage $3V \leq V_C \leq V_{CEQ(max)}$, the voltage drop across the R_E and R_C at $I_C \approx I_E = I_{CEQ}$ could be assumed 10% and 40% of V_{CC} respectively. Will it be sufficient to nullify the effect of dynamic emitter resistance, r_e', on the thermal instability?

05. (a) Determine the quiescent current and collector-to-emitter voltage for a Ge transistor with $\beta = 50$, in the self-biasing arrangement of Fig. 4. The circuit component values are V_{CC} = 20 V, R_C = 2k, R_e = 0.1k, R_1 = 100 k and R_2 = 5k. **[5]**

(b) Find the stability factor S.

```
FROM EMP, PROJ, ASG,PAY
WHERE EMP.ENO = ASG.ENO
AND EMP.TITLE = PAY.TITLE
AND (BUDGET>200000 OR DUR>24)
AND ASG.PNO = PROJ.PNO
AND (DUR>24 OR PNAME = "CAD/CAM")
```

Compose the selection predicate corresponding to the WHERE clause and transform it, using the idempotency rules, into the simplest equivalent form. Furthermore, compose an operator tree corresponding to the query and transform it, using relational algebra transformation rules, to its (three) equivalent forms.