Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: IV**
Title of the Course	**: Analog Electronics**	**Course Code**	**: ECB 252**
Time: 2 Hours		**Maximum Marks: 25**	

- **Questions are printed on BOTH sides. Answers should be CLEAR AND TO THE POINT.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**

---

1. In the Darlington stage shown in figure 1, $V_C = 24$ V, $\beta_1 = 24$, $\beta_2 = 39$, $V_{BE} = 0.6$ V, $R_C =$ 330 Ω and $R_E = 120$ Ω. If at the Q-pt, $V_{CE2} = 6$ V, determine (a) value of resistance R, (b) stability factor $S = d_{IC}/d_{ICO1}$. [4]

2. Given in the two-battery transistor circuit in figure 2, find the expression for stability factor, S. You may neglect V_{BE}. [2]

3. Calculate I_C, I_B and h_{fE} for the switching circuit as shown in figure 3, when Q_1 is switched into saturation. [2]

4. Given the load line plot with defined Q-pt in figure 4, determine the values of V_{CC}, R_C and R_B for a fixed bias configuration of transistor. [3]

5. For the emitter bias network shown in figure 5, determine (a) I_B, (b) I_C, (c) V_{CE}, (d) V_C and (e) V_E. [5]

6. Determine the quiescent currents (I_E, I_B and I_C) and the Collector- Emitter voltage for Ge transistor with $\beta = 50$ in the self-biasing arrangement as shown in figure 6, where, $V_{CC} = 20$V, $R_C = 2$K, $R_E = 0.1$ K, $R_1 = 100$K $R_2 = 5$ K and $V_{BE} = 0.2$ V. Also find the stability factor S. [5]

7. Write True (T)/ False (F) only, against each of the following statements: [1x4 = 4]

   (a) In h-parameter equivalent model of transistor, h-parameters are both real and imaginary number.

   (b) Compensation bias techniques refer to use of temperature sensitive devices.

   (c) For input signal, having magnitude greater than V_{BE}, transistor will always be driven in cut off region.

   (d) Transistor means transfer of resistance.

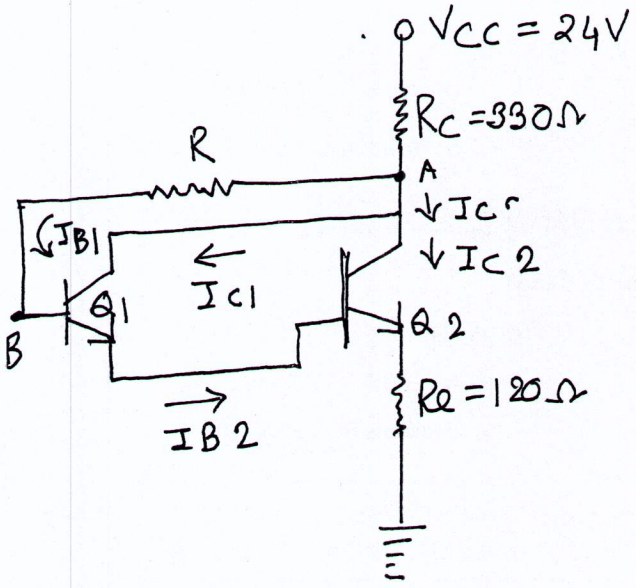

Figure 1

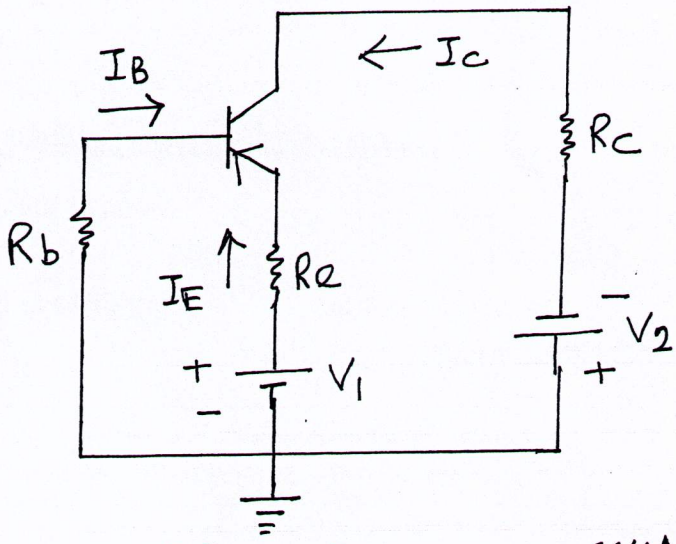

Figure 2

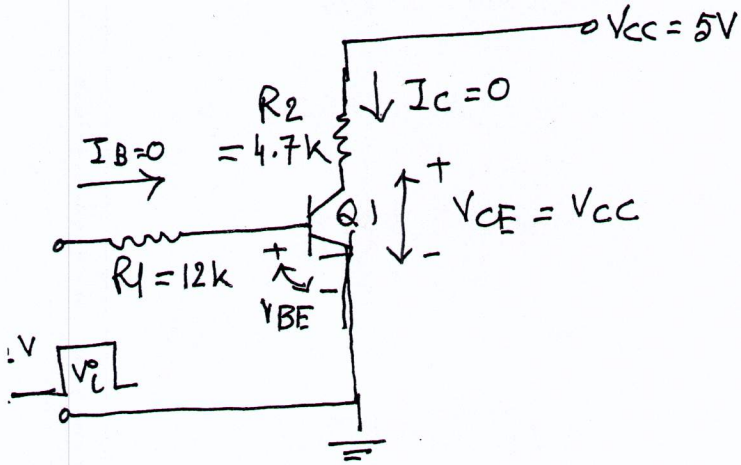

Figure 3

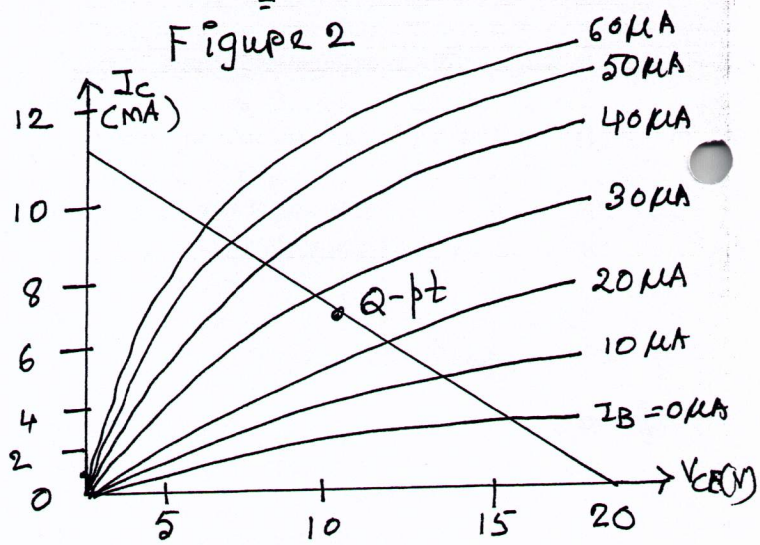

Figure 4

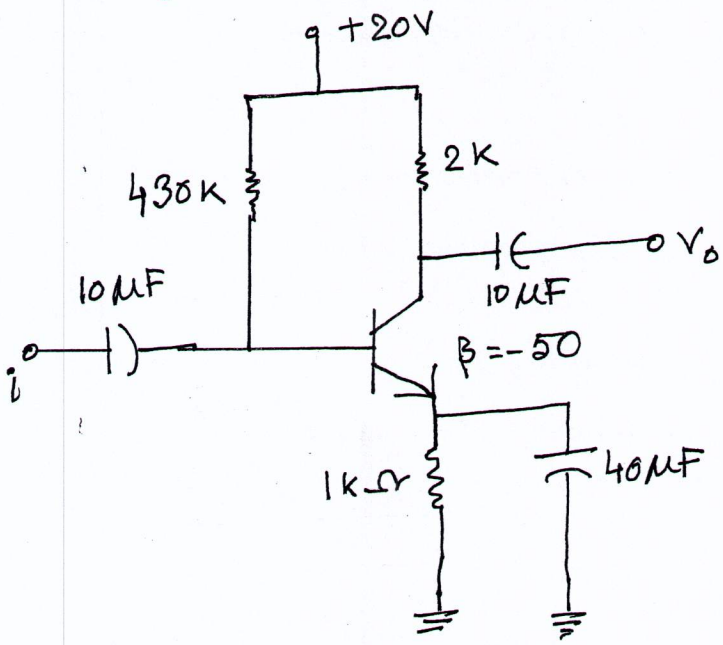

Figure 5

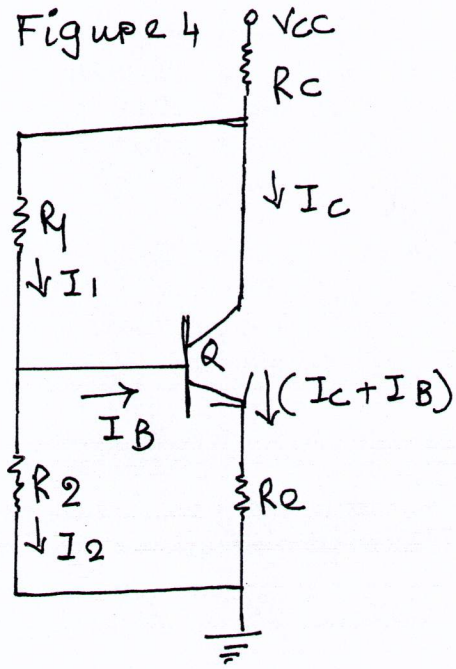

Figure 6