Roll No.:.....

National Institute of Technology, Delhi

End Semester Examination, May 2022

Branch	: ECE	Semester	: VI
Title of the Course	: Basics of VLSI	Course Code	: ECB 351
Time	: 3 Hours	Maximum Marks	: 50

Section I

Attempt all questions (2x5)

1. Define Logical effort.
2. Write short note on delay time for CMOS inverter.
3. Implement two input AND and NAND gate using DCVSL logic.
4. Design 2 input XOR using CMOS transmission gate.
5. Draw and explain MOSFET I-V characteristic.

Section II

Attempt any five questions (5x5)

6. Why transistor scaling is of great importance in VLSI? Write down comparison between constant field scaling and constant voltage scaling.

7. Draw circuit diagram to implement the following function. Also draw its layout using colour coding.
$Y = [(A+B).C]'$

8. Explain types of power consumption in detail.

9. Explain the concept of RC delay model and what are the limitations of logical effort

10. Explain any one of the following
(a) VTCMOS technique
(b) MTCMOS technique

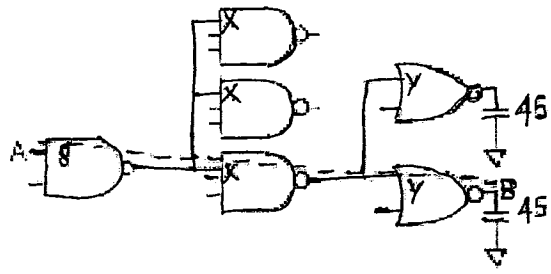
11. What is charge leakage and charge sharing issue in dynamic logic. How these can be removed in dynamic CMOS circuits.

12. Explain Pass transistor logic (PTL). How it is used to transfer logic '1' and logic '0'.

Section III

Attempt any two questions (7.2x2)

13. Estimate the minimum delay of the path from *A* to *B* in Figure, using logical effort and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width.



14. Explain Read/Write operation of SRAM memory cell. How a 1-bit cell is used in bigger memory systems.

15. Draw neat diagram DRAM and also explain its working in detail. What are the advantages and disadvantages of this design.