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National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch : ECE **Semester : Vth**

Title of the Course : Digital System Design **Course Code : EC305**

Time: 3 Hours **Maximum Marks: 50**

Note: Question paper consist of three sections

1. **Section A: Contains one (01) question comprising of 10 parts of 01 mark each and all parts are compulsory.**
2. **Section B: Contains Five (05) questions of five (05) marks each any four (04) are to be attempted.**
3. **Section C: Contains Three (03) questions of ten (10) marks each and any two (02) are to be attempted.**

Section –A (**Attempt all the Questions**)

1. How will you compare component declaration and component instantiation. **[1]**
2. Write a program for the simulation of a Tri-state buffer, using behaviour modelling? **[1]**
3. Differentiate between a process and a wait statement. Can they be used simultaneously in a program? **[1]**
4. What is the difference between function and procedures in VHDL? Give suitable example. **[1]**
5. Write Dataflow model of 3-bit binary to gray code converter. **[1]**
6. Explain Moore and Mealy circuits with the help of diagram. **[1]**
7. What is ASM chart and why it is used in VHDL? **[1]**
8. What are the standard values used to support multivalued logic in VHDL. **[1]**
9. What is the package body and package declaration? **[1]**
10. What are generics and why they are being used? **[1]**

Section-B (**Attempt any four Questions**)

11. Derive the state diagram and state table for an FSM that has an input w and an output z. The machine has to generate $z = 1$ when the previous four values of w were 1001 or 1111; otherwise , $z = 0$. Overlapping input patterns are allowed. An input and output sequence of the desired behaviour is: **[5]**

    w: 0101111001100111111

    z: 0000001001000100 11

12. Assume that there are three devices in the system, D_1, D_2, D_3. The request signals are named r_1 , r_2 , r_3 and the grant signals are called g_1, g_2 , *and* g_3. The devices are assigned a priority level such that D_1 has the highest priority, D_2 has the next highest and D_3 has the lowest priority. Thus if more than one request signal is asserted when the FSM assigns a grant, the grant is given to the requesting device that has the highest priority. Represent the specified arbiter FSM in form of an ASM chart. **[5]**
13. (a) if $A = 00001111$. find out value of *A srl-4*

    (b) Explain with example that how a component can be made more general using generics. **[2.5+2.5]**
14. Write down the truth table and VHDL code(structural modelling) for the four bit up/down counter. Also draw the circuit and output wave form. **[5]**

15. A VHDL entity has inputs ***A*** and ***B*** , and outputs ***C*** and ***D***. ***A*** and ***B*** are initially high. Whenever ***A*** goes low, ***C*** will go high 5 ns later, and if ***A*** changes again, ***C*** will change 5ns later. ***D*** will change if ***B*** does not change for 3 ns after ***A*** changes.
(a) Write the VHDL architecture with a process that determines the outputs ***C*** and ***D***.
(b) Write another process to check that ***B*** is stable 2ns before and 1 ns after ***A*** goes high. The process should also report an error if B goes low for a time interval less than 10ns. **[2+3]**

Section-C (**Attempt any two Questions**)

16. (a) Design a circuit for control of lights used to start a race, which works as follows. There are three inputs: Reset, Start and Clock. There are three outputs: Red, Yellow and green which turn on the lights. Only one light can be on at any time. The reset signal forces the circuit into a state in which the red light is turn on. When the start signal is activated, the red light stays on for atleast one second longer, and then the yellow light is turn on. The yellow light stays turn on about one sec and then the green light is turn on. The green light stays on for atleast three seconds and then the Red light is turned on and the circuit returns to its reset state.

(b) Write VHDL code that can be used to synthesize the circuit specified in above problem. **[5+5]**

17. Represent the FSM in fig:1 in the form of an ASM chart and write the VHDL code for a given FSM. **[10]**

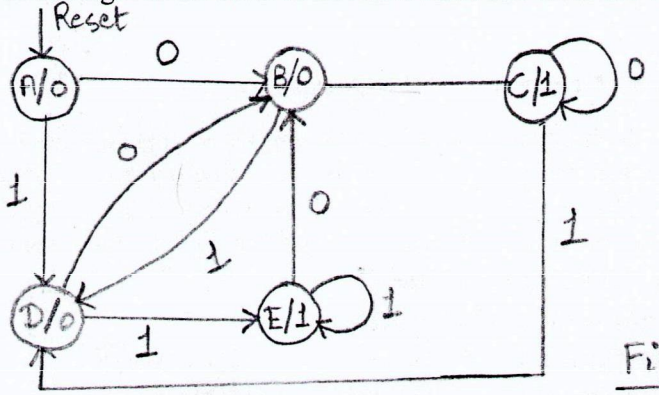

Figure: 1

18. A Moore sequential machine with two inputs(X_1 and X_2) and one output Z has the following state table:

Present State	Next State $X_1\ X_2$=00	01	10	11	Output (Z)
1	1	2	2	1	0
2	2	1	2	1	1

Write VHDL code that describes the machine at the behavioral level. Assume that state changes occur 10ns after the falling edge of the clock, and output changes occur 10 ns after the state changes. **[10]**