Roll No.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

End-Semester Examination May, 2019

Branch : EEE

Semester : 4th

Title of the Course : Digital Electronics & Logic Design

Course Code : CSB 254

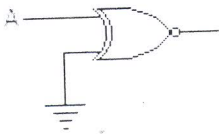
Time: 3 Hours

Maximum Marks: 50

Note: Attempt any complete five questions.

Q1. All questions are compulsory. 1x10=10

(a) For the gate in the given figure the output will be .....



(b) A device which converts BCD to seven segments is called .....

(c) Decimal number 10 is equal to binary number .....

(d) An OR gate has 4 inputs. One input is high and the other three are low. The output is .....

(e) BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are .....

(f) Define latch.

(g) List two applications of Flip-Flop.

(h) What is meant by parity bit?

(i) What is code conversion?

(j) Define memory.

Q2(a) Draw the multiple-level NOR circuit for the following expression: 1x5=5

$$CD(B+C)A+(BC'+DE')$$

Q2(b) Define full adder and full subtractor with its truth table and logic diagram. 1x5=5

Q3(a). What do you mean by Flip-Flop? Explain all four types with its truth table and diagram. 1x5=5 1x5=5

Q3(b). Define the term counter and register? Also explain ripple and synchronous counters with four-bit counter block diagram. 1x5=5

Q4(a). Simplify the following functions and implement them with two-level NOR gate circuit 1x5=5

(*i*) $F = wx' + y'z' + w'yz'$ (*ii*) $F(w,x,y,z) = \sum(0,3,12,15)$

Q4(b). Show that the dual of that exclusive-OR is also its complement. 1x5=5

Q5(a). Implement the following Boolean expression with exclusive-OR and AND gate. 1x5=5

$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$

Q5(b). Design a combinational circuit with three inputs and one output using following condition- The output is 1 when the binary value of the input is less than 3. The output is 0 otherwise. 1x5=5

Q6(a). Design a four-bit binary synchronous counter with D flip-flops. 1x5=5

OR

What do you mean by shift register? Explain with four-bit shift register.

Q6(b). What do you understand by shift decoder? Explain its three-to-eight-line decoder structure. 1x5=5