Roll No.:.....

National Institute of Technology, Delhi

End Semester Examination (Spring, 2022)

Branch	**: ECE**	**Semester**	**: IV**
Title of the Course	**: DIGITAL ELECTRONICS & LOGIC DESIGN**	**Course Code**	**: ECB 257**
Time	**: 3 Hours**	**Maximum Marks**	**: 50**

- **All questions are compulsory.**
- This question paper comprises **three sections, A, B and C.**
  - **Section A**: Contains 5 questions of 1 marks each.
  - **Section B**: Contains 3 questions of 5 marks each.
  - **Section C:** Contains 3 questions of 10 marks each.
- All questions should be answered in the same sequence as mentioned in the paper: You have to answer Q1 first, then Q2, so on, and finally Q 11. **ELSE QUESTIONS SHALL NOT BE EVALUATED.**

Section A

Q1. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of bulb resembles **[1]**

1. AND gate
2. OR gate
3. XOR gate
4. NOR gate

Q2. The minimum number of NAND gates required to implement the Boolean function A+AB'+AB'C is equal to **[1]**

1. 2
2. 3
3. 0
4. 1

Note: X' implies complement of X

Q3. Indicate which of the following logic gates can be used to realize all possible combinational Logic functions. **[1]**

1. OR gate only
2. XOR gate only

3. NAND gate only
4. AND gate only

Q4. Which of the following gates is known as a coincidence detector? [1]
1. XOR gate
2. XNOR gate
3. NOT gate
4. NOR gate

Q5. Which of the following is the output of XOR gate with inputs A and B. [1]
1. A'B + AB'
2. AB + A'B'
3. AB + A'B
4. A'B'

Note: X' implies complement of X

Section B

Q6. Design the logic circuit for half adder, full adder, and full subtractor. **[1+2+2]**

Q7. Clearly differentiate between the following concepts **[2+2+1]**
1. Combinational and sequential circuits
2. Flip flop and Latch
3. Level triggered and edge triggered flip flop

Q8. Explain race around condition? Suggest at least two methods to overcome race around conditions. **[2+3]**

Section C

Q9. Design 8×1 MUX using 2×1 MUX which select the min terms 1, 3, 5, 6, 7, 13, 15 **[10]**

Q10. Convert JK flip flop into AB flip flop, where the truth table of AB flip flop is given as **[10]**

A	B	Q_{n+1}
0	0	1
0	1	Q_n
1	0	Q_n'
1	1	0

Note: Q_n' implies complement of Q_n

Q11. Minimize the following boolean function **[10]**
$f(A,B,C,D,E) = \sum(0,1,6,7,8,9,21,22,23,29,31)$