Roll No.:.....

National Institute of Technology, Delhi

Mid Semester Examination: B. Tech.

Branch	**: EEE,ECE**	**Semester**	**: V**
Title of the Course	**: IC Application**	**Course Code**	**: ECB 304**
Time: 2 Hours		**Maximum Marks: 25**	

Answer all the questions

Section A

1. Draw the Block Diagram of an Op-Amp. **[One Marks]**
2. List the properties of an ideal op-amp and draw the equivalent circuit of an ideal. **[One Marks]**
3. Discuss Roll off problem in a basic integrator. What do you do to eliminate this problem? **[One Marks]**
4. What were the drawbacks of basic logarithmic amplifier circuit? **[One Marks]**
5. Draw the circuit of Voltage shunt feedback amplifier and write its closed loop voltage gain and input resistance. **[One Marks]**

Section B

1. Draw the pin diagram of IC-741 op-amp. In the voltage amplifier circuit of Fig. 1, let $V_S = 100mV$, $R_S = 100k\Omega$, $v_I = 75mV$, $R_L = 10\Omega$ and $v_0 = 2V$. If connecting a 30Ω resistance in parallel with R_L drops v_0 to 1.8V, find R_I, A_{OC} (open Loop Voltage Gain) and R_0. **[4 Marks]**

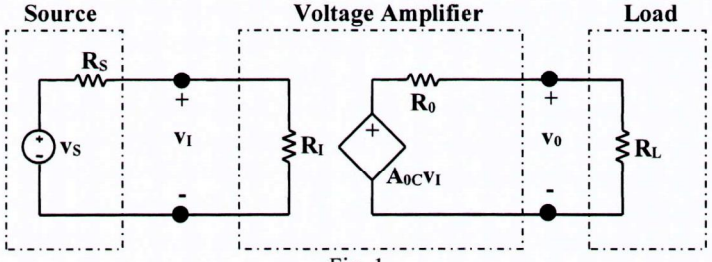

Fig. 1

2. Why is an op-amp termed as a direct coupled high gain amplifier? Explain. In the circuit of non-inverting amplifier, fig.2. let $R_1 = 100k\Omega$, $R_f = 200k\Omega$ and A (open loop gain) = ∞. (a) What is its closed-loop gain? How does its gain change if a third resistance $R_3 = 100k\Omega$ is connected in series with R_1? In parallel with R_1? In series with R_f? In parallel with R_f?

[4 Marks]

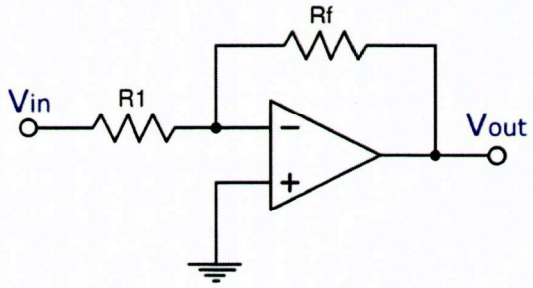

Fig. 2

3. Discuss the concept of virtual ground. Under what circumstances it cannot be applied to the op-amp? Show that the circuit of Fig. 3 has $R_i = \infty$ and $A = -\left(1+\frac{R_3}{R_4}\right)\frac{R_1}{R_2}$

[4 marks]

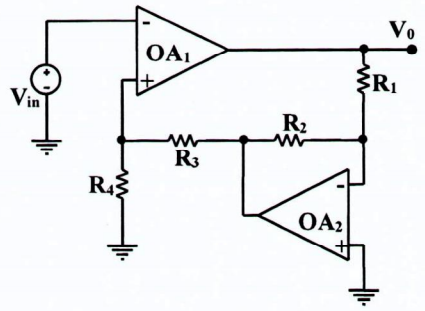

Fig. 3

4. Draw the circuit diagram of a buffer circuit. Calculate its closed loop voltage gain. Also list the applications of this circuit. Write its significance. For the circuit shown in Fig. 4, if all the resistances are equal then, prove that $V_0 = (V_2 + V_4 + V_6) - (V_1 + V_3 + V_5)$.

[4 Marks]

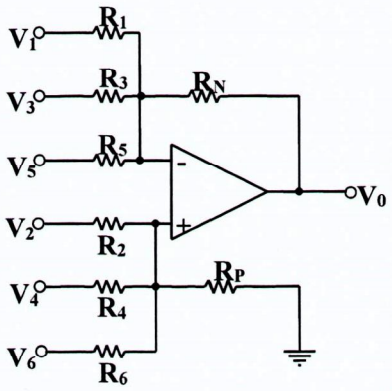

Fig. 4

5. What circuit is used at the output stage of an operational amplifier? Write its significance. Derive an expression for the single Op-Amp logarithmic amplifier and explain its operation.

[4 Marks]