RollNo.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch	**: ECE**	**Semester**	**: Vth**
Title of the Course	**: Digital System Design**	**Course Code**	**: EC305**

Time: 2 Hours **Maximum Marks: 30**

Note: All the questions are Compulsory

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1. (a) Write a selected signal assignment statement to represent the 4:1 MUX shown in figure 1. Assume that there is an inherent delay in the MUX that causes the change in output to occur 10ns after a change in input.
   (b) Repeat (a) using a process and a case statement in VHDL. **[4]**

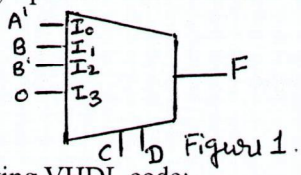


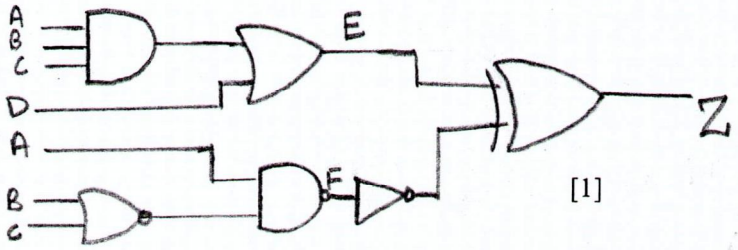
Figure 1.

2. Consider the following VHDL code:

```
entity Q3 is
   port(A, B, C, F, Clk: in bit;
        E: out bit);
  end Q3;
architecture Qint of Q3 is
  signal D, G: bit;
begin
   process (clk)
   begin
      if Clk'event and Clk = '1' then
        D <= A and B and C;
        G <= not A and not B;
        E <= D or G or F;
      end if;
   end process;
end Qint;
```

(a) Draw the circuit generated by the preceding code (at the gate level) **[2]**

(b) Write a VHDL description of the combinational circuit shown in figure 2, using concurrent statements. Each gate has a 5 ns delay, excluding the inverter, which has a 2 ns delay. **[3]**



[1]

Figure 2.

3. A 4-bit magnitude comparator chip (e.g., 74LS85) compares two 4-bit numbers A and B and produces outputs to indicate whether *A<B, A=B, or A>B.* There are three output signals to indicate each of the above conditions. Note that exactly one of the output lines will be high and other two lines will be low at any time. The chip is a cascadable chip and has three inputs, *A > B.IN, A=B.IN, and A<B.IN,* in order to allow cascading the chip to make 8-bit or bigger magnitude comparators.
   (a) Write behavioral VHDL description for the 4-bit comparator.
   (b) Draw a block diagram to indicate how you can construct an 8-bit magnitude comparator using two 4-bit magnitude comparators. **[4]**

4. Draw the signal driver for signal Z. The signal assignment statements for signal Z are:

```
Process
   Begin
    Z <= 18 after 5 ns;                          (i)
    Z <= reject 10 ns inertial 22 after 20 ns;   (ii)
    Z <= 33 after 12 ns;                         (iii)
   Wait;
  end process;
```

[2]

5. What will be the result of the operation given below:
   "01010101" sla 3 **[2]**

6. What are various design stages in designing a digital system? Prove how VHDL is capable of releasing the purpose of each design stage? **[3]**

7. Write a behavioral model for D-type rising-edge-triggered flip-flop that reports error for setup and hold time violation. Assume set up time= hold time=5ns and display text string as violation of set up or hold time. **[3]**

8. An M-N flip-flop responds to the falling clock edge as follows:

   If *M* = *N*= '0', the flip-flop changes state.

   If *M* = *'0'* and *N*= '1', the flip-flop output is set to '1'.

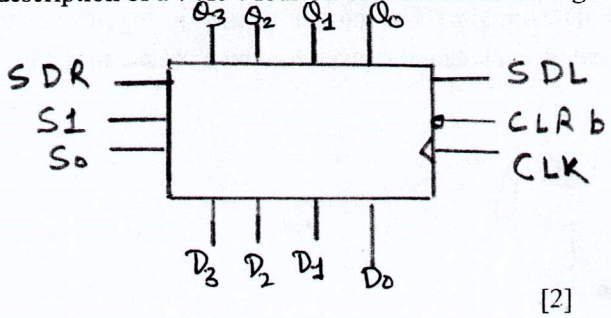
   If *M* = *'1'* and *N*= '0', the flip-flop output is set to '0'.

   If *M* = *N*= '1', no change of flip-flop state occurs.

   The flip-flop is cleared asynchronously if *CLRn* = '0'.

   Write a complete VHDL module that implements an M-N flip-flop. **[3]**

9. A description of a 74194 four-bit bidirectional shift register shown in figure 3:



[2]

Figure 3.

The CLRb input is asynchronous and active low and overrides all the other control inputs. All other state changes occur following the rising edge of the clock. If the control inputs $S_1 = S_0 = 1$, the register is loaded in parallel. If $S_1=1$ and $S_0=0$, the register is shifted right and SDR (serial data right) is shifted into Q_3. If $S_1=0$ and $S_0=1$, the register is shifted left and SDL is shifted into Q_0. If $S_1 = S_0 = 0$, no action occurs.

Write a behavioral-level VHDL model for the 74194. **[4]**

[3]