ripeded robil (March 12, 2018) (Morning Roll No.:....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch

: ECE

Semester

: VIth

: 25

Title of the Course

: Basic of VLSI

Course Code

: ECB 351

Time

: 2 Hours

Maximum Marks

Note: All questions are compulsory.

- What is the threshold voltage of MOS transistor? Derive the expression for PMOS.
- 2. Derive the expression of drain current I_d for an NMOS transistor in saturation region. 3
- 3. Calculate the power dissipation in CMOS inverter if $C_{load} = 2pF$ and VDD = 5V and 2 the switching frequency of the inverter is 100KHz.
- 4. Discuss the operation of enhancement mode NMOS transistor with suitable diagrams. 3
- 5. Derive the expressions for noise margins of CMOS inverter.

5

3

6. Briefly explain the following with suitable diagrams

 $3 \times 2 = 6$

3

- a. Body bias effect
- b. Short channel effect
- c. Latch-up effect
- 7. Design the circuit with p-channel MOSFET as shown in figure 1. to meet the below specification.

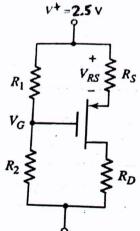
 $K_p = 100 \ \mu A/V^2$, VTP = -0.4V

 $I_{D} = 100 \mu A$

 $V_{SD} = 3V$,

 $V_{RS} = 0.8V$

Figure 1



= -2.5 V