

National Institute of Technology, Delhi

Roll No.:

Name of the Examination: B. Tech

Branch : ~~ECF~~ & EEE & CSE

Semester : III

Title of the Course : Analog Electronics

Course Code : ECB 206

Time: 3 Hours

Maximum Marks: 50

Note:

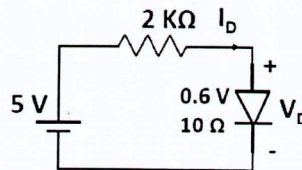
- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

Section A

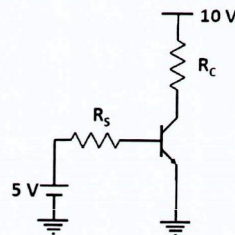
Q 1 Solve the following problems

(2×5)

- What is Zener diode? Explain, how it works as voltage regulator with the help of its VI-characteristics.
- Calculate I_D and V_D in the circuit shown below.



- A silicon transistor with $V_{BE,sat} = 0.8$ V, $\beta = 100$, $V_{CE,sat} = 0.2$ V and $R_S = 200$ KΩ is used in the circuit shown below. Find the minimum value of R_C for which the transistor will remain in the saturation.

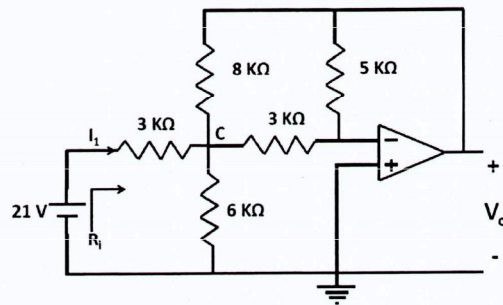


- Determine the output voltage of an op-amp for the input voltages of 150μ V and 140μ V, if the differential gain is 4000 and value of CMRR is 10^5 .
- Sketch the circuit diagrams of the voltage series and shunt feedback amplifiers by using op-amp and potential divider network.

Section B

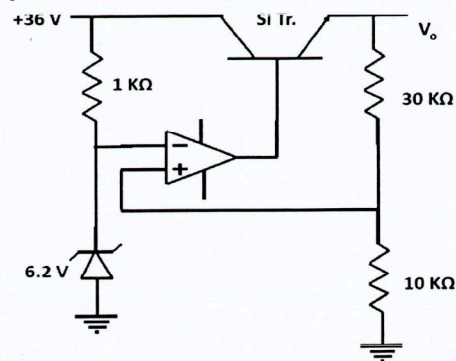
Q 2 Find, I_L , R_L , V_c and V_o for circuit shown below.

(5)



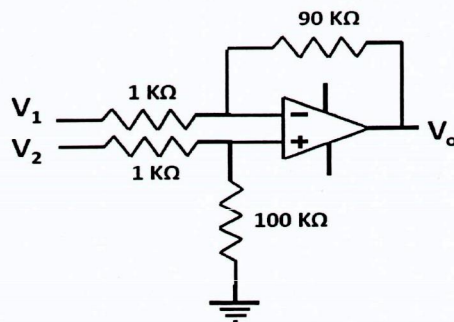
Q 3 (a) Find the output V_o for the series regulator circuit shown below.

(2.5)



(b) Find differential gain, common mode gain and CMRR of the OPAMP circuit shown below.

(2.5)

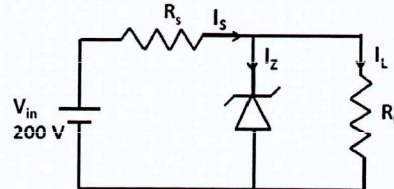


Q 4 A 50 V, 5 to 40 mA is used as shown in the regulator circuit-

(2.5+2.5)

(a) Calculate R_s to allow voltage regulation from $I_L = 0$ to I_{Lmax} . Also calculate I_{Lmax} value?

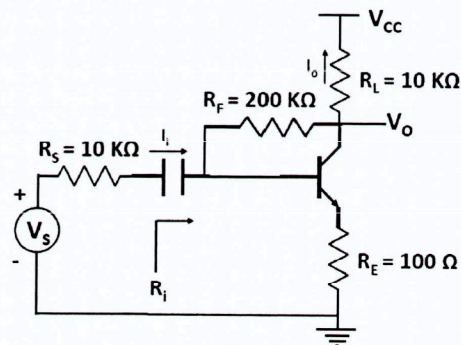
- (b) If R_s is set as found in part (a) and I_L is fixed at 25 mA, then what is the permissible range of V_{in} for Zener diode to act as regulator safely?



- Q 5 Assume that a Si transistor with $\beta = 50$, $V_{BE,active} = 0.7$ V is biased using potential divider network with $V_{CC} = 22.5$ V and collector resistance $R_c = 5.6$ K Ω . It is desired to establish a Q point at $V_{CE} = 12$ V, $I_C = 1.5$ mA, and stability factor $S \leq 3$. Find the emitter resistance R_e , resistance connected between the base and supply (R_1) and resistance connected between the base and ground (R_2). (5)
- Q 6 Why do you need constant current biasing in the differential amplifier? Draw the circuit diagram of a differential amplifier using current mirror circuit and briefly discuss about the functioning of the circuit. (5)

Section C

- Q 7 For the circuit shown below, calculate $A_I = I_o/I_i$, A_V , A_{V_s} , and R_i . Assume suitable h -parameters. (10)



- Q 8 Draw the schematic diagram of Enhancement mode MOSFET. Explain its working principle along with drain characteristics and transfer characteristics curves. (10)

Q 9 For the FET amplifier shown in the circuit, calculate input impedance (Z_i), output impedance (Z_o) and voltage gain (A_v) with and without bypass capacitor (C_s). (10)

