Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch	**: ECE**	**Semester**	**: VIth**
Title of the Course	**: Basic of VLSI**	**Course Code**	**: ECB 351**
Time	**: 3 Hours**	**Maximum Marks**	**: 50**

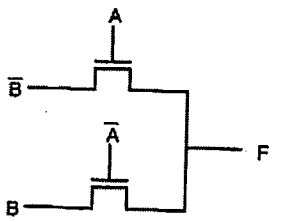
Note: All questions are compulsory.

1. Briefly explain the following with suitable diagrams 10
   (a) Channel length modulation
   (b) Short channel effects
   (c) Rise time, Fall time, Delay time
   (d) BiCMOS technology
   (e) 6T SRAM cell

2. Calculate the threshold voltage V_{T0} at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 4 \times 10^{18}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 16$Å, and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. Assume $n_i = 1.45 \times 10^{10}$ cm^{-3} and Fermi potential of polysilicon gate is 0.55 V. 5

3. Consider the circuit shown in figure 1 below. 6
   (a) Determine the logic function F.
   (b) Design a circuit to implement the same logic function by NOR gates in the transistor-level schematic using pseudo nMOS technology.
   (c) Design a circuit to implement the same logic function, in the transistor-level schematic using CMOS technology.

Figure 1



4. Consider a CMOS inverter circuit with the following parameters: 6
   $V_{DD} = 3.3$ V, $V_{TO,n} = 0.6$ V, $V_{TO,p} = -0.7$ V, $k_n = 200$ μA/V^2, $k_p = 80$ μA/V^2.
   Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{TO,n} \neq |V_{TO,p}|$ hence, it is not a symmetric inverter.

5. Explain CMOS Transmission gates. Determine the equivalent resistance in different regions of operations. 6

6. Consider the domino CMOS circuit shown in figure 2 below. Using the input voltage waveforms illustrated in figure 3, determine the output voltage waveform. 4

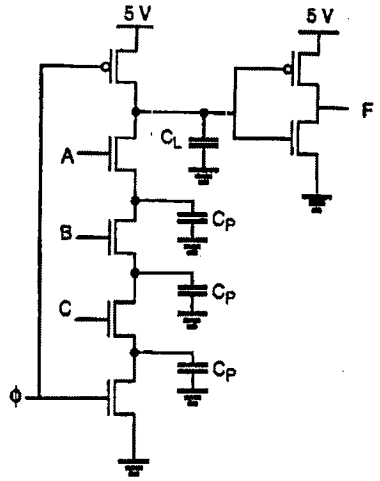


Figure 2

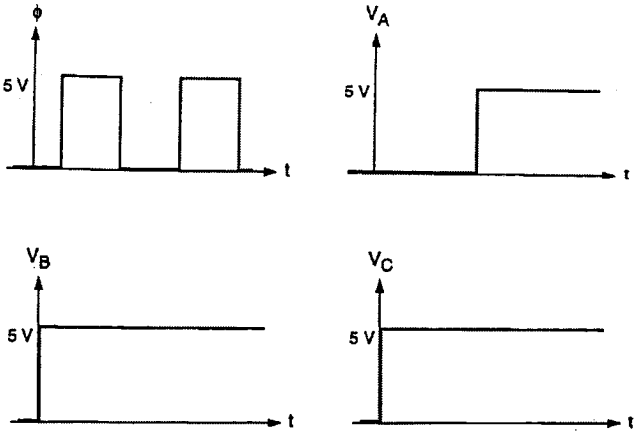
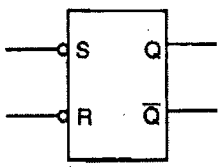


Figure 3

7. Design a circuit to implement the truth table shown in figure 4 below. 5

Figure 4

S	R	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$



8. A single transistor DRAM cell is represented by the circuit diagram in figure 5 below. The bit line can be precharged to $V_{DD}/2$ by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to V_{DD} or 0V during the WRITE operation with word line at V_{DD}. Using the parameters given 8

$V_{T0} = 1.0V$
$\gamma = 0.3\ V^{1/2}$
$|2\varphi_F| = 0.6V$

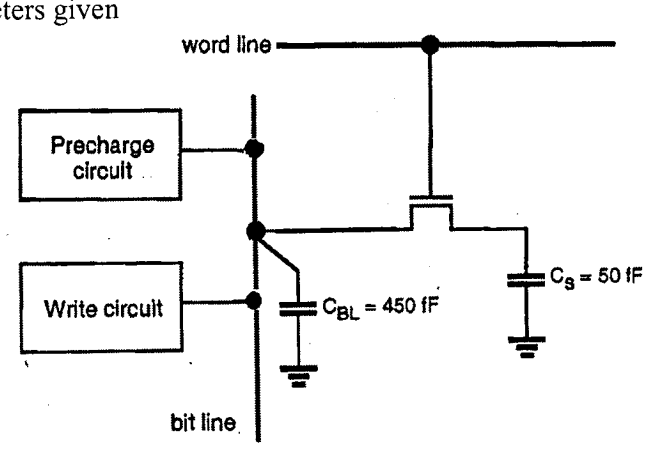


Figure 5

(a) Find the maximum voltage across the storage capacitor Cs after WRITE-I operation, i.e., when the bit line is driven to $V_{DD} = 5V$.

(b) Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-operation after the bit line is first precharged to $V_{DD}/2$