Roll No.: .....

National Institute of Technology, Delhi
Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: 4th**
Title of the Course	**: Analog Electronics**	**Course Code**	**: ECB 252**
Time: 3 Hours		**Maximum Marks: 50**	

- **Answers should be CLEAR AND TO THE POINT.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**

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1. For the ideal OPAMP shown in figure 1, what should be the value of feedback resistor, R_f, to obtain a closed loop gain of 5? **[5M]**

2. Calculate V_o and i_o of the circuit shown in figure 2. What kind of amplifier it will be? **[5M]**

3. In the series-shunt feedback amplifier shown in figure 3, calculate the voltage gain (A) without feedback and voltage gain (A_f) with feedback. **[3M]**

4. Figure 4 shows an OPAMP circuit with voltage series feedback through resistors R_1 and R_2. The internal gain of OPAMP is 5×10^4 and input impedance is 100 $k\Omega$. Find out the gain and input impedance of the amplifier with feedback. **[4M]**

5. In the transformer coupled amplifier stage as shown in figure 5, $V_{BE} = 0.5\ V, \beta = 50$ and q-point voltage is $V_{CE} = 4\ V$. Determine, (a) R_e (b) under what condition stability factor S = 1? **[3M]**

6. The bias circuit shown in figure 6, uses a Si transistor with $V_{BE} = 0.7\ V$. **[5M]**

(a) Find the collector current I_C and voltage V_{CE}, if $\beta = 60$.
(b) Find I_C and V_{CE}, if β changes to 80.
(c) What kind of biasing arrangement is this?

7. For the circuit shown in figure 7, $V_1 = 10\sin(200t)$ and $V_2 = 15\sin(200t)$. What will be V_{out}? The OPAMP is ideal one with infinite gain. **[5M]**

8. Cascaded circuit shown in figure 8 is with emitter resistor. Find overall input resistance of the circuit, if $h_{ie} = h_{re} = h_{oe} = 0$ and h_{fe} is same for each of the transistors Q_1 to Q_N. Draw the small signal equivalent circuit. **[4M]**

9. For the circuit shown in figure 9, what will be the output? What is the name of the circuit? **[4M]**

10. Define following properly: **[4M]**

(a) Integrator circuit using OPAMP.

(b) Transistor as a switch.

11. **Answer the following questions properly.** **[8x1=8M]**

(a) Cascode transistor configuration consists of a _____ stage in series followed by a _____ stage.

(b) In an amplifier circuit the average power delivered to the load depends on the phase angle. (**True/ False**).

(c) In a self or emitter bias circuit, the stability increases as the base resistance (R_b) **increases/ decreases/ remains constant.**

(d) An amplifier supplies output current proportional to the signal voltage and independent of Rs and R_L, is known as – **trans-resistance/ trans-conductance/ mutual conductance** amplifier.

(e) Monolithic integrated circuit is made on a **single Si crystal/ single Si atom/ single Si sheet.**

(f) The amplifier in which the operating point is chosen so that the output current or voltage is zero for more than one half of an input sinusoidal cycle is known as **class AB / class A/ class C/ Class B** amplifier.

(g) Phase shift distortion is also known as **non-linear distortion/ delay distortion/ destructive distortion.**

(h) Physical model of a transistor includes **early feedback generator/ base spreading resistance/ both.**

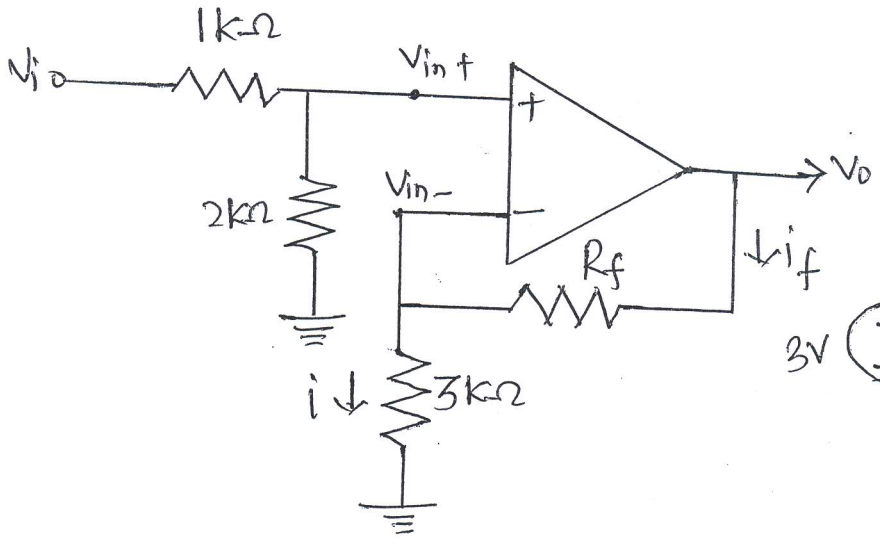

Figure 1

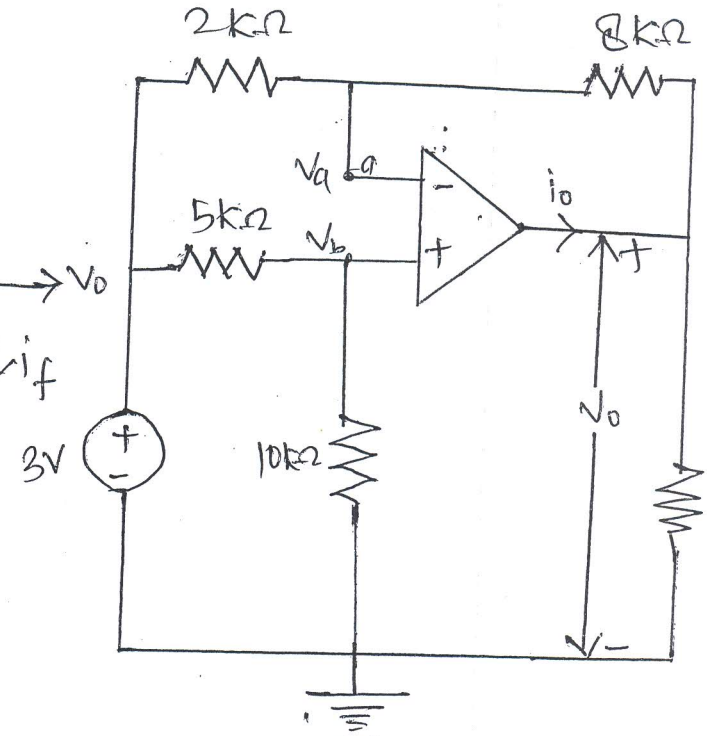

Figure 2

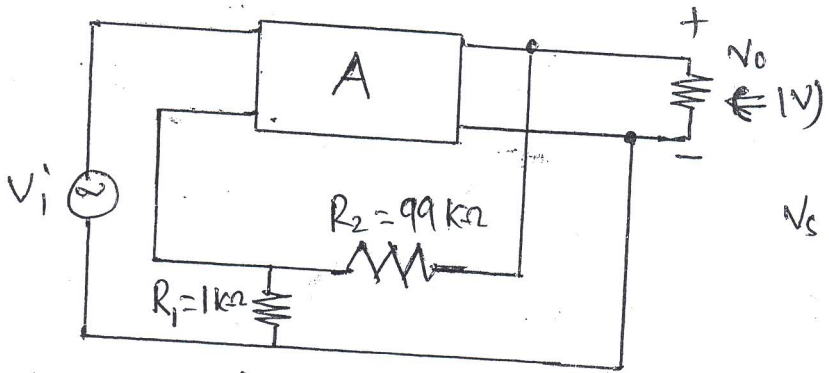

Figure 3.

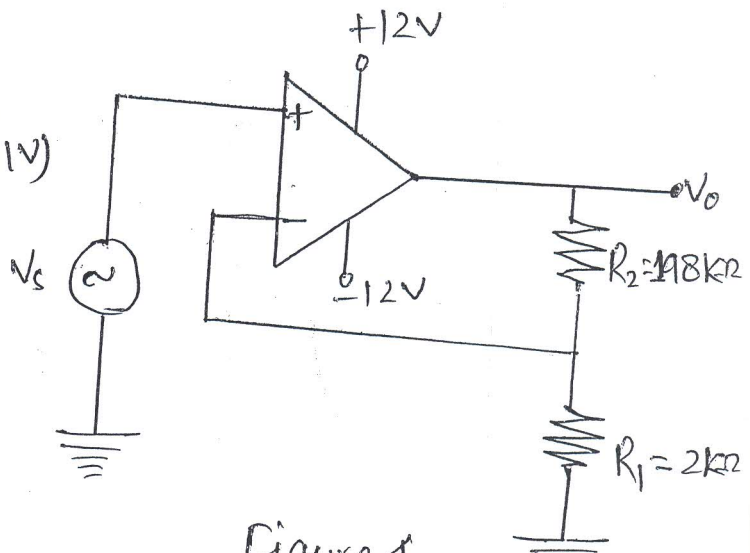

Figure 4

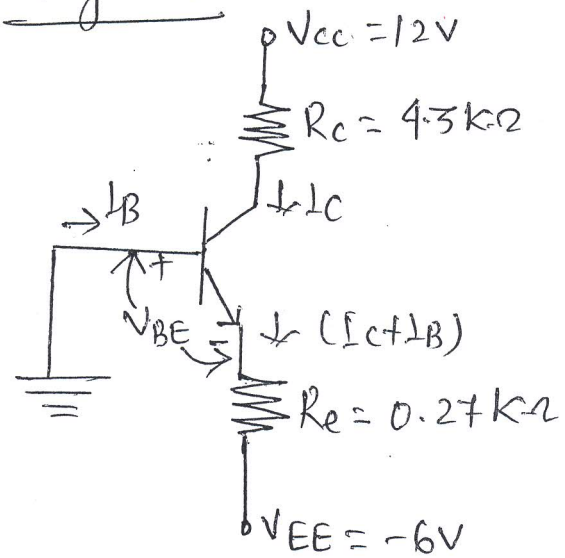

Figure 5

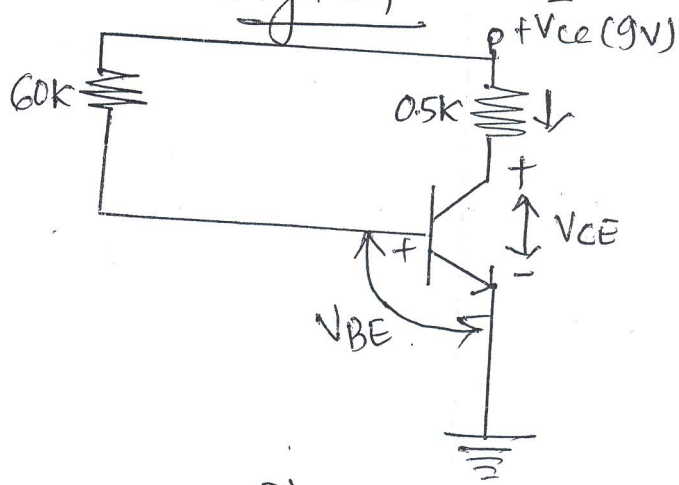

Figure 6.

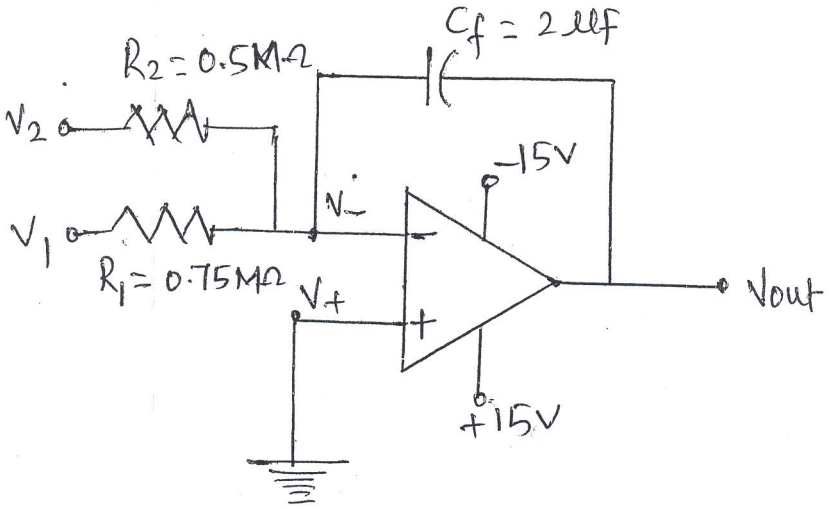

Figure 7.

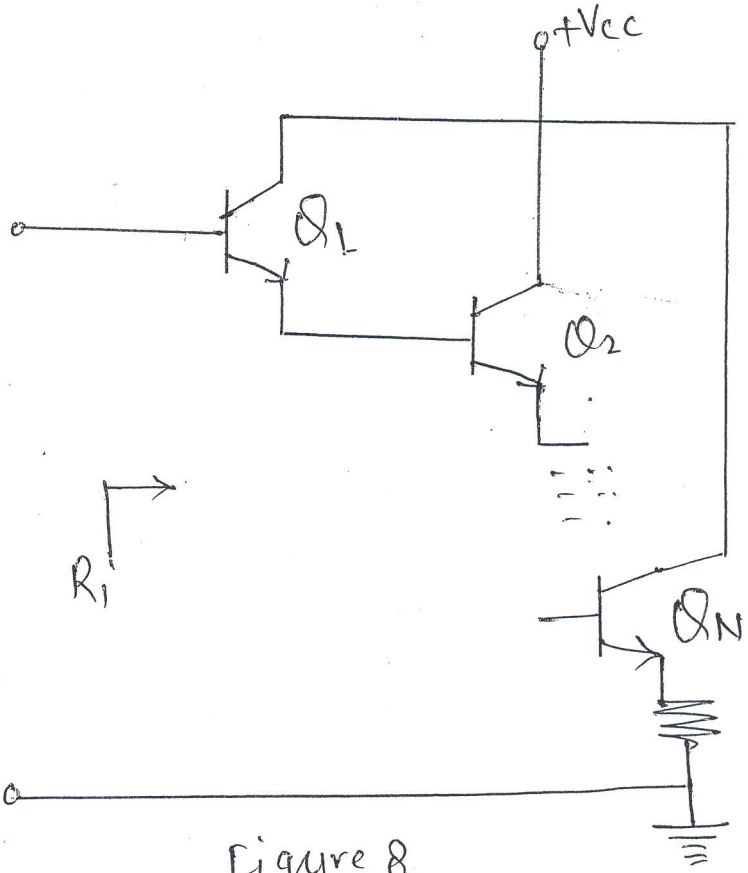

Figure 8.

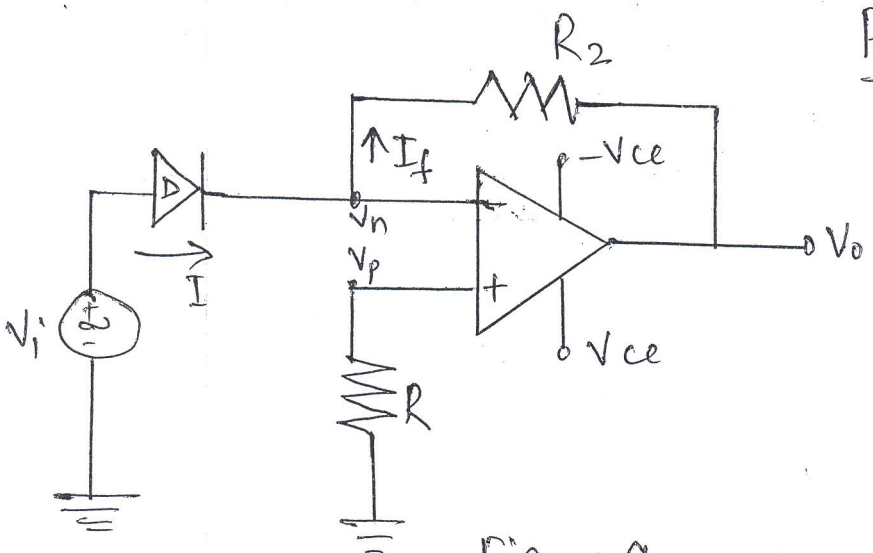

Figure 9.