Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: III**
Title of the Course	**: Digital Electronics**	**Course Code**	**: ECB 202**

Time: 3 Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

Section A

Q 1 Solve the following problems **(1×10)**

a. Convert the binary number 1011 into gray code.
b. Perform (5+4) using 2's complement representation.
c. Find the octal equivalent of $(2F.C4)_{16}$ and hex equivalent of $(762.013)_8$.
d. What is the result of addition of numbers $(-64)_{10}$ and $(80)_{16}$ in decimal number system?
e. Reduce the following Boolean expression using Boolean algebra:
$F = (A + B + \bar{C})(A + B + C)(A + \bar{B} + \bar{C})$.
f. Simplify the given function $f(A, B, C, D) = \sum(0, 1, 4, 5, 8, 9, 13, 15)$, using K-map.
g. Implement the Boolean function $(A + B)(C + D)$ using three NOR gates.
h. Draw the logic circuit of JK-FF using gates and also write its function table.
i. A clock of frequency 200MHz is being applied to cascaded stages of MOD-10 and MOD-20 counters. What will be the frequencies at the output of MOD-10 and MOD-20 counters, respectively?
j. Find the resolution of 8-bit DAC for a full-scale output voltage of 5 V.

Section B

Q 2 Given the Boolean function F in three variables R, S, and T as $F = \bar{R}S\bar{T} + R\bar{S}T + RST$

a. Express F in minimal SOP form
b. Express F in the minimal POS form
c. Assuming that both true and complement forms of the input variables are available draw a circuit to implement F using NAND gates only.

(5)

Q 3 Show how an asynchronous counter can be implemented having a modulus of 12 with a straight binary sequence from 0000 through 1011. **(5)**

Q 4 What is full adder? Obtain the expression for sum and carry output from truth table. Implement the logic circuit using two half –adders. **(5)**

Q 5 Implement $F(A, B, C) = \sum(0, 1, 3, 5, 6, 7)$ using 4×1 MUX with **(5)**

a. AB as select line
b. AC as select line

Q 6 Design a simple logic circuit such that the output is 1 when the binary number ABCD is greater than 0110. **(5)**

Section C

Q 7 The inputs A_2, A_1, A_0 and the outputs X, Y of a digital circuit are given in the following truth table **(10)**

A_2	A_1	A_0	X	Y
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	0

Design the circuit using

a. 8 to 1 multiplexers.
b. 3-bit binary decoder and logic gates.

Q 8 The truth table for AB flip-flop is shown below. Draw schematic diagram using JK flip-flop and any additional logic to implement it. Show the design steps? **(10)**

A_n	B_n	Q_{n+1}
0	0	$\overline{Q_n}$
1	0	Q_n
0	1	1
1	1	0

Q 9 Design a synchronous counter circuit using JK-FF having 7 states with the states sequence 000 to 110. Draw the state transition diagram of a synchronous counter. Use the state table for the design. **(10)**

-End of the paper-