Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch	**: CSE+EEE**	**Semester**	**: III**
Title of the Course	**: Analog Electronics**	**Course Code**	**: ECB 206**

Time: 3Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.
- Used symbols have their usual meaning
- Assumed, if any data is missing.

Section A

(2×5)

Q1. Draw the low frequency small signal model for FET which consists of a Norton's output circuit containing a dependent current generator.

Q2. Sketch the output waveform of the circuit shown in Figure-1 below. It is given that discharging time constant (CR_L) is much greater than the time period of input wave.

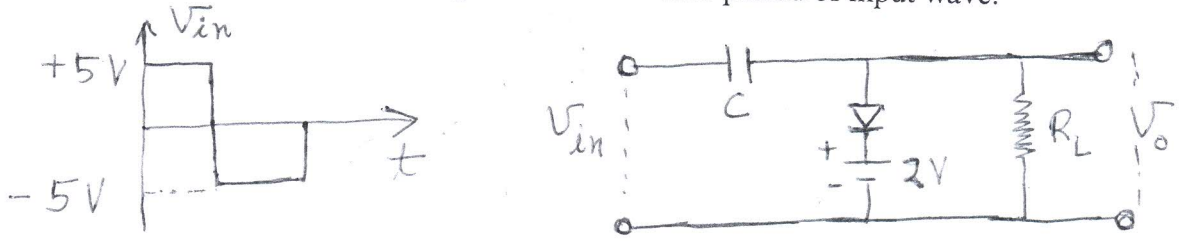


Figure – 1

Q3. Find the h-parameters of the circuit shown in Figure-2 below.

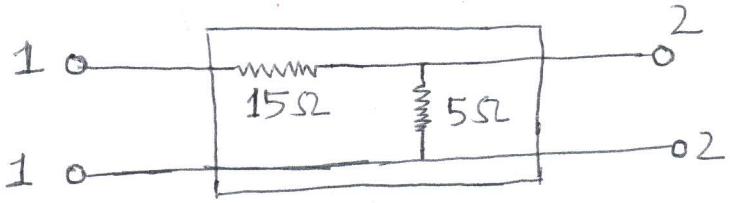


Figure – 2

Q4. Define CMRR and input offset voltage of an op-amp.

Q5. An op-amp has a slew rate of 0.5 V/μ s. If the input signal varies by 0.25 in 10 μs, find the maximum voltage gain?

Section B

Q1. For the circuit shown in Figure-3, calculate V_0, Z_i, Z_0, *and* A_v. Input$V_i = 0.2\ V_{rms}$, I_{DSS}, = $9\ mA$ and $V_p = -4.5V$. **(5)**

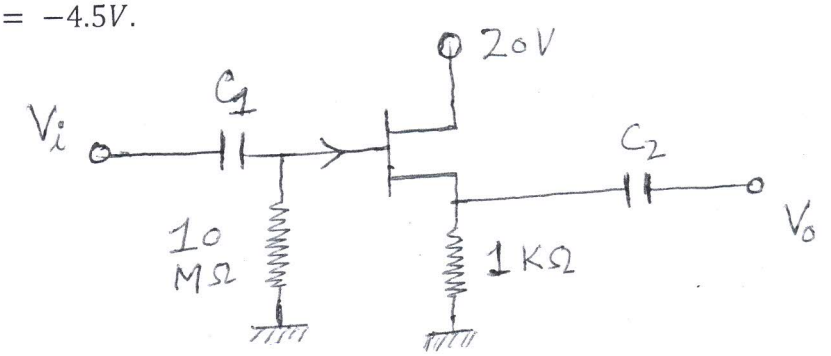


Figure-3

Q2. The amplifier shown in Figure-4 uses a transistor with following parameters: $h_{ie} = 1.1\ k\Omega, h_{fe} = 50, h_{re} = 2.5 \times 10^{-4}, and\ h_{oe} = 25 \times 10^{-6}\ A/V$. Calculate $(i)\ A_i\ and\ A_{is}$, $(ii) A_v\ and\ A_{vs}$, and $(iii) R_o', and\ R_i'$. **(5)**

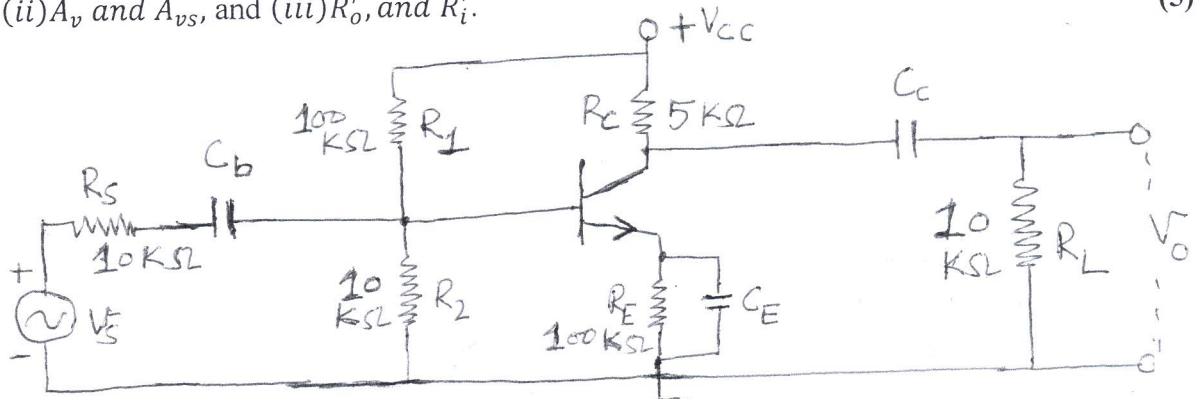
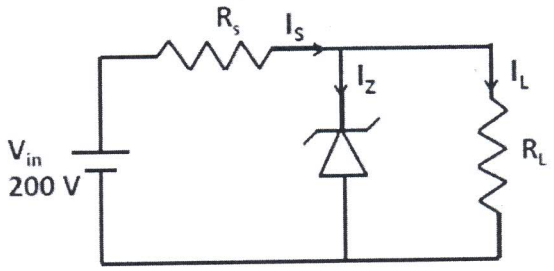


Figure-4

Q3. A 50 V, 5 to 40 mA is used as shown in the regulator circuit-

(a) Calculate R_s to allow voltage regulation from $I_L = 0$ to I_{Lmax}. Also calculate I_{Lmax} value?

(b) If R_s is set as found in part (a) and I_L is fixed at 25 mA, then what is the permissible range of V_{in}, for Zener diode to act as regulator safely? **(2.5+2.5)**



Q4. Design an op-amp circuit whose output is given as $V_0 = 3\ V_1 - 5V_2 + 4\ V_3 - 2V_4$. **(5)**

Q5. How is the voltage series feedback amplifier different from voltage shunt feedback amplifier? Find out the expression for the voltage gain of voltage series feedback amplifier using op-amp for which open loop gain in A. **(5)**

Section C

Q1. What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET? Explain the working principle along with drain characteristics and transfer characteristics curves of n-channel depletion type MOSFET.

(10)

Q2. Sketch the circuit diagram of the basic differential amplifier by using npn transistors and a constant current bias arrangement which contains compensating diodes. For this circuit determines the following parameters:

(a): Emitter current flowing in constant current source.

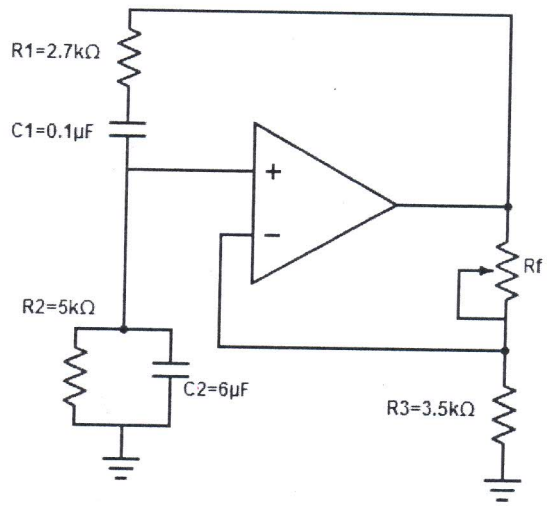
(b): AC-voltage gain in common-mode operation using r_e model for transistor.

(10)

Q3.

(a) Draw the block diagram of an operational amplifier. Briefly explain the working of each block. **(5)**

(b) Determine the values of $\mathbf{f_o}$, $\boldsymbol{\beta}$ and $\mathbf{R_f}$ for the Wein Bridge Oscillator given below. **(5)**



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