Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech, End (Spring)Semester: 2017-2018

Branch	**: ECE**	**Semester**	**: IV**
Title of the Course	**:Analog Electronics**	**Course Code**	**: ECB 252**

Time: 3 Hours **Maximum Marks: 50**

Note:

- **Questions are printed on BOTH sides. Answers should be CLEAR and TO THE POINT.**
- **All parts of a single question must be answered together and in the same sequence as given in question paper. ELSE QUESTION SHALL NOT BE EVALUATED.**

Q1. Consider the cascaded circuit in **figure 1 (a)** with emitter resistor. Find the input resistance of a single stage and then find the overall input resistance of the entire circuit if $h_{ie} = h_{re} = h_{oe} = 0$ and h_{fe} is same for each of the transistor Q_1 to Q_N. **[1+1]**

The small signal equivalent circuit model of each of such transistor is given in **figure 1 (b).**

Q2. **Answer the following questions properly.** **[8x1=8]**

(a) Cascode transistor configuration consists of a _____ stage in series followed by a _____ stage.

(b) In an amplifier circuit the average power delivered to the load depends on the phase angle. (**True/ False**).

(c) In a self or emitter bias circuit, the stability increases as the base resistance (R_b) **increases/ decreases/ remains constant.**

(d) An amplifier supplies output current proportional to the signal voltage and independent of Rs and R_L, is known as - **trans-resistance/ trans-conductance/ mutual conductance** amplifier.

(e) Monolithic integrated circuit is made on a **single Si crystal/ single Si atom/ single Si sheet.**

(f) The amplifier in which the operating point is chosen so that the output current or voltage is zero for more than one half of an input sinusoidal cycle is known as **class AB / class A/ class C/ Class B** amplifier.

(g) Phase shift distortion is also known as **non-linear distortion/ delay distortion/ destructive distortion.**

(h) Physical model of a transistor includes **early feedback generator/ base spreading resistance/ both.**

Q3. Find out the input impedance ($Z_{in}=V_{in}/I_{in}$) of the circuit in **figure 2.** **[2]**

Q4. Design an inverter amplifier (also draw the circuit diagram) with gain of 120 and input impedance of 5 kΩ. **[3]**

Q5. For the summing amplifier shown in **figure 3**, estimate the values of resistors R_1, R_2 and R_3 so that the output V_o is $V_o=-(3V_1+V_2+0.2V_3)$
What is the approximate value of the compensating resistor R? **[3]**

Q6. Determine the output voltage in the circuit shown in **figure 4**, if $V_a=5V$, $V_b=-2V$ and $V_c=3V$. **[3]**

Q7. Calculate the approximate value for the base resistor R_B, in the circuit as shown in **figure 5**, which will forward bias the emitter junction of silicon transistor ($\beta=100$) in the circuit. Collector-emitter voltage V_{CE} of 2.5 V reverse biases the collector. ($V_{BE}=0.7V$). **[4]**

Q8. The operating point values of current $I_C(=I_{CQ})$ and voltage $V_{CE}(=V_{CEQ})$ in the circuit, as shown in **figure 6**, have magnitudes of 0.9 mA and 3.72 V respectively when the current gain β for the transistor is 100. The transistor in the circuit is replaced by another one with $\beta=200$. Calculate the new values of I_{CQ} and V_{CEQ}. What do you infer? **[4]**

Q9. Design a fixed bias circuit using a silicon transistor having β value of 100, $V_{cc} = 10\ V$ and DC bias condition are to be $V_{CE} = 5V$ and $I_C = 5mA$. **[3]**

Q10. Determine whether the transistor is biased in cutoff, saturation or linear region, as shown in the **figure 7.** **[5]**

a) $R_B = 330\ \Omega\ , R_E = 3k\Omega, R_C = 1.6k\Omega$
b) $R_B = 150\ \Omega\ , R_E = 1k\Omega, R_C = 1.6k\Omega$
c) $R_B = 150\ \Omega\ , R_E = 500\Omega, R_C = 4k\Omega$

Q11. Determine $I_C, V_{CE}, I_{C(sat)}$ *and* $V_{CE(cut\ off)}$, in the figure shown in **figure 8**, Also, construct DC load line and plot q-point. Assume $\beta_{DC} = 220$ *and* $I_E = I_C$. **[3]**

Q12. For the circuit as shown in **figure 9**, $V_1 = 10\sin(200t)$*and* $V_2 = 15\sin(200t)$. What is V_{out}? The op amp is ideal with infinite gain. **[5]**

Q13. Evaluate the following amplifier circuit, shown in **figure 10**, to determine the value of resistor R_4 in order to obtain a voltage gain (v_o/v_i) of -120. **[5]**

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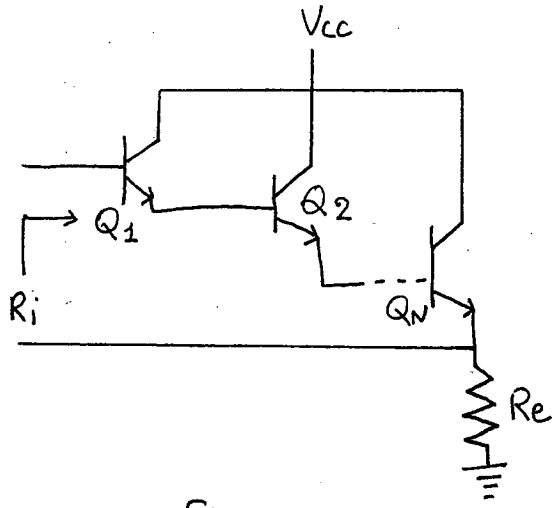

Figure 1(a)

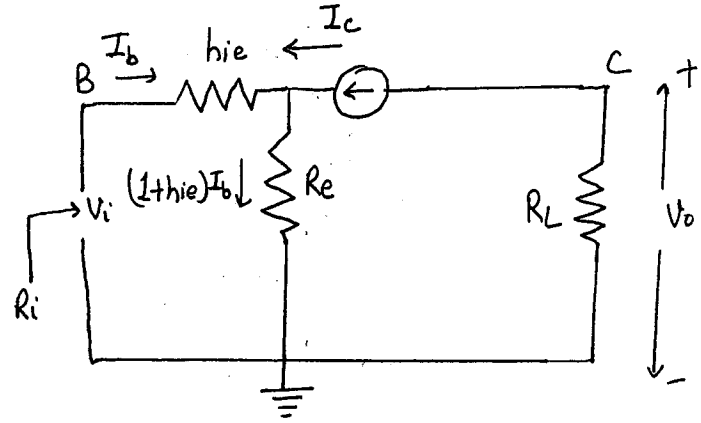

Figure 1(b)

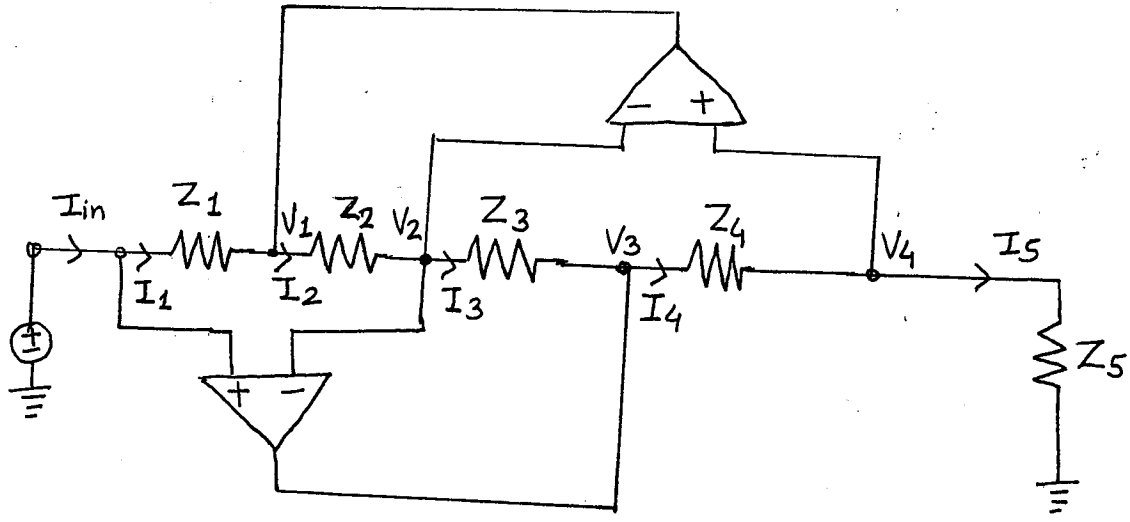

Figure 2

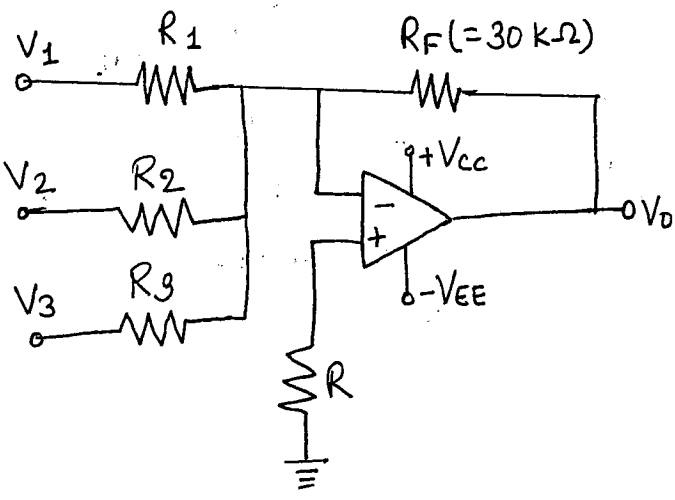

Figure 3

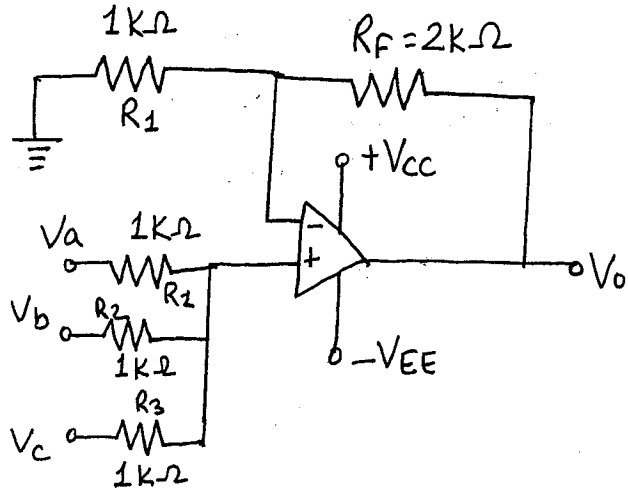

Figure 4

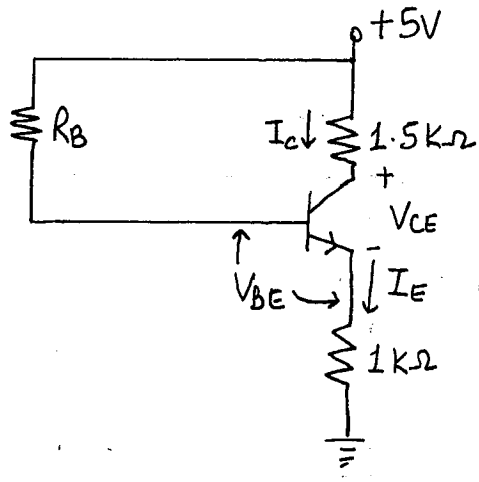

Figure 5

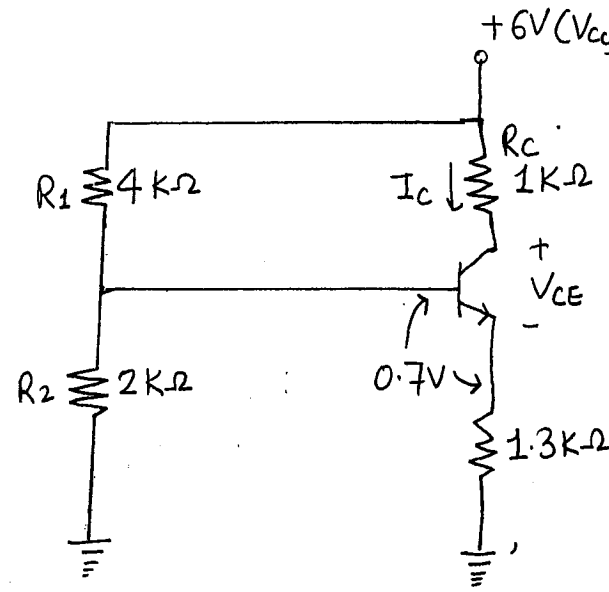

Figure 6

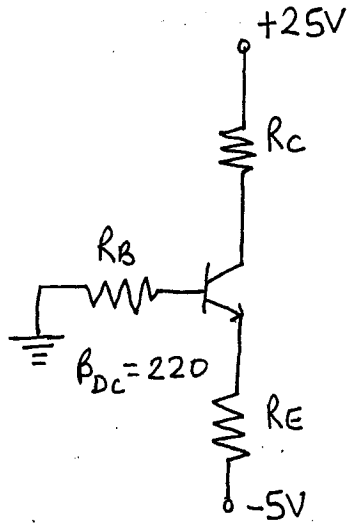

Figure 7

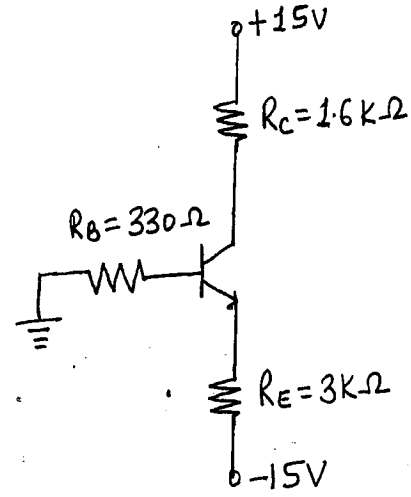

Figure 8

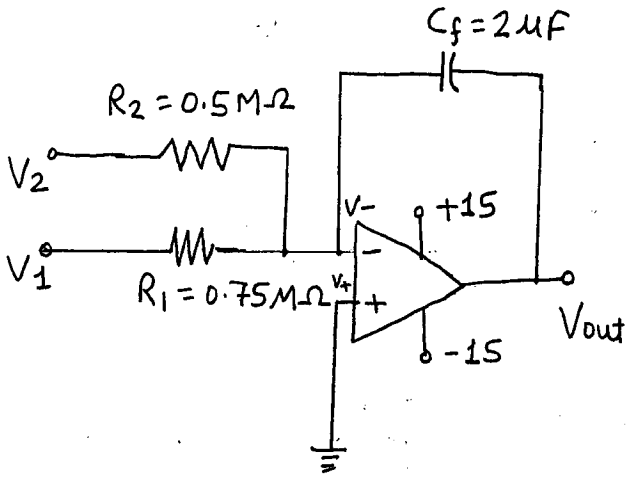

Figure 9

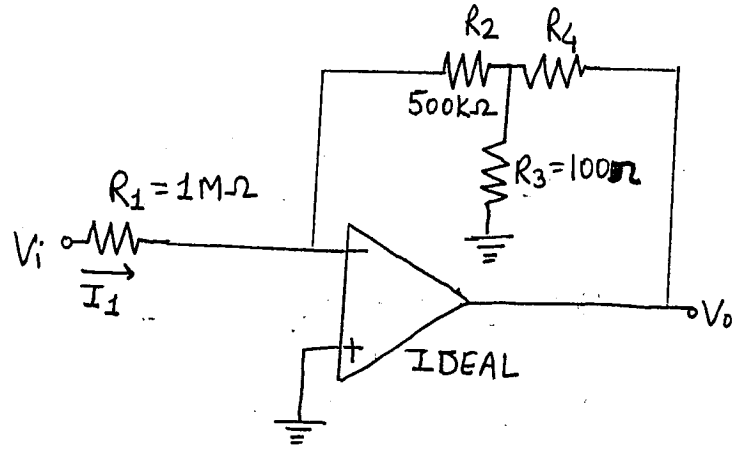

Figure 10