Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	: CSE & EEE	Semester	: III
Title of the Course	: Analog Electronics	Course Code	: ECB 206
Time: 2 Hours		Maximum Marks: 25	

Note:

- **Answers should be CLEAR, TO THE POINT AND LEGIBLE.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**
- **Assume if any data is missing.**
- **All Questions are compulsory.**

Q1. What do you understand by depletion layer across the P-N Junction? Explain and draw the load line and Q point selection for CE configuration of NPN transistor.

(5)

Q2. Draw the transfer characteristics ($^{v_o}/_{v_i}$) for the circuit shown in **Figure-1** below. Assume ideal diodes. Also assume that v_i varies from 0-50V. Indicate all slopes and voltage levels. Also indicate for each region which diodes are conducting. (5)

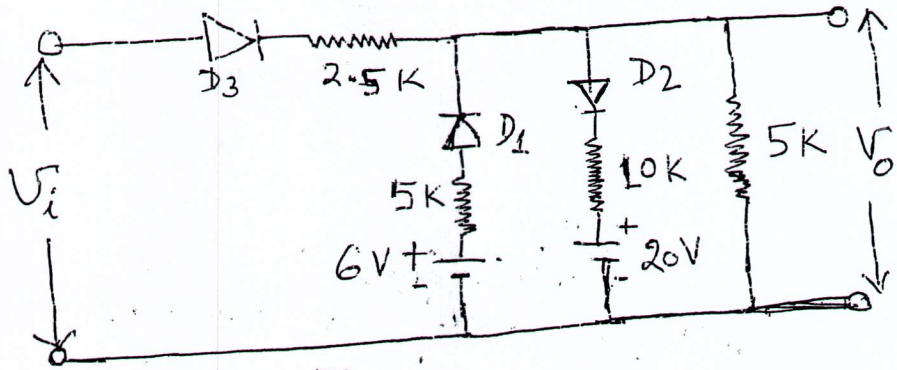

Figure-1

Q3. Define transfer utilization factor (TUF) and Ripple factor of a rectifier circuit. For a rectifier circuit shown in **Figure-2**, find (i) d.c. load current, (ii) power loss in all diodes and (iii) power conversion efficiency. Assume that the peak current rating of the diode is 2A and average current rating is 0.3A and diode drop is 1volt. (5)

P.T.O

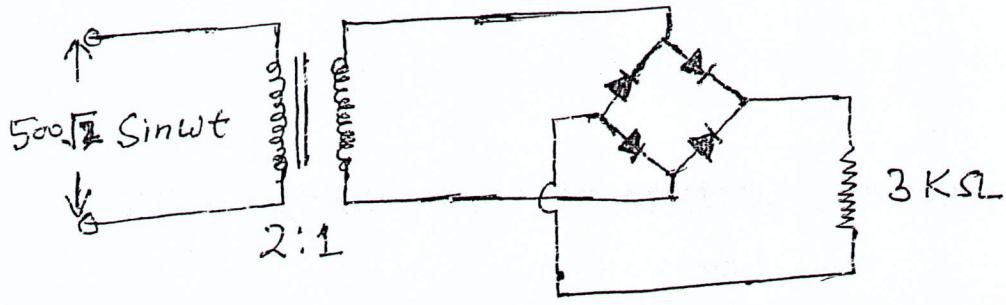

Figure – 2

Q4. Discuss the factor responsible for the shifting of operating points. A common emitter amplifier with self bias arrangement is shown in **Figure-3**. This employs an NPN transistor having $\beta = 99$. If this circuit is required to have a stability factor 5, calculate the values of R_1, R_2 *and* R_E if the values of resistance R_L and various voltages are as shown in Figure. **(5)**

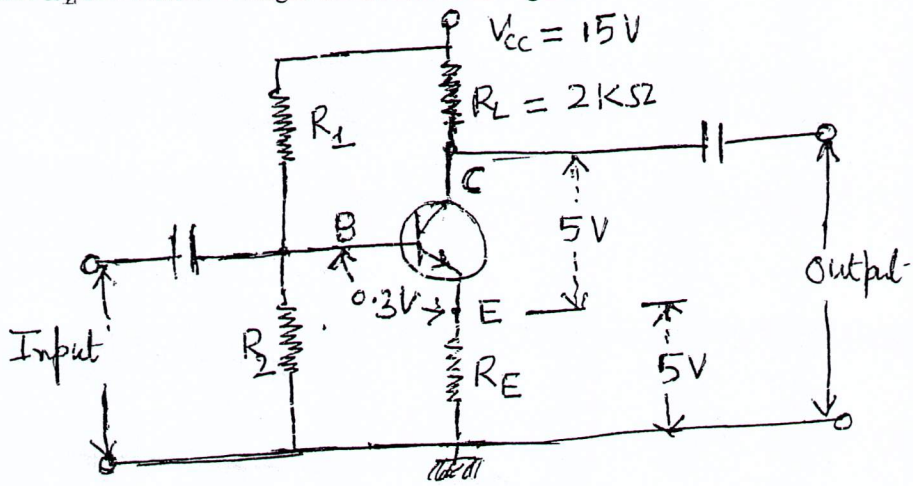

Figure – 3

Q5. **(a)** For the Zener diode network of **Figure-4**, determine V_L, V_R, I_Z and P_Z.

(b) Repeat part (a) with R_L =3K ohm. **(5)**

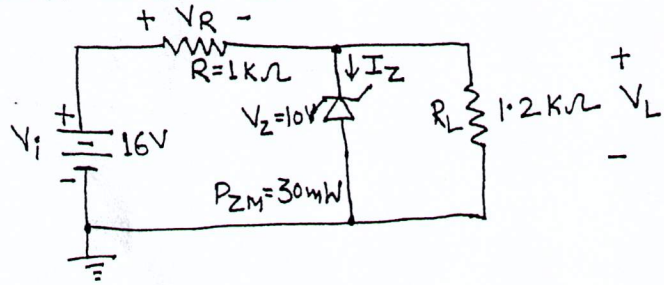

Figure – 4

********** END OF THE QUESTION PAPER **********