Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B.Tech.

Branch	**: ECE**	**Semester**	**: VI**
Title of the Course	**: Microprocessor Systems**	**Course Code**	**: EC 353**
Time	**: 3 Hours**	**Maximum Marks: 50**	

Note:

- **Questions are printed on BOTH sides. Answers should be CLEAR, TO THE POINT AND LEGIBLE.**
- **All parts of a single question must be answered together and in the same sequence as given in question paper. ELSE QUESTION SHALL NOT BE EVALUATED.**

SECTION-A

Q. 1. Find the address in the Interrupt Vector Table (IVT) at which the higher byte of the instruction pointer is stored for the interrupt INT 61H of 8086. (1)

Q.2. In a Fully Nested Mode, the interrupt IR4 is given the highest priority (taken as priority 0). Then what will be the priority for IR_0? (1)

Q.3 Form the effective(i.e. Physical) addresses for Based Indexed addressing mode for MOV AX, [BX] [SI] and Relative Based Indexed addressing mode for MOV AX, 5000 [BX],[SI]
The contents of different registers are given below:
Offset (displacement) = 5000H, [AX] = 1000H, [BX] = 2000H, [DS] =1000H, [SI] = 3000H (1)

Q.4. Compute the delay which the LOOP 2 will insert. The numbers in the brackets are T-states for the instructions. For the LOOP 2, ignore the 3 T-states for the last JUMP instruction as the reduction in time delay will be insignificant. The frequency of the system is 2MHz. (2)

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        MVI B, 38H (7)
LOOP2:  MVI C, FFH (7)
LOOP1:  DCR C (4)
        JNZ LOOP1 (10/7)
        DCR B (4)
        JNZ LOOP2 (10/7)
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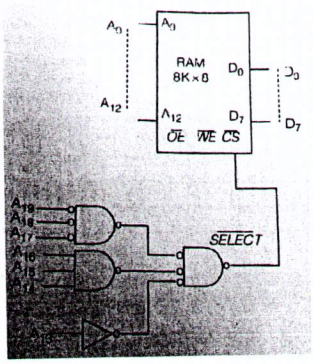
Q.5. What is the address range of addresses when the memory chip is connected to 8086? (1)



Q.6. Find the result and the state of the flags CF, ZF and OF when the following instructions are executed
AX = 008CH, BX = 345EH, CX = 67EB H (2)
a) AND BL, CL b) OR AH, BH

Q.7. Configure the control word for counter 0 in modes 3, counts in BCD, and specify that a 16 bit count is written with LSB first for an 8253/8254? (1)

Q.8. Name the different machine cycles of 8085. (1)

SECTION-B

Q.9. Discuss the the major difference between 8085 and 8086 microprocessor. (4)

Q.10. Discuss the Execution Unit (EU) and the Bus Interface Unit (BIU) of 8086 preferably through a block diagram. What main features they hold? (4)

Q.11. What is the significance of INT1 i.e. Single stepping interrupt? Write an ALP to set the Trap flag. (4)

Q.12. How the memory is organized as odd and even bank in 8086? Explain with an example. (4)

Q.13. How memory segmentation is a good technique to access memory in context of x86 family of microprocessor. Give at least three points. (4)

SECTION-C

Q.14. (a) Explain the Mode 0: Interrupt on terminal count of 8253. If in between, the GATE pin goes low, what will happen? Give a practical application of this mode.
(b) The counter 0 is used in mode 1 to generate a delay of 10 msec. After this delay the OUT 0 pin must go high. The clock frequency used for the counter chip is 1.5 MHz. Find the COUNT. (5)

Q.15. What are the different blocks of an 8259 Programmable Interrupt Controller? Explain the function of each in brief. (5)

Q.16. List the different modes of 8255 and give their salient features. Draw a schematic showing how a stepper motor is connected to the 8086 using 8255. List each step for this interfacing. (5)

Q.17. What are the building blocks which make a generic 8051? Explain various features of 8051. How do we set the 8051 for selecting register bank 2 (5)