Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch	**: EEE and ECE.**	**Semester**	**: 1st**
Title of the Course	**: Introduction to Electrical & Electronics Engineering**	**Course Code**	**: EEB100**

Time: 2 Hours **Maximum Marks: 25**

Note : 1. This paper contains 7 questions in 2 printed pages.

2. Answer all the questions.

1. For the circuit shown in Fig.1, use nodal analysis to determine V_x and V_s. What is the power consumed by the ***6 Ω*** resistance? Also calculate the power supplied by ***240 V*** and ***60 V*** voltage sources. **[4]**

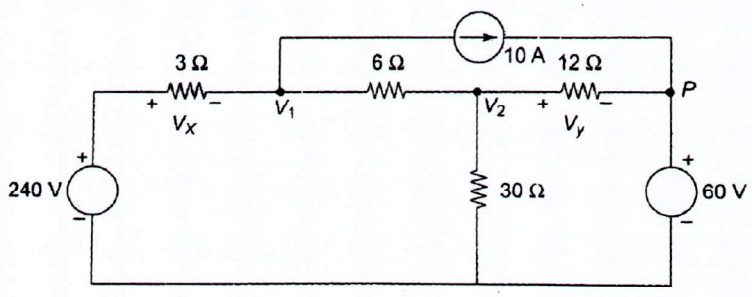


Fig. 1

2. Obtain the Thevenin's and Norton's equivalent circuit across ***x - y*** terminals shown in Fig.2. **[4]**

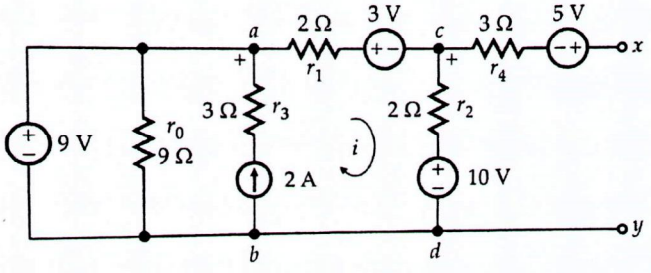


Fig. 2

3. In a series RLC circuit, the maximum inductor voltage is twice the capacitor voltage maximum. However, the circuit current lags the applied voltage by 30° and the instantaneous drop across the inductance is given by $v_L = 100 \sin 377t\ V$. Assuming the resistance being $20\ \Omega$, find the values of the inductance and capacitance. **[4]**

4. a) Subtract 14 from 46 using 8-bit 2's complement arithmetic.
   b) Convert $(5497)_{10}$ to radix 8 number system.
   c) Convert $(A0F9.0EB)_{16}$ to decimal number system.
   d) Convert $(756.603)_8$ to hexadecimal number system.
   e) Construct a truth table for the expression $f = \bar{x}y + yz + xz$
   f) Express the following Boolean function in a standard POS form.

   $$f = AB + \bar{A}C$$ **[1*6]**

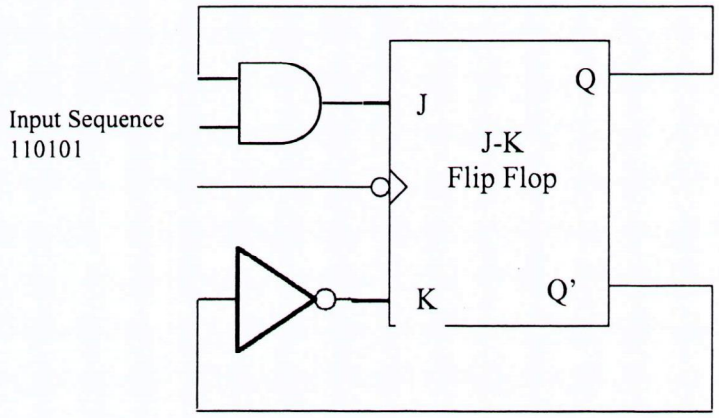
5. Design the following function using basic logic gates and also reduce the function using Boolean algebra rules and then redesign the reduced function using NAND gates only.

   $$f = A\left[B + \bar{C}\left(\overline{AB + A\bar{C}}\right)\right]$$ **[2]**

6. Simplify the following expression and design it using 2-input NAND gates only.

   $$f = A\bar{B} + ABD + AB\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{A}B\bar{C}$$ **[2]**

7. Draw the input (J and K) and output (Q and Q') waveform of the J-K flip shown in fig. 3 for the 6 consecutive clock pulses. Assume that the one of the input of the AND gate follows a sequence 110101 at negative edge of clock pulse. Initially flip flop is in reset state i.e. Q=0 and Q'=1.



[3]

Fig. 3