Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch:	**EEE**	**Semester:**	**4th**
Course Title:	**Digital Electronics and Logic Design**	**Course Code:**	**CSB 254**
Time:	**3 Hours**	**Max. Marks:**	**50**

Note: Do not write anything on the question paper except Roll number

Section A: Answer all 10 multiple choice questions. Each question carries 01 mark. [10×1=10]

A1. Convert gray code $(1010111)_G$ to binary.

A2. A PLA consists of

(a) AND matrix (b) OR matrix (c) invert/non-invert matrix (d) all of the above

A3. A 4-bit PIPO shift register will receive 4 bits of _____ data for each clock pulse.

A4. The code used for labeling cells of the K-map is:

(a) BCD (b) Hexadecimal (c) Gray (d) Octal

A5. Simplify the given expression using Boolean algebra: A'B+AB+A'B'

A6. Subtract $(1010)_2$ from $(1111)_2$ using 2's complement method.

A7. Generally shift register is constructed by using:

(a) T flip flops (b) D flip flops (c) JK flip flops (d) all

A8. A flip flop can be used to store:

(a) 1-bit data (b) 2-bit data (c) nibble (d) 1-byte data

A9. Draw a truth table for equation Y=AC+AB.

A10. A k-map is an abstract form of _____ organized as a matrix of squares.

(a) Venn Diagram (b) Cycle Diagram (c) Block Diagram (d) Triangular Diagram

Section B: Answer any 4 questions. Each question carries 5 marks. [4×5=20]

B1. Implement function $F(A,B,C)=\sum(1,3,5,6)$ using a 4:1 MUX.

B2. Design a 2-bit magnitude comparator using basic logic gates.

P.T.O

B3. Design a 4-bit parallel adder/ subtractor and explain the working of same with the help of an example.

B4. Design Mod-6 asynchronous counter using T flip flops.

B5. Design a 4-bit shift register which takes serial input and transfer the parallel data to output.

Section C: Answer any 2 questions. Each question carries 10 marks. **[2×10=20]**

C1. Design a MOD-10 synchronous counter using J-K flip flop.

C2. Using the K-map method, simplify the following Boolean function and obtain

(i) Minimal SOP and (ii) minimal POS expressions :

$Y=\sum m(0,2,3,6,7) +\sum d(8,10,11,15)$

C3. Design a 4-bit even parity checker circuit.