Roll No : .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech.

Branch : ECE

Semester : IV

Title of the Course : Digital Electronics

Course Code : ECB 202

Time: 3 Hours

Maximum Marks: 50

Section A

Note: Attempt ALL Questions. Each question carries equal marks. **(10 × 1= 10 Marks)**

1. A flip-flop can store
   a) one bit of data
   b) two bit of data
   c) three bits of data
   d) Any number of bits of data

2. The characteristic of J-K flip-flop is similar to
   a) S-R flip-flop
   b) D flip-flop
   c) T flip-flop
   d) None of the Mentioned

3. The Race around condition occurs in a J-K flip-flop when
   a) both the inputs are 0
   b) both the inputs are 1
   c) the inputs are complementary
   d) Anyone of the above input combinations is present

4. How many flip-flops are required to construct a decade counter?
   a) 4
   b) 8
   c) 5
   d) 10

5. The full form of PLD is
   a) Programmable Load Devices
   b) Programmable Logic Data
   c) Programmable Logic Devices
   d) Programmable Loaded Devices

6. PLA contains
   a) AND and OR arrays
   b) NAND and OR arrays
   c) NOT and AND arrays
   d) NOR and OR arrays

7. A ROM of size M*N bits can store
   1) N words of M bits each
   2) M words of N bits each
   3) M bits
   4) N bits

8. The decimal equivalent of the highest possible address for an 8-bit address bus is
   a) 8
   b) 128
   c) 255
   d) 256

9. A sequential circuit does not use clock pulses. It is
   a) an asynchronous sequential circuit
   b) a synchronous sequential circuit
   c) a Counter
   d) a shift register

10. The output frequency of a mod-12 counter is 6 kHz. Its input frequency is
    a) 6 kHz
    b) 500 Hz
    c) 24 kHz
    d) 72 kHz

Section B

Note: Attempt Any FOUR Questions. Each question carries equal marks. **(4 × 5 = 20 Marks)**

11. Show that (A+B) $\overline{AB}$ is equivalent to A ex-or B. Also construct the corresponding logic diagram.

12. Implement a full adder using 2-input NAND logic.

13. Design a BCD to Gray code converter and construct the corresponding logic diagram.

14. Design a combinational circuit using a PROM. The circuit accepts a 3-bit binary number and generates its equivalent excess-3 code.

15. Convert SR-Flip flop to JK-flip flop.

Section C

Note: Attempt Any TWO Questions. Each question carries equal marks. **(2 × 10 = 20 Marks)**

17. Design a synchronous Mod-6 counter using JK Flip flop.

18. Design a 4-bit parallel in, serial out shift register.

20. Design a 32:1 Mux using two 16:1 Muxs and one 2:1 mux modules.