Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: EEE**	**Semester**	**: IV**
Title of the Course	**: Digital Electronics and Logic Design**	**Course Code**	**: CSB 254**

Time: 3 Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

Section A

Q 1 Solve the following problems **(1×10)**

a. Convert the decimal number 11.35 into equivalent octal number.
b. Find 15's and 16's complement of hexadecimal number $(ABCD)_{16}$.
c. Show that NOR gate is a universal gate.
d. A clock of frequency 120MHz is being applied to cascaded stages of MOD-4 and MOD-3 counters. What will be the frequencies at the output of MOD-4 and MOD-3 counters, respectively?
e. Verify the following Boolean expression using Boolean algebra: $AB + AC + B\bar{C} = AC + B\bar{C}$.
f. Simplify the given function $f(A, B, C, D) = \sum(3, 4, 5, 7, 9, 13, 14, 15)$, using K-map.
g. An equality detector gives the output $y = 1$, if both the inputs A and B are either 1 or 0. Construct the truth table and obtain the Boolean expression for y.
h. Implement the XOR function using NOR gate.
i. Find all the prime implicants for the Boolean function $F(w, x, y, z) = \sum(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$, and determine which are essential?
j. In a 4-bit Johnson ring counter, if propagation delay of each flip-flop is 10 ns, then calculate the maximum frequency that can be applied to the counter.

Section B

Q 2 Reduce the expression and implement the same using OAI implementation **(5)**

$$F(A, B, C, D) = \prod(2, 8, 9, 10, 11, 12, 14)$$

Q 3 Write the count sequence of a 4-bit binary up counter. Design a synchronous series carry counter using flip-flop for this sequence. Also, draw the waveforms of outputs with clock signal. **(5)**

Q 4 Implement $F(A, B, C) = \sum(0, 2, 4, 6, 7)$ using two stage 2×1 MUX. **(5)**

Q 5 Draw the circuit diagram of 4-bit Ring counter using JK-FF. Explain its working with suitable timing diagrams. **(5)**

Q 6 What is full subtractor? Obtain the expression for difference and borrow output from truth table. Implement the logic circuit using two half –subtractor. **(5)**

Section C

Q 7 (a) Draw a 4-bit look ahead carry adder along with designing equations and explanations. **(5)**

(b) Implement a full adder circuit using two 4×1 multiplexers. **(5)**

Q 8 (a) What is race-around condition? Explain, how this can be eliminated? **(5)**

(b) Implement SR-FF using T-FF. **(5)**

Q 9 Explain the following programmable logic devices with suitable diagram **(10)**

a. ROM
b. PROM
c. PLA
d. PAL

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