Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: III**
Title of the Course	**: Digital Electronics**	**Course Code**	**: ECB 202**
Time: 3 Hours		**Maximum Marks: 50**	

Note: 1. Do not write anything on the question paper except Roll number.
2. Attempt the question as per the order of section as well as question number.

Section A: Answer the 10 multiple choice questions. Each question carries 01 mark. **[10×1=10]**

A1. 1 Nibble is equal to _____ bit(s)
a) 1 b) 2 c) 4 d) 8

A2. The terminal count of a modulus-11 binary counter is
1010 b. 1000 c. 1001 d. 1100

A3. A k-map is an abstract form of _____ organized as a matrix of squares.
a) Venn Diagram (b) Cycle Diagram (c) Block Diagram (d) Triangular Diagram

A4. The logic gate used in parity checkers is
a) NOR b) NAND c) X-OR d) X-NOR

A5. Which logic gate is basic comparator?
a) NOR gate (b) NAND gates (c) X-OR gate (d) X-NOR gate

A6. In an SR latch built from NOR gates, which condition is not allowed
a) S=0, R=0 b) S=0, R=1 c) S=1, R=0 d) S=1, R=1

A7. The characteristic equation of a J-K flip-flop is
a) $Q_{n+1} = J\,\overline{Q}_n + \overline{K}\,Q_n$
b) $Q_{n+1} = J\,Q_n + K\,\overline{Q}_n$
c) $Q_{n+1} = \overline{J}\,Q_n + \overline{K}\,Q_n$
d) $Q_{n+1} = \overline{J}\,\overline{Q}_n + K\,Q_n$
e)

A8. A combinational PLD with fixed OR array and programmable AND array is called a
a) PROM b) PAL c) PLA d) EPROM

A9. The decimal equivalent of the highest possible address for an 8-bit address bus is
a) 8 b) 128 c) 255 d) 127

A10. How many bits are required to store one BCD digit?
a) 1 b) 2 c) 3 d) 4

Section B: Answer any 4 questions. Each question carries 05 mark. **[4×5=20]**

B1. Write a note on following:
a) Flip flop and latches
b) Synchronous counter Vs Asynchronous counter

B2. Design a combinational circuit using a PROM, which accepts a 3-bit binary number

and generates its equivalent Excess-3 code.

B3. Convert the S-R flip-flop into J-K flip-flop and also write the excitation table and characteristic equation for J-K and S-R flip flop.

B4. Design a MOD-12 Asynchronous counter using T flip flop.

B5. Write the Boolean Algebra laws with proof(Any five).

Section C: Answer any 2 questions. Each question carries 10 mark. **[2×10=20]**

C1. Use a Multiplexer (Mux) having 3 select lines to implement the logic for the function given below. Also realize the same using a 16:1 Mux.

$$F = \sum m(0,1,2,3,4,10,11,14,15)$$

C2. Design a synchronous MOD-5 gray up counter using J-K Flip-flop (follow the step wise approach).

C3. Write a note on any two of the following with the help of circuit diagram and an example :

a) Carry look ahead adder
b) Programmable logic array
c) Universal shift register (Example: shift sequence 1010)

********** END OF THE QUESTION PAPER **********