Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	: ECE	Semester	: IV
Title of the Course	: Analog Electronics	Course Code	: ECB 252

Time: 2 Hours | Maximum Marks: 25

- **Questions are printed on BOTH sides. Answers should be CLEAR AND TO THE POINT.**
- **All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.**

1. For the circuit in figure 1, derive the expression for stability factor S, in terms of β. V_{BE} can be neglected. [3]

2. In the circuit shown in figure 2, V_{CC} = 24 V, R_c = 10K Ω, and R_e = 270 Ω. If a Si transistor is used with β = 45, and if under quiescent conditions V_{CE} = 5V, then determine (a) value of R and (b) stability factor (S). [4]

3. Determine the minimum value of current gain (β) for the transistor in figure 3, required to drive in saturation when V_{in} = +5V, $V_{BE\,(sat)}$ = 0.8 V and $V_{CE\,(sat)}$ = 0.12 V. [3]

4. A Si transistor with $V_{CE\,(sat)}$ = 0.2 V, h_{fE} = 100, $V_{BE\,(sat)}$ = 0.8 V is used in the circuit in figure 4. [3]

   (a) Find the minimum value of R_L for which the transistor is in saturation. Assume, $I_C \sim I_E$, V_{BB} = 12V and V_{CE} = 10V.
   (b) Determine the output (V_0) at saturation for $R_L = R_{L,\,min}$ for which transistor remains in saturation.

5. If the Si transistor used in the circuit in figure 5 has a minimum value of $\beta = h_{fE}$ = 30, determine whether the transistor is in cut off or active or in saturation region? V_1= +12V, V_2 = -12V, R_1 = 15K Ω, R_2 = 100 K Ω, R_c = 2.2 K Ω. Also find the output (V_0). [5]

6. For the self-bias circuit in figure 6, the Q-pt is assumed to be exactly at the middle of the dc-load line. [2]
   What will be the expression for the total combination of R_c and R_e, in terms of V_{CC} and power dissipation (P_{DQ}) at Q-pt.

7. Answer the followings only writing either True (T) or False (F) against each one. [5]

(a) In a self-bias circuit, the stability increases as the base resistance increases.

(b) For R_b = 0 and R_e not equal to 0, transistor can not be operated in active region.

(c) Rate of change of stored charge is responsible for storage time in switching.

(d) Heavily doped base in HBT, increases the base resistance.

(e) Stabilization techniques of bias stability uses thermistors.

P.T.O

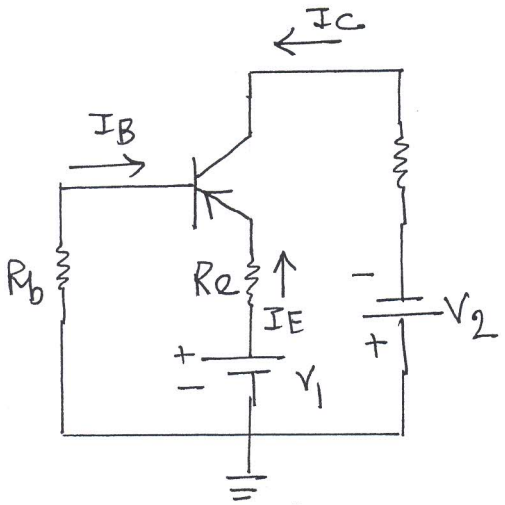

Figure 1.

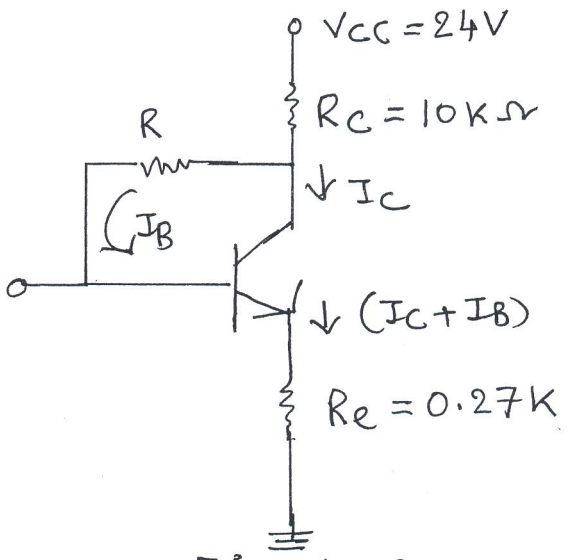

Figure 2.

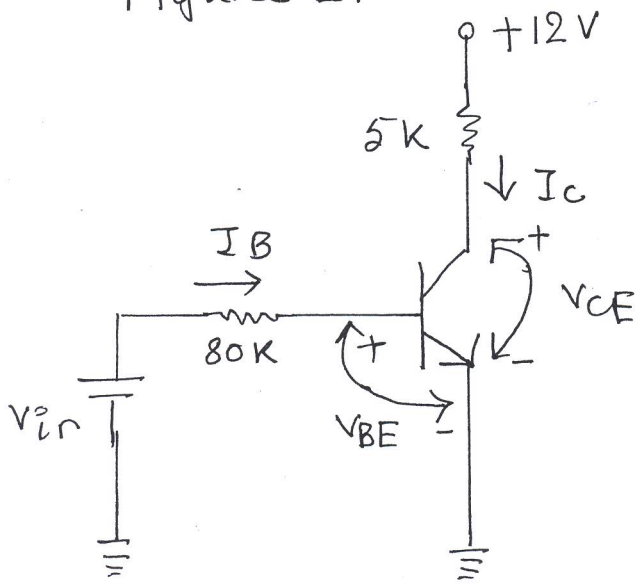

Figure 3

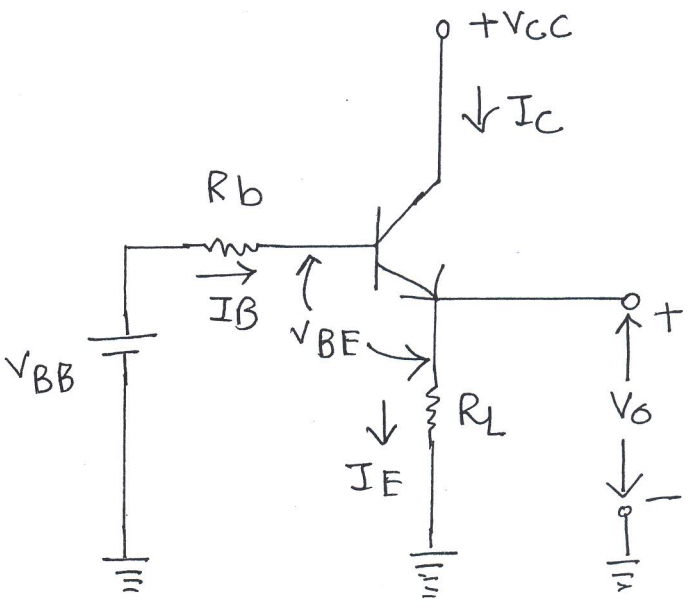

Figure 4

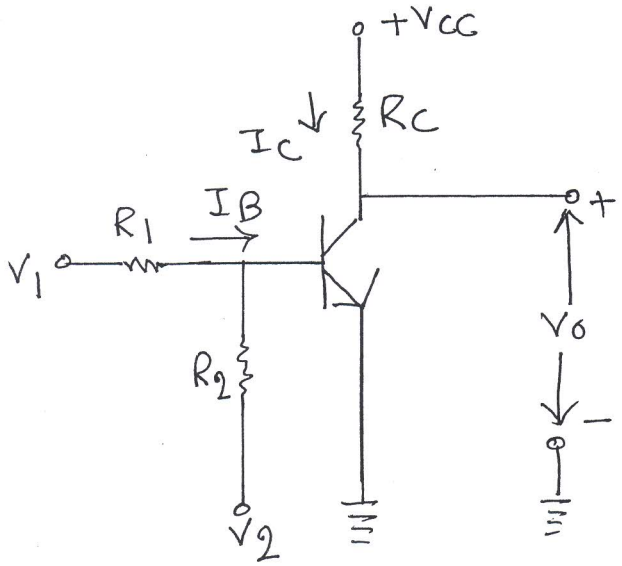

Figure5

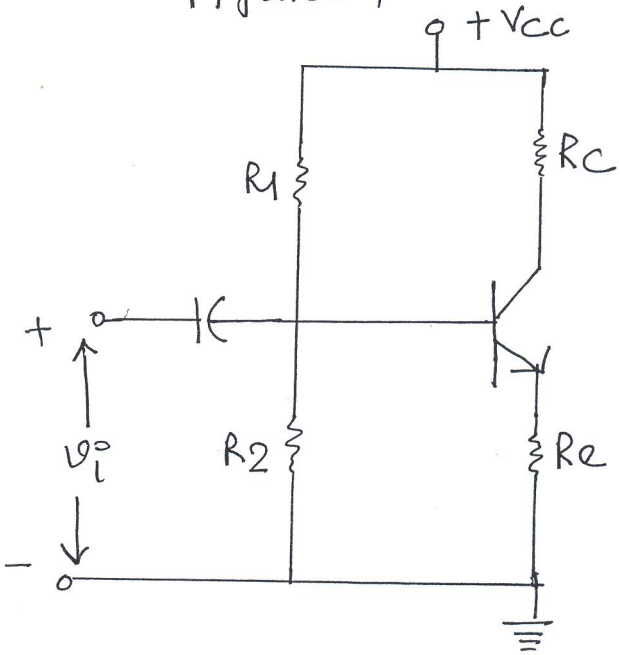

Figure 6