Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B.Tech 2nd year

Branch : ECE | Semester: 4th

Title of the Course : Architectural Design of ICs | Course Code: ECL-351

Time: 3 Hours | Maximum Marks: 50

Section-A

Note: Attempt all questions **(1×5=5)**

Q.1 What is pre layout and post layout simulation?

Q.2 Explain briefly the standard cell library?

Q.3 Explain Feedthrough cells.

Q.4 What do you understand by the term netlist?

Q.5 What is fault tolerance and DUT?

Section-B

Note: Attempt all questions **(5×6=30)**

Q.1 Differentiate the types of test procedures? Explain the terms controllability and observability.

Q.2 Explain the concept of CORDIC architecture and how the original MAC algorithm changed into iterative shift and add algorithm.

Q.3 Differentiate between hard macros and soft macros. How are they optimized for power, area and performance?

Q.4 Draw and explain the architectures of ripple carry adder and carry skip adder. How the delay optimization is achieved in carry skip adder? Draw the propagation delay (t_P) vs. number of bits (N) graph for both.

Q.5 What do you understand by the terms throughput and latency? Explain the data dependencies in pipelining and parallel processing?

Q.6 Explain how the optimization in terms of area, delay and power consumption for squaring a number is performed?

Section-C

Note: Attempt all questions **(7+8=15)**

Q.1 What is array based digital circuit implementation approach. Explain pre-diffused and pre-wired classification in detail.

Q.2 Elaborate the meaning of "Design-for-test" approaches for sequential modules. Explain scan based test technique in detail.