Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch : ECE Semester : VII

Title of the Course: VLSI Design Course Code : EC 403

Time: 2 Hours Maximum Marks: 30

Note:

Section A

Attempt all **5 × 3 = 15**

1) Draw the Layout of 2 input CMOS AND gate?
2) Explain fabrication steps for NMOS with neat diagram?
3) Derive drain current equation for saturation and linear region?

Section B

Attempt any three **5 × 3 = 15**

4) What is latch up problem? Discuss the technology with diagram to resolve latch up problem?
5) Sketch the stick diagram of given function
$\overline{(A+B+C)D}$

6) Explain working of MOSFET with its characterstics.Compare BJT with MOSFET?
7) Discuss Lamda based design rules?