Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	: EEE & CSE	**Semester**	: III
Title of the Course	: Analog Electronics	**Course Code**	: ECB 206

Time: 3 Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

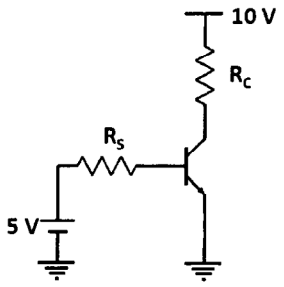
Section A

Q 1 Solve the following problems (2×5)

a. Draw the full wave center-tap rectifier circuit, input/output waveform and explain its working. Calculate PIV of the citcuit.

b. An N-channel JFET has I_{DSS} = 2 mA and V_P = -4 V. Calculate the trans-conductance (g_m) for an applied gate to source voltage V_{GS} of -2 V.

c. A silicon transistor with $V_{BE,sat}$ = 0.8 V, β = 100, $V_{CE,sat}$ = 0.2 V and R_S = 200 KΩ is used in the circuit shown below. Find the minimum value of R_C for which the transistor will remain in the saturation.



d. Define CMRR and input offset voltage of an op-amp.

e. An op-amp has a slew rate of 0.5 V/μ s. If the input signal varies by 0.25 in 10 μs, find the maximum voltage gain?

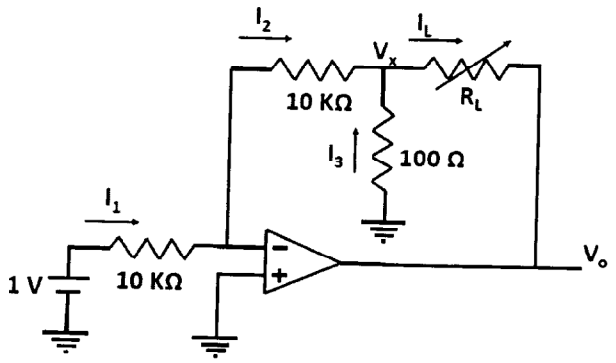
Section B

Q 2 Consider an ideal op-amp in the circuit below (5)

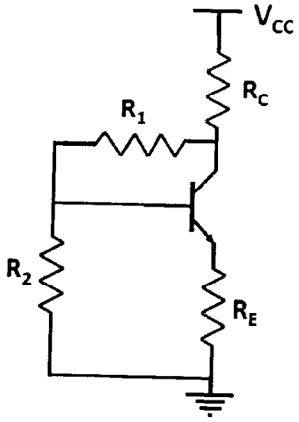
(a) Find I_1, I_2, I_4 and V_x.

(b) If V_o is not to be lower than -13 V, find maximum allowed value for R_L.

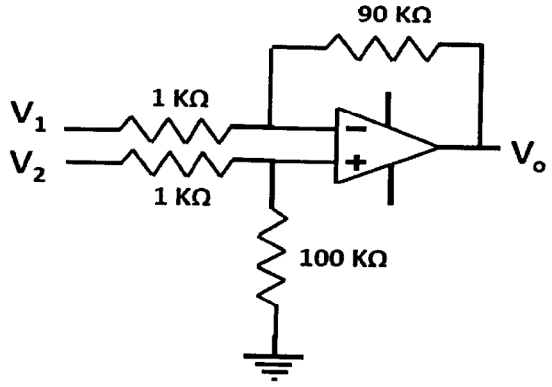
(c) If R_L is varied in the range 100 Ω to 1 KΩ, what is the corresponding change in I_L and V_o?



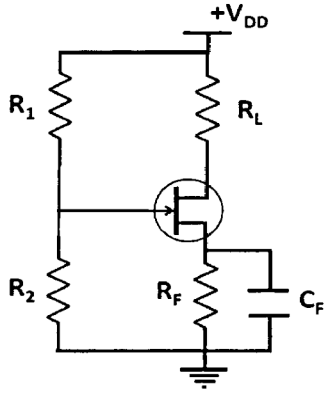
Q 3 (a) Determine the stability factor $S(I_{co})$ for the circuit shown below. **(2.5)**



(b) Find CMRR of the opamp circuit shown below. **(2.5)**



Q 4 Define the pinch-off voltage of the JFET. A JFET amplifier with stabilized biasing circuit shown below has following parameters: $V_P = -2\,V$, $I_{DSS} = 5\,mA$. $R_L = 910\,\Omega$, $R_F = 2.29\,k\Omega$, $R_1 = 12\,M\Omega$, $R_2 = 8.57\,M\Omega$ and $V_{DD} = 24$ V. Determine the value of drain current I_D at the operating point. Also verify that FET will operate in pinch-off region. 50 V, 5 to 40 mA is used as shown in the regulator circuit- **(5)**

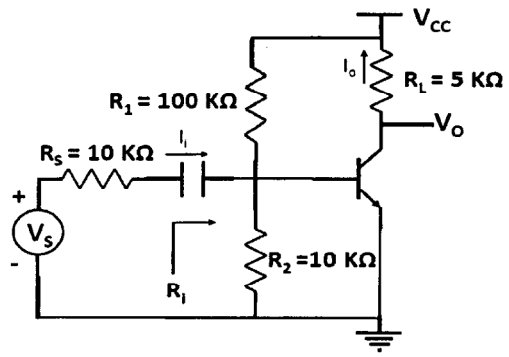


Q 5 Design an op-amp circuit whose output is given as $V_0 = 3\,V_1 - 5V_2 + 4\,V_3 - 2V_4$. **(5)**

Q 6 How is the voltage series feedback amplifier different from voltage shunt feedback amplifier? Find out the expressions of the input impedance in both cases. **(5)**

Section C

Q 7 For the circuit shown below, calculate $A_I = I_o/I_i$, A_V, A_{Vs}, and R_i. Assume suitable *h*-parameters. **(10)**



Q 8 Draw the schematic diagram of Depletion mode MOSFET. Explain its working principle along with drain characteristics and transfer characteristics curves. **(10)**

Q 9 Analyze the following characteristics of the basic differential amplifier (sketch the circuit diagram) in which a constant current bias with compensating diodes are used:

(a): Emitter current flowing in constant current source.

(b): AC-voltage gain in common-mode operation. **(10)**

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