Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: VII**
Title of the Course	**: VLSI Design**	**Course Code**	**: EC 403**

Time: 3 Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

Section A

Q 1 Answer the following questions **(2×5)**

a. What is Moore's law of integration?
b. Compare the properties of metal gate and poly-Si gate in MOS fabrication?
c. What is light field and dark field photomask?
d. Why Si is the popular material for IC fabrication compared to other semiconductor materials?
e. How CVD is different from PVD?

Section B

Q 2 What are the different techniques for crystal growth? Explain the popular technique for Si crystal growth in detail with suitable diagram. **(5)**

Q 3 Explain the sputter deposition technique for metals with suitable diagram. **(5)**

Q 4 Discuss the diffusion doping technique in detail. Compare the doping profile obtained for diffusion and ion implantation technique. **(5)**

Q 5 Determine the pull up to pull down ratio ($Z_{p.u}/Z_{p.d}$) for an NMOS inverter directly driven by another NMOS inverter. **(5)**

Q 6 Make the comparison between MOS and BJT in view of IC fabrication. **(5)**

Section C

Q 7 Discuss the metal gate process of NMOS fabrication. Explain the demerits of metal gate process. **(10)**

Q 8 What we mean by epitaxial layer? Explain the necessities of epitaxial layer growth. Neatly draw the MBE setup and explain it in detail. **(10)**

Q 9 Sketch the stick diagram for a CMOS gate computing $y = \overline{(A + B + C).D}$ and estimate the cell width and height. **(10)**

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