Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	: ECE	Semester	: IV
Title of the Course	: Analog Electronics	Course Code	: ECB 252
Time: 2 Hours		Maximum Marks: 25	

- Questions are printed on BOTH sides. Answers should be CLEAR AND TO THE POINT.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.

1. A silicon (Si) transistor with $V_{CE}(sat) = 0.2V$, $h_{fe} = 100$, $V_{BE}(sat) = 0.8V$ is used in the following circuit in Fig. 1. [2+2 = 4]

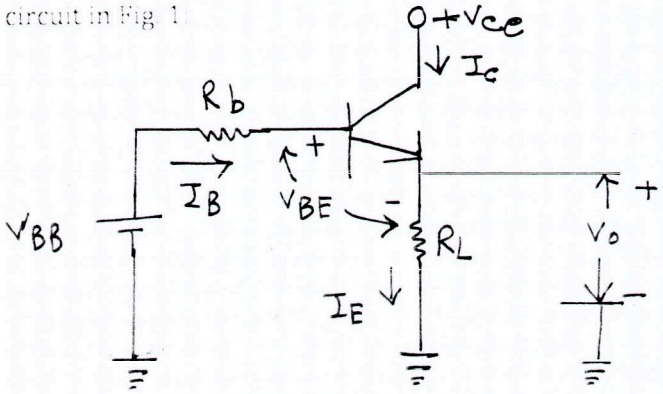


Fig ①.

(a) Find the minimum value of R_L for which the transistor is in saturation. Assume $I_C \approx I_E$, $V_{BB} = 12V$ and $V_{CE} = 10V$.

(b) Determine the output, V_0 at saturation for $R_L = R_{L,min}$, for which the transistor remains in saturation.

2. In CE mode of transistor operation, the DC current gain is defined as, $\beta_{dc} = \frac{I_C}{I_B} \equiv h_{fE}$, [4]

small signal forward current gain is defined as, $\beta_{ac} = \beta' \equiv \frac{\delta I_C}{\delta I_B}\Big|_{V_{CE}} = h_{fe}$.

The above two are related as, $\beta' = \beta + (I_{CBO} + I_B)\cdot\frac{\delta\beta}{\delta I_B}$, where, symbols have their usual meanings. At the condition $I_B \gg I_{CBO}$, show that,

$$\frac{h_{fe} - h_{fE}}{h_{fe}} \approx \frac{I_C}{h_{fE}} \cdot \frac{\delta h_{fE}}{\delta I_c}$$

3. Consider the following transistor switching circuit (Fig. 2) [2+2 = 4]

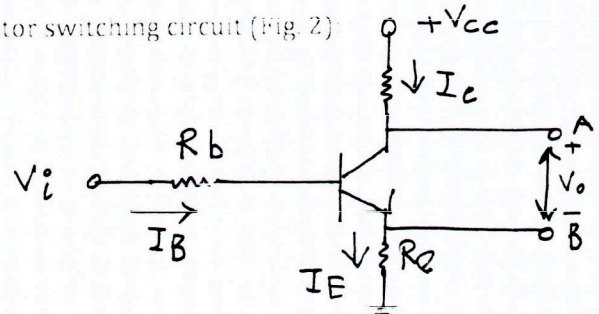


Fig. ②

(a) Let the input varies between the two voltage levels as, $V_i = V_{low} \leq 0$ and

$V_i = V_{high} \geq V_{min}$, then what will be the expression for the minimum voltage required for the transistor to be operated in saturation, under non-ideal situation?

(b) If suppose now, $V_i \geq V_{BE(sat)}$ and R_e=0 in the above circuit and we receive $R_b \approx 10\ R_c$, then at what region transistor will operate? What will be the output of the corresponding voltage levels of input for, $V_i = V_{low} < 0$ and $V_i = V_{high} \geq V_{min}$?

4. For the two-battery transistor circuit, as shown in Fig. 3, prove that the stabilization factor is given by, [2]

$$S = \frac{1 + \beta}{1 + \beta \cdot R_e/(R_e + R_b)}$$

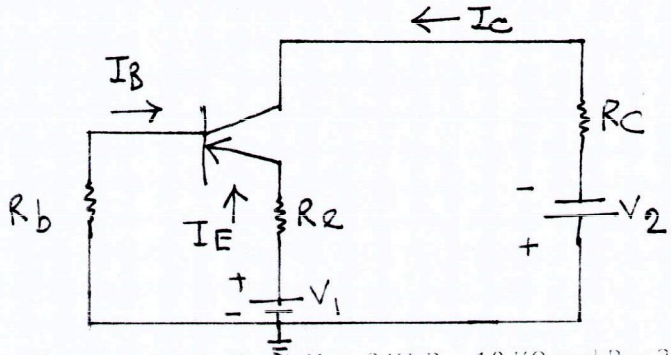
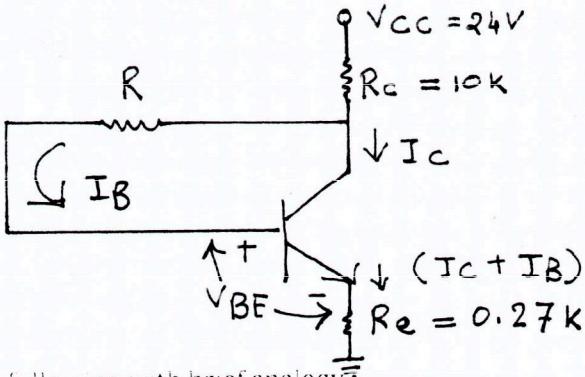


Fig ③

5. In the circuit shown in Fig. 4, V_{CC}= 24V, R_C= 10 KΩ and R_E= 270 Ω. If a Si transistor is used with β =45 and at quiescent condition, V_{CE}= 5V, determine (a) value of R (b) stability factor. [2 + 2 = 4]



Fig④

6. Comment on the following with brief analogy: [2]
"Fixed bias circuit provides higher gain but less stability than collector feedback bias circuit".

7. Write true (T)/false (F) against each of the following statements: [1 x 5 = 5]

(a) For R_b=0 and $R_e \neq 0$, transistor cannot be operated in active region.
(b) Compound can be made up of two alloy semiconductors
(c) Rate of change of stored charge is responsible for storage time in switching.
(d) Heavily doped base in HBT increases the base resistance.
(e) Stabilization techniques of bias stability use thermistors.