Roll No.: .....

National Institute of Technology, Delhi

Name of the Examination: B. Tech

Branch	**: ECE**	**Semester**	**: III**
Title of the Course	**: Digital Electronics**	**Course Code**	**: ECB 202**

Time: 3 Hours **Maximum Marks: 50**

Note:

- Answers should be CLEAR, TO THE POINT AND LEGIBLE.
- All parts of a single question must be answered together. ELSE QUESTION SHALL NOT BE EVALUATED.
- All questions in Section A are compulsory. Attempt any 4 questions from Section B and 2 questions from Section C.

Section A

Q 1 Solve the following problems **(1×10)**

a. Convert the decimal 1.375 number into equivalent binary number.
b. Find 15's and 16's complement of hexadecimal number $(2789)_{16}$.
c. Show that NAND gate is a universal gate.
d. What is the result of addition of numbers $(-64)_{10}$ and $(80)_{16}$ in decimal number system?
e. Verify the following Boolean expression using Boolean algebra: $AB + AC + B\bar{C} = AC + B\bar{C}$.
f. Simplify the given function $f(A, B, C, D) = \sum(0, 1, 4, 5, 8, 9, 13, 15)$, using K-map.
g. An equality detector gives the output $y = 1$, if both the inputs A and B are either 1 or 0. Construct the truth table and obtain the Boolean expression for y.
h. Implement the XOR function using NAND gate.
i. Find all the prime implicants for the Boolean function $F(w, x, y, z) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$, and determine which are essential?
j. In a 4-bit ripple counter, if propagation delay of each flip-flop is 10 ns, then calculate the maximum frequency that can be applied to the ripple counter.

Section B

Q 2 Reduce the expression and implement the same using NOR gate **(5)**

$$F(A, B, C, D) = \prod(2, 8, 9, 10, 11, 12, 14)$$

Q 3 Write the count sequence of a 3-bit binary down counter. Design a ripple counter using flip-flop for this sequence. Also, draw the waveforms of outputs with clock signal.**(5)**

Q 4 Implement $F(A, B, C) = \sum(0, 2, 4, 6, 7)$ using 4×1 MUX with **(5)**

a. BC as select line
b. AC as select line

Q 5 Design a four bit combinational circuit 2's complementer (The output generates the 2's complement of the input binary number). Implement the logic circuit using exclusive-OR gates. **(5)**

Q 6 Draw the circuit of 3-bit R-2R ladder network for digital to analog conversion. Derive the expression for output voltage in terms of circuit elements and binary inputs. **(5)**

Section C

Q 7 (a) What is priority encoder? Design a 4-bit priority encoder and implement using gates. **(5)**

(b) Implement a full adder circuit using two 4×1 multiplexers. **(5)**

Q 8 (a) What is race-around condition? Explain, how this can be eliminated? **(5)**

(b) Implement JK-FF using D-FF. **(5)**

Q 9 Explain the following logic families with suitable circuit diagram **(10)**

a. RTL
b. TTL
c. ECL

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