Roll No.:.....

National Institute of Technology, Delhi

Name of the Examination: B. Tech. (End Sem Exam)
Dec 2022

Branch	: B.Tech (ECE)	Semester	: III
Title of the Course	: Digital Electronics	Course Code	: ECB 202

Time: 3 Hours **Maximum Marks: 50**

Note : All questions are compulsory.

Q1. Perform the BCD subtraction of two numbers **(83-21)** using **9's** complement. **[1 Marks]**

Q2. What is the difference between synchronous sequential circuit and asynchronous sequential circuit? **[1 Marks]**

Q3. Using K-map realize the following Boolean function. **[3 Marks]**
$F(A, B,C,D) = \Sigma m(1, 2, 9, 10, 11, 14, 15)$

Q4 What is multiplexer? Implement the following Boolean function using 8x1 multiplexer. **[3 Marks]**
$F(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{D} + ABC + \overline{B}CD + \overline{A}CD$

Q5. Implement the following using PLA **[4 Marks]**
$E_3 = D_3 + D_2D_0 + D_2D_1$
$E_2 = D_2\overline{D_1}\,\overline{D_0} + \overline{D_2}\,D_0 + \overline{D_2}\,D_1$
$E_1 = \overline{D_1}\,\overline{D_0} + D_1D_0$
$E_0 = \overline{D_0}$

Q6. Write short notes on the ROM. **[4 Marks]**

Q7. Design **16 x 1** multiplexer using **4 x 1** multiplexer. **[4 Marks]**

Q8. Design 4 bit BCD to excess-3 code converter. **[5 Marks]**

Q9. Minimize the following function using Quine Mc Cluskey method **[5 Marks]**
$F(A,B,C,D, E) = \Sigma m(2, 4, 8, 11, 15) + d(1, 10, 12, 13)$

Q10. Explain the working of J-K flip flop with suitable diagram. Also discuss about the race-around condition in the J-K flip-flop. **[5 Marks]**

Q11. What is shift register? Explain the working of parallel in serial out shift register with suitable diagram. **[5 Marks]**

Q12. Design a 3-bit synchronous up counter using T flip-flop. **[5 Marks]**

Q13. Construct the transition plot (next state maps for each flip-flop), transition table, state table and state diagram of the given circuit. **[5 Marks]**