Roll No:

National Institute of Technology Delhi

Mid Semester Examinations-B. Tech

Branch- CSE and EEE Year-**2016**, Semester-3rd
Course Name – Analog Electronics **Maximum Marks – 25**
Course Code - ECB-206 **Total Time: 2:00 Hours**

All questions are compulsory.
Symbols have their usual meaning.
Assume any data, if it is missing.

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Q.1-(a): How does the band theory differ from the free electron model in explaining the properties of metals? The resistivity of an intrinsic semiconductor is 4.5 Ω m at $20^o\ C$ and 2.0 Ω m at $32^o\ C$. Find the energy gap in eV unit. **(2.5)**

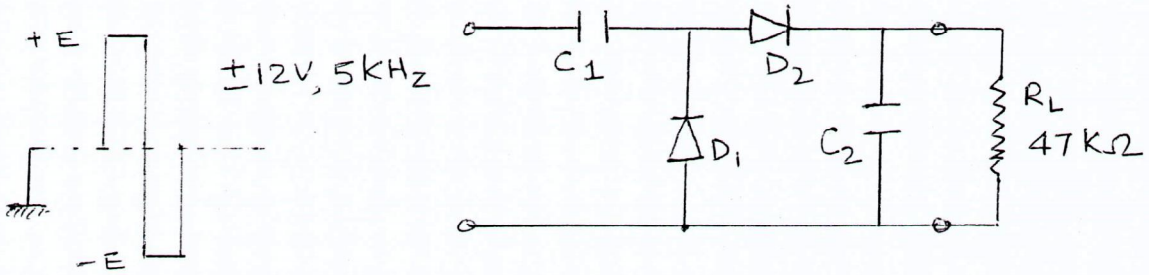
(b): Why does the effective mass of the electron differ from its free mass toward an external force in the crystal lattice? Using the concept of de-Broglie wave show that effective mass of the electron in the crystal lattice is expressed by following relation: $\boldsymbol{m^* = \frac{\hbar^2}{d^2E/dk^2}}$. **(2.5)**

Or

What do you understand by thermal runaway? Derive the condition $V_{CE} < V_{CC}/2$ to avoid thermal runaway in transistor. **(2.5+2.5)**

Q.2-(a): Consider a peak rectifier fed by a 60 Hz sinusoid having a peak $V_p = 100\ V$. Let the load resistance $R = 10\ k\ \Omega$. Find the value of the capacitance C that will result in a peak to peak ripple of 2 V. Also, calculate the fraction of the cycle during which the diode is conducting and the average and peak values of the diode current. **(3)**

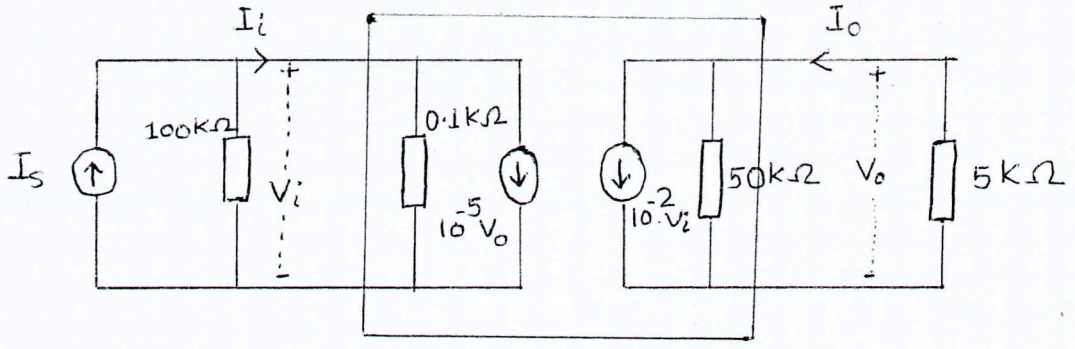
(b): Determine C_1 *and* C_2 for the voltage doubling circuit as shown below to produce a 1% maximum output ripple. The input is a $\pm$ 12 V, 5 kHz square wave. **(2)**



Or

(b): For a BJT, the CB current gain $\alpha = 0.98$ and the collector-base junction reverse saturation current is 0.6 μA. This BJT is connected in CE-mode and operated in active region with a base drive current of 20 μA. Determine the collector current. **(2)**

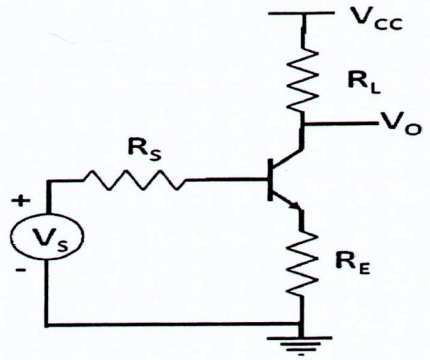
Q.3: What are the characteristics of the ideal current and trans-conductance amplifiers? For the two port network as shown below determine: $\boldsymbol{\frac{V_0}{V_i}, \frac{I_0}{I_i}, R_{in}\ and\ R_{out}}$. Further, comment that can this network be considered as an amplifier or not? **(5)**



Or

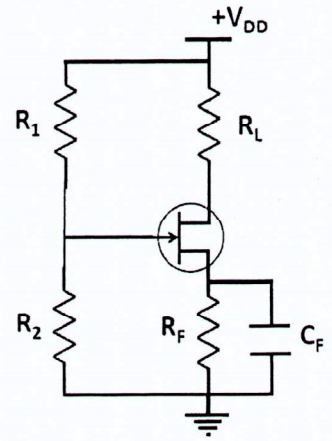
(a) In the circuit shown, find the input impedance R_i in terms of the CE h parameters, R_L and R_E.
(b) If $R_L = R_E = 1$ K and assume the suitable h parameters, what is the value of R_i?.

(3+2)



Q.4: A CE amplifier employing an NPN transistor has load resistor R_C connected between collector and V_{CC} supply of +16V. For biasing, a resistor R_1 is connected between V_{CC} supply and base, resistor $R_2 = 30k\Omega$ is connected between base and ground and a resistor $R_E = 1\ k\Omega$ is connected between emitter and ground. Draw the circuit diagram. Calculate the values of R_1 *and* R_C and the stability factor S, if $V_{BE} = 0.2\ V, I_E = 2\ mA, \alpha = 0.985$ *and* $V_{CE} = 6\ V$. **(5)**

Q.5- Define the pinch-off voltage of the JFET. A JFET amplifier with stabilized biasing circuit shown below has following parameters: $V_P = -2\ V$, $I_{DSS} = 5\ mA$. $R_L = 910\ \Omega$, $R_F = 2.29\ k\Omega$, $R_1 = 12\ M\Omega$, $R_2 = 8.57\ M\Omega$ and $V_{DD} = 24$ V. Determine the value of drain current I_D at the operating point. Also verify that FET will operate in pinch-off region. **(5)**



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