Design and Verification of Memory Model using SystemVerilog

This project describes the design and verification of a memory model using SystemVerilog. Memory refers to the hardware component that store information for temporary or permanent use. The major functions of the memory include storage and retrieving of data and maintain the state of programs and operating systems. The project outlines the process of defining the memory characteristics and implementing the core functionality.

Outcomes:

A functional memory model implemented in SystemVerilog, configurable with parameters like data width and address space.

A SystemVerilog testbench with driver, monitor, and scoreboard for comprehensive verification.

This project demonstrates the application of SystemVerilog for designing and verifying the components, ensuring their functionality and correctness before integration and implementation.