1. I have created all the components separately and the steps to see the following components are:

* Top.sv – where I have **created clock, reset, instantiated counter detection design, physical interface and the testbench program block.**
* Tx\_tb: this is my top level testbench program block where all my components will be there. For ex**: test-> top\_env-> master\_env -> Generator, BFM, Monitor, Coverage.**

1. I have taken coverage of each test and have merged all the coverage to see the total coverage. You can open the Coverage folder and check in **coverage report folder**. The report is in HTML format. For checking code coverage percentage. Check in the **dut.**
2. In our counter detection design if you see :

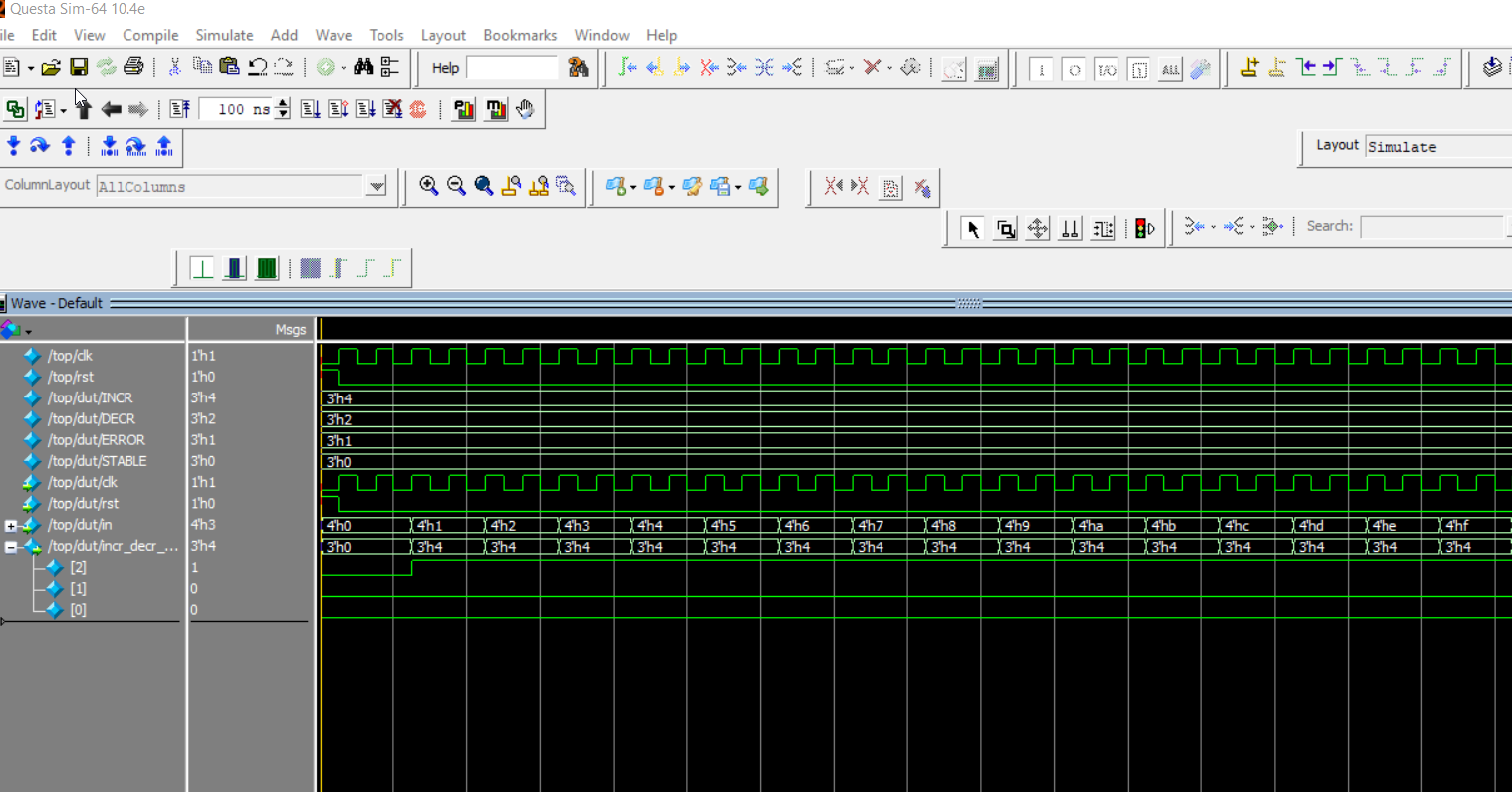
The output **(incr\_decr\_error) = 4 🡪 It means it is incrementing**

**(incr\_decr\_error) = 2 🡪 It means it is decrementing**

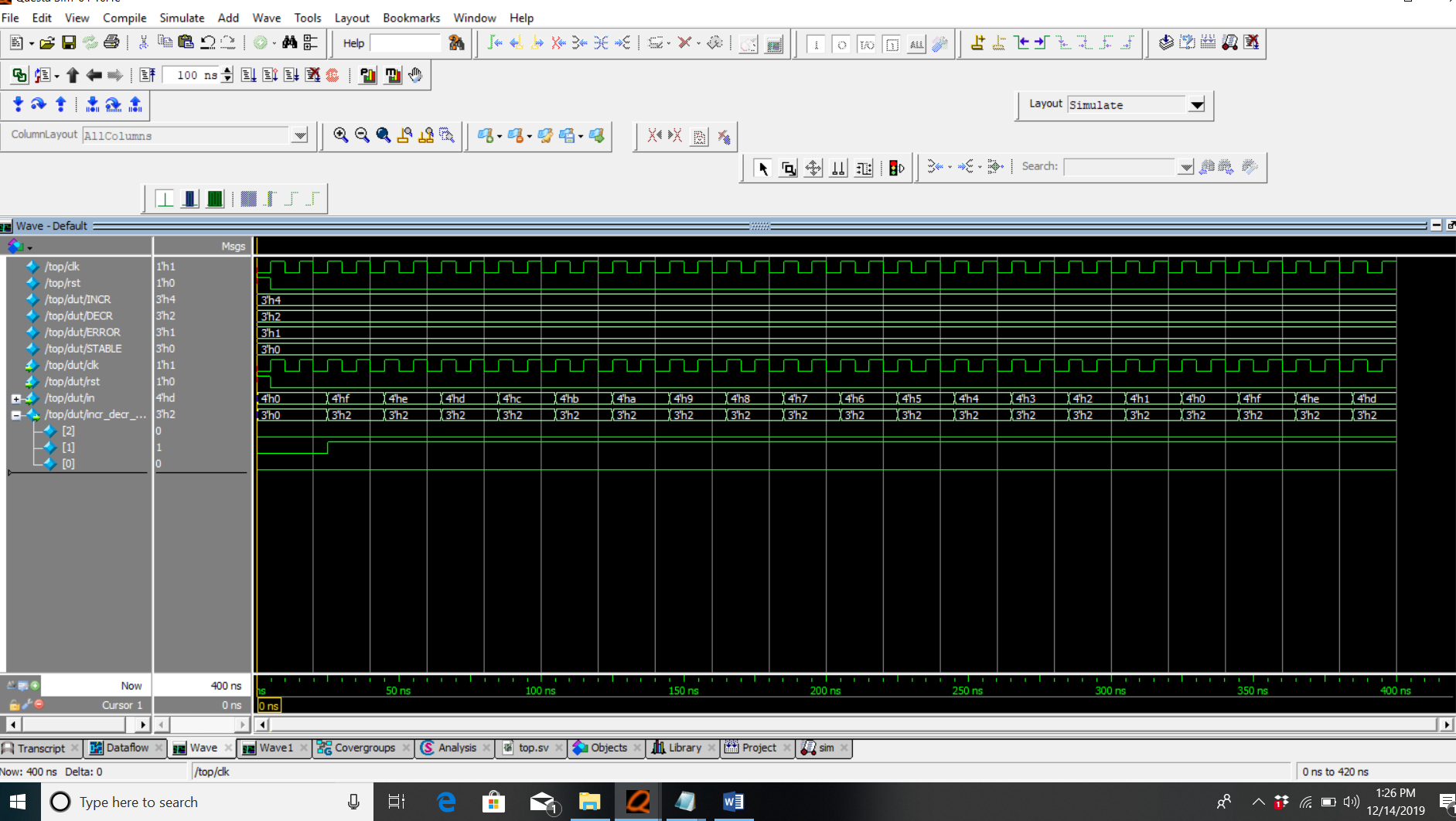
**(incr\_decr\_error) = 1 🡪 It means error**

**(incr\_decr\_error) = 0 🡪 It means it is stable**

1. INCREMENT\_WAVEFORM



1. DECREMENT\_WAVEFORM



1. ERROR\_WAVEFORM

