DIGITAL RAILWAY TIMER

Problem statement:-

Design a digital railway clock using logic gates that displays the current time in a 24-hour format (00:00 to 23:59). The clock should be synchronized with a master clock and accurately display the hours and minutes. The design should incorporate features such as seconds ticking, and the clock should handle transitions between 11:59 AM and 12:00 PM and between 11:59 PM and 12:00 AM. Minimize power consumption and prioritize simplicity and efficiency in the logic circuitry.

Introduction:-

In the realm of railway timekeeping, precision and synchronization are non-negotiable. This design task centers around crafting a digital railway clock using logic gates, adhering to a 24-hour format (00:00 to 23:59) while maintaining synchronization with a central master clock. Beyond the fundamental time display, the clock must incorporate features such as an emphasis on accuracy and simplicity. A critical aspect is handling transitions between 11:59 AM and 12:00 PM, as well as between 11:59 PM and 12:00 AM, with a seamless display switch that upholds accuracy.

The core focus of this design is on minimizing power consumption and prioritizing simplicity and efficiency in the logic circuitry. By combining advanced digital logic with the timeless tradition of railway timekeeping, the goal is to create a clock that not only meets the stringent demands of modern rail systems but also stands as a symbol of precision and efficiency in time management.

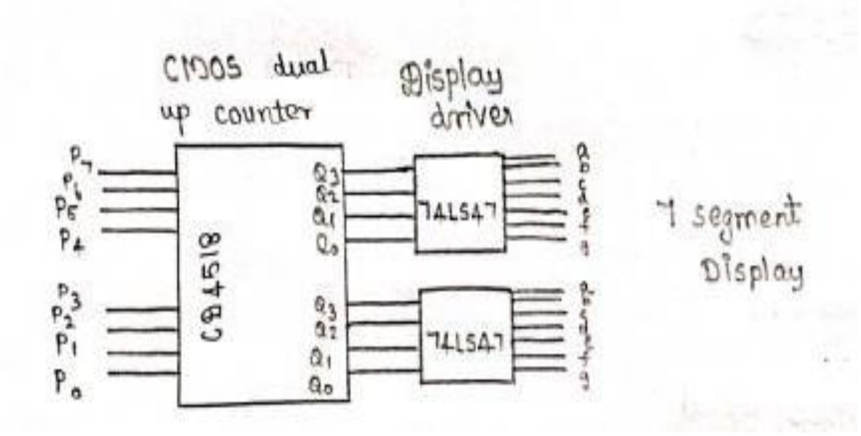
In addition to this function, the clock should exude functional elegance without displaying seconds. This design choice aligns with the straightforward nature of railway operations, where emphasis lies on accurate hour and minute displays. The digital railway clock, in its simplicity, becomes a symbol of precision and reliability, seamlessly integrating into the operational heartbeat of railway networks..

Components Required:-

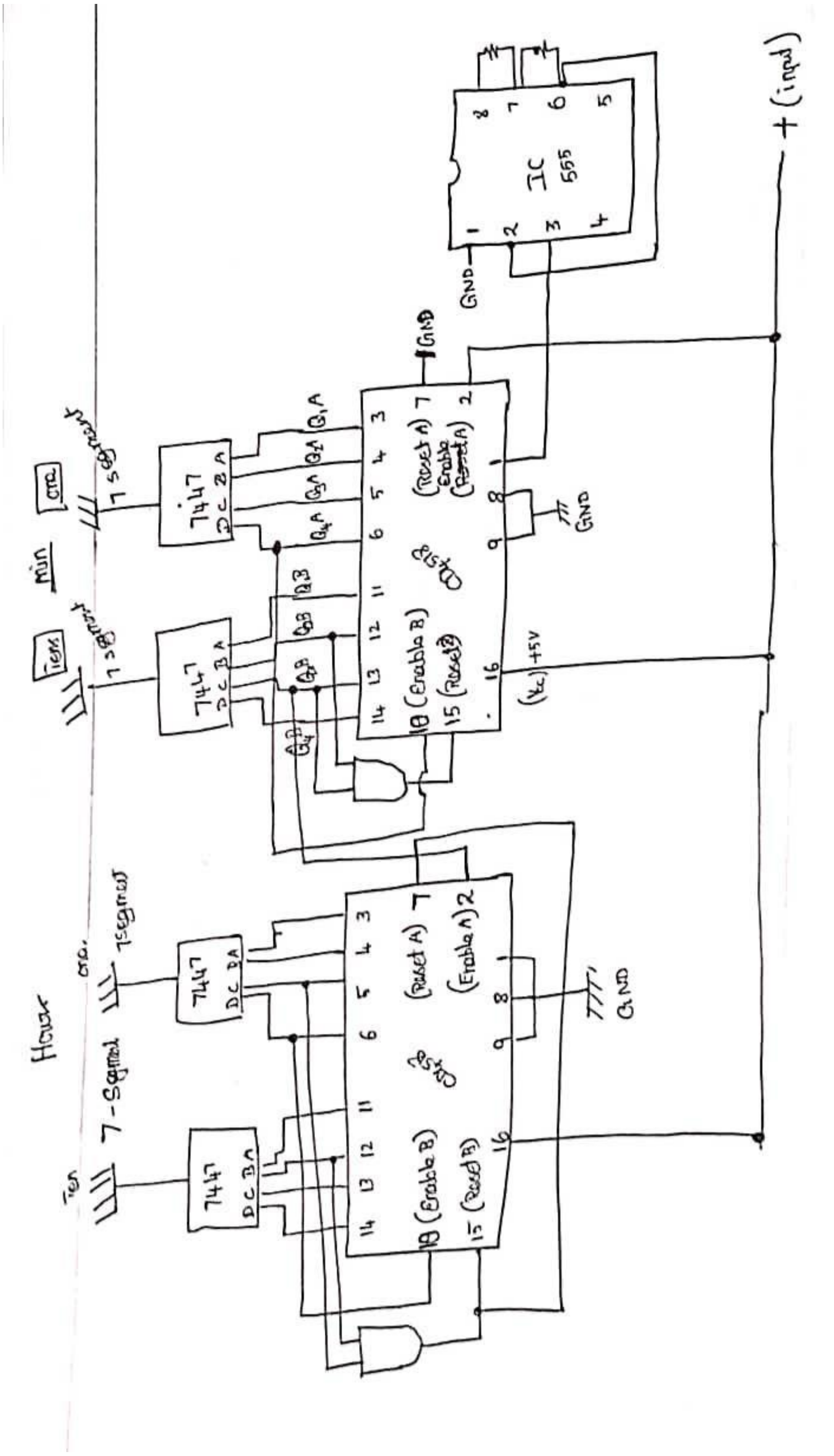
- IC 555 Timer – 1
- CD4518 (Dual Up Counter) – 2
- 74LS47(7-Segment Display Driver) – 4
- 7 Segment Display – 4
- Basic Gates -As Per Requirement
- Bread Board

Block Diagram / Architecture:-

Block Diagram:-



Circuit Diagram:-



HDL Code:-

Minute Calculation:-

```
module RailwayTimerMinute (
  input clk,
  output reg [3:0] q1A, q2A, q3A, q4A,
  output reg [1:0] q2B, q3B,
  output reg reset_minute,
  output reg [3:0] minute_tens, minute_units
);

// BCD Counter
always @(posedge clk) begin
  if (q4A) begin
    q1A <= 4'b0;
    q2A <= q2A + 1;
    if (q2A == 4'b1010) begin
      q2A <= 4'b0;
      q3A <= q3A + 1;
      if (q3A == 4'b1010) begin
        q3A <= 4'b0;
        q4A <= 1'b0;
      end
    end
  end else begin
```

```
    if (q2A == 4'b1001) begin
      q2A <= 4'b0;
      q3A <= q3A + 1;
      if (q3A == 4'b1010) begin
        q3A <= 4'b0;
        q4A <= 1'b1;
      end
end
end
end

// Additional Logic for q2B and q3B
always @(posedge clk) begin
  q2B <= q2A;
  q3B <= q3A;
  reset_minute <= (q2B & q3B);
end

// BCD to 7-Segment Decoder
always @* begin
  case ({q1A, q2B, q3B, q4A})
    4'b0000: {minute_tens, minute_units} = 4'b0000;
    4'b0001: {minute_tens, minute_units} = 4'b0001;
    4'b0010: {minute_tens, minute_units} = 4'b0010;
```

```
   4'b0011: {minute_tens, minute_units} = 4'b0011;
  4'b0100: {minute_tens, minute_units} = 4'b0100;
  4'b0101: {minute_tens, minute_units} = 4'b0101;
  4'b0110: {minute_tens, minute_units} = 4'b0110;
  4'b0111: {minute_tens, minute_units} = 4'b0111;
  4'b1000: {minute_tens, minute_units} = 4'b1000;
  4'b1001: {minute_tens, minute_units} = 4'b1001;
  default: {minute_tens, minute_units} = 4'b0101;
  endcase
end
endmodule
```

Hour Calculation:-

```
module RailwayTimerHour (
  input clk,
  output reg [3:0] q3B, q4C,
  output reg [1:0] q2D,
  output reg reset_C_D,
  output reg [3:0] hour_tens, hour_units
);

// Cascading CD4518s
always @(posedge clk) begin
if (reset_C_D) begin
```

```
    q4C <= 4'b0;
    q2D <= 2'b0;
    reset_C_D <= 1'b0;
  end else begin
    q4C <= q4C + 1;
    if (q4C == 4'b1001) begin
      q4C <= 4'b0;
      q2D <= q2D + 1;
    end
end
end

// Additional Logic for Resetting C and D
always @* begin
  reset_C_D = (q3B == 4'b1001) && (q2D == 2'b10);
end

// BCD to 7-Segment Decoder for Hours
always @* begin
  case ({q1A, q2B, q3B, q4C})
    4'b0000, 4'b1000: {hour_tens, hour_units} = 4'b0000;
    4'b0001, 4'b1001: {hour_tens, hour_units} = 4'b0001;
    4'b0010, 4'b1010: {hour_tens, hour_units} = 4'b0010;
    4'b0011, 4'b1011: {hour_tens, hour_units} = 4'b0011;
```

```
        4'b0100, 4'b1100: {hour_tens, hour_units} = 4'b0100;
        4'b0101, 4'b1101: {hour_tens, hour_units} = 4'b0101;
        4'b0110, 4'b1110: {hour_tens, hour_units} = 4'b0110;
        4'b0111, 4'b1111: {hour_tens, hour_units} = 4'b0111;
        default: {hour_tens, hour_units} = 4'b0000;
      endcase
    end
    endmodule
```

Implementation Details:-

Minute Calculation:

For minute calculation in the Railway Timer, a clock is generated using a 555 timer, with its output connected to the clock input (pin 1) of the CD4518 IC. The CD4518 functions as a BCD counter, and the outputs (q1A, q2A, q3A, q4A) represent the minute values (0-9). The enable input B is connected to q4A, ensuring a reset when it reaches 10, maintaining a 0-9 minute cycle. An AND gate, using q2B and q3B, resets the minute counter at 59 minutes. The BCD values are then decoded using a CD7447 into signals suitable for 7-segment displays, showing minutes in the range of 0-9 and 0-5 for the tens and units places, respectively.

Hour Calculation:

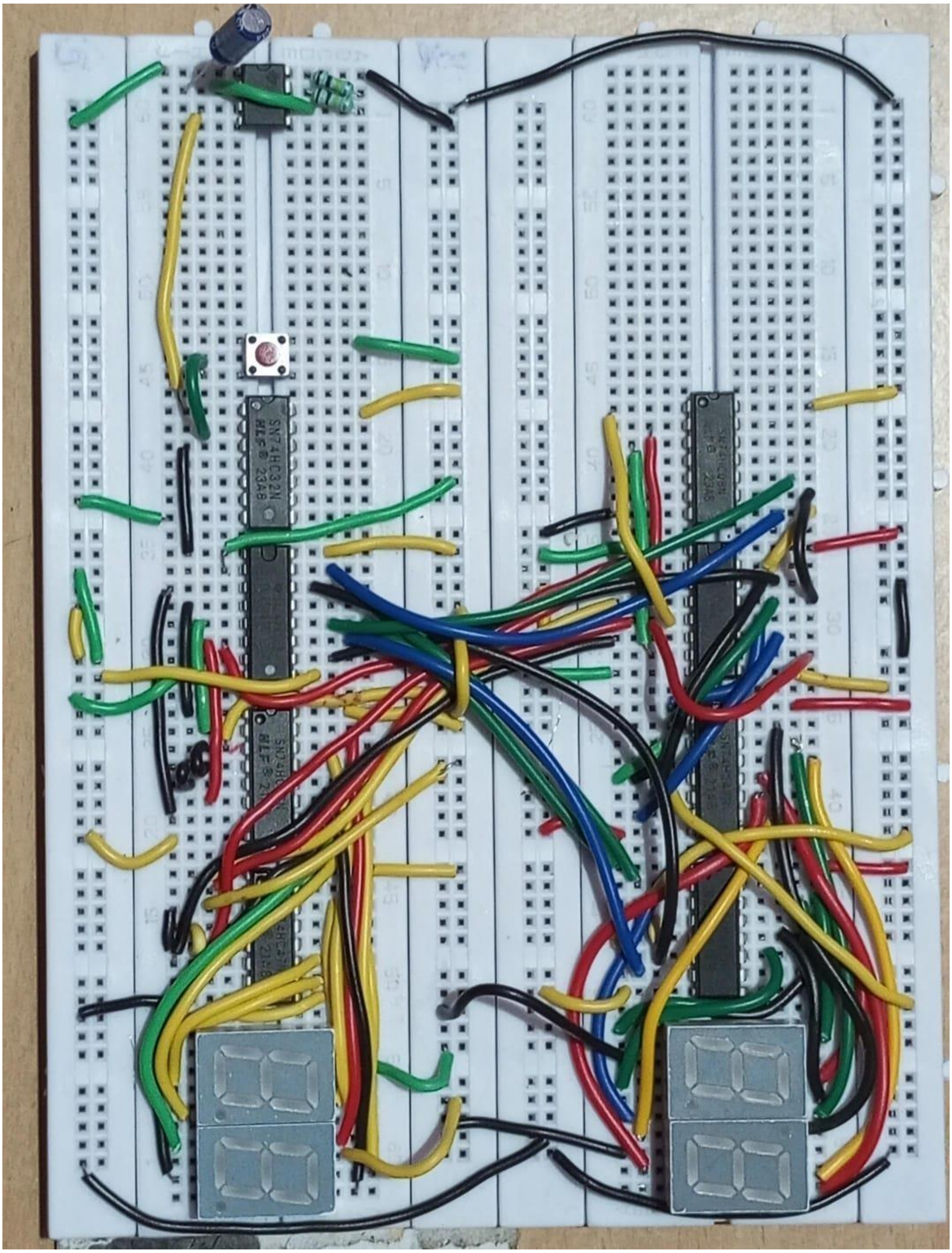
For hour calculation, q3B (from the first CD4518) is connected to the second CD4518, acting as the tens place for hours. The clock for the second CD4518 (clock C) is grounded. Q4C is connected to enable D, and clock D is grounded. An AND gate, using q3C and q2D as inputs, triggers a reset for both CD4518s (reset C and reset D) when the count reaches 24. This setup ensures the hour count remains within the 0-23 range. The decoded BCD values are then processed through another CD7447 to display hours on a 7-segment display.

Result:-

The Railway Timer implementation seamlessly combines minute and hour calculations. Using a 555 timer, the minute calculation employs a CD4518 BCD counter with added logic for a reset at 59 minutes. A CD7447 then decodes BCD values for 7-segment display presentation. For hour calculation, two cascaded CD4518 counters represent hours, with a CD7447 decoding BCD values for display. Additional logic resets counters at 24 hours, ensuring the hour count stays within 0-23. This concise implementation promises a reliable digital railway clock with accurate timekeeping.

The Verilog HDL code snippets provided earlier serve as a starting point for translating this conceptual design into a hardware description language, offering a solid foundation for further customization and integration into a hardware platform. Adjustments may be necessary based on specific hardware requirements and synthesis tools, ensuring a seamless transition from design to implementation.

Photo of the Project:



Conclusion:-

In summary, the Railway Timer project successfully integrates minute and hour calculations using a 555 timer, CD4518 BCD counters, and CD7447 decoders. The design ensures accurate timekeeping, displaying minutes and hours on 7-segment displays. The provided Verilog HDL code snippets serve as a foundation for hardware description. Overall, the project achieves a reliable digital railway clock with a focus on accuracy, efficiency, and simplicity.