SURESH MATHEW

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*Senior Member of Technical Staff at Intel's Datacenter IP Development Group with ~14 years of **DV** experience; proven track record to lead verification teams, architect complex verification environments to improve design execution and quality. A recognized leader in server IP verification with innovations in architecture and verification methodologies.*

EDUCATION

MS	**Purdue University**, Electrical & Computer Engineering Thesis: Lower Power Hardware Software Architectures for Wireless Sensor Networks Advisor: Prof. Vijay Raghunathan	August 2010
BE	**PSG College of Technology**, Electrical & Electronics Engineering Gold Medalist (conferred by Anna University) Vice Chairman, IEEE College Chapter (Mar.2005 - Mar.2006)	May 2006

PATENTS

US 10,891,240 - Mathew, Suresh, Diamond, Mitchell, Fleming Jr., Kermin *"Apparatus, Methods and Systems for Low Latency Communication in a Data Flow Accelerator"*

WORK EXPERIENCE

Intel Corporation — 2010 -Present

DV - Senior Member of Technical Staff - (2023 – Present)
BU: Data Center IP Development Group

- **IP Verification Leader**
  - ✓ Leading the 3rd generation *Non-coherent Transaction Processor IP* with a focus on delivering a highly parametrized IP to both server and client products; the IP is required for XEON register configuration, interrupt and lock distribution, and other non-coherent flows; knowledgeable in Intel's UXI and out-of-band protocols.
  - ✓ Architected an SV-UVM IP testbench; devised a comprehensive stimulus, checking and coverage strategy for a 6 member DV team; systematically drove DV execution to meet schedule and quality with no bug slips to SOCs.
  - ✓ Led coverage development for *Intel's High-Speed IO Processor IP block; d*eveloped new techniques to speed up coverage development by 50 %; traditional techniques for a complex IP can take ~15 weeks, while my new technique took less than 10 weeks; knowledgeable in Intel's cache coherency protocols, PCIE and proprietary link-layer layer protocols.
  - ✓ Responsible for developing new techniques to solve the problem of **proving validation intent**; applied data science tools like Pandas, Bokeh, etc., to improve IP verification quality (reduced false tests to < 1% from ~20%; found hard-to-find BFM knob issues, stimulus pattern issues etc.)
  - ✓ Knowledgeable in cache coherency and PCIE protocols
  - ✓ Applying Generative AI tools to interact with architectural specifications.
    - Reduces ramp time for new members of the team.

        - Generate APIs to connect architectural specifications to verification tools.

- **DV Methodology Initiatives: Post-process technologies**
    - ✓ Leading the adoption and roll-out of **post-process technologies** across the Intel's server IP org
    - ✓ Reduce checker/coverage development time by 50% by developing and self-testing all components outside the simulation using Python.
    - ✓ Decreased checker-debug and turn-around time (days to a few minutes) using out-of-simulation trace and test methodologies.
    - ✓ Improved checker quality (using self-test checkers), and increased coverage scope.
    - ✓ Spear-heading the application of data analysis tools (like Pandas, NumPy, Bokeh etc.) to gather more insights from simulation data and flush out both RTL and TB bugs early-on

DV - Member of Technical Staff - (2020 – 2023)
BU: Data Center IP Development Group

- **IP Verification Lead**
    - ✓ DV Architect and verification execution lead for the *Non-coherent Transaction Processor IP* for XEON
    - ✓ Architected scalable verification environments (in UVM) that implemented a coherent strategy for constrained random stimulus, checkers, and coverage analysis; currently leading a team of *6 DV engineers.*
    - ✓ Led the verification efforts for a *high-speed link layer protocol bridge IP* for Intel's Scalable Coherent fabric for Granite Rapids
    - ✓ Responsible for evaluating external vendors for tools and VIP development.
    - ✓ Single-handedly converted a complex IP testbench from OVM to UVM in just under a quarter, while IP execution was in progress.
    - ✓ Developed a novel method to amortize the exponential costs associated with the verification of highly parametrized soft IPs. This technique was required to maintain high IP quality, but at the same time, allowed for every increasing configuration capability for the IP.
    - ✓ Drove the adoption of Intelligent-Constraint Optimization tool, a ML offering from Synopsys to rapidly increase functional coverage and find corner case bugs faster with fewer simulation runs.
- **DV Methodology Initiative: Code Review workflow**
    - ✓ Architected, developed and rolled-out a tool that seamlessly integrated off-the-shelf code review solutions into any project's workflow.
    - ✓ Worked with external vendors, developed tooling to integrate a widely used code review tool into our custom workflows, and deployed the code review process to over 1000 engineers across the entire BU.
    - ✓ Deployed a scalable solution that allowed large teams to catch coding issues early on, gate check-ins on code review approvals and track quality metrics.
- **DV Architect: Ethernet Product Group - Architecture**
    - ✓ DV Architect for Intel's POC efforts to build Smart-NIC; led a team of contractors to verify the Smart-NIC which became the pre-cursor to Intel's IPU
    - ✓ Developed an innovative hardware-software design solution to provide any-time expansion of smart NIC offload capabilities with zero network service interrupts; this technique is now used by Intel's CSP customers. Software was written in C++.

- **Architecture Innovation Program - (6-month rotation)**
  - ✓ Spent 50% of my time working on a team that architected high-bandwidth data flow accelerations for HPC.
  - ✓ Designed a novel hardware architecture that enabled several high-bandwidth data flow accelerators to communicate control information between each other at very low latencies. Current techniques require significant resource to achieve this kind of communication. This new technique uses very little power and occupies very little/or no area.
  - ✓ **Patent issued: US 10,891,240, 2018**
- Won several divisional awards for developing novel verification techniques and tools and delivering high quality IPs for Intel's server portfolios.
- Participated in hiring activities for the BU; responsible for coaching and mentoring junior DV engineers.

Senior DV Engineer (2010-2020)
Multiple ASIC design groups at Intel

- ~**10** years developing test-plans, designing OVM/UVM testbenches, writing constrained random stimulus, checkers and driving coverage closure for two Intel's server generations and 3 Intel's Chipset generations.
- **Intel's Data Center Design Group (2013-2020)**
  - ✓ Cluster integration and verification lead for a complex subsystem in Intel's Sapphire Rapids platform
  - ✓ Led the Reliability, Accessibility and Serviceability (RAS) Expert Verification User Group for XEON for IP org on Sapphire Rapids
  - ✓ Developed the verification suite (testbench, stimulus, configuration, checkers and coverage) for Intel's out-of-band fabric on the Icelake SOC.
  - ✓ Developed a router BFM for Intel's out-of-band fabric that was re-used by multiple server IP development teams.
  - ✓ Participated in hiring activities for my IP team.
- **Intel's Chipset Development Group (2010-2013)**
  - ✓ Chipset products: CougarPoint, PantherPoint, SunrisePoint
  - ✓ Responsible for verifying PCIE and display controllers on Intel's Sunrisepoint Chipset SOC.
  - ✓ Member of the team that first ventured into IP-SOC design re-use methodology and application of OVM methodology to verification.
  - ✓ Developed a scalable build methodology that enabled SOC verification teams to easily build smaller clusters, increase SOC simulation verification throughput by 30%. Awarded the Intel Chipset and SOC IP Group Divisional Award for this effort.
  - ✓ Developed RAL adapters for multiple protocols – e.g., PCIE, and other custom Intel protocols.
  - ✓ Gained experience with SOC integration automation tools such as Synopsys CORETOOLS.

Graduate Research Assistant 2008-2010
Embedded Systems Laboratory, Purdue University

- *Research Advisor: Prof. Vijay Raghunathan*
- Research focus - Low power network protocol architectures for wireless sensor networks
  - ✓ Developed a mathematical model for performance, lifetime and feasibility metrics for on-demand wake-up in wireless sensor networks.
  - ✓ Developed a Markovian power-model analysis tool for single transmitter multi-receiver networks.

- ✓ Designed the Physical layer for RF triggered wake-up in wireless sensor networks; ultra-low power cost-effective off-the-shelf component-based circuit design; integration with CHASQUI Embedded Network sensor nodes.
- ✓ Developed the MAC Layer for RF triggered wake-up in wireless sensor networks.

- Responsible for setting up the Embedded Systems Laboratory – planning, purchase, and maintenance of equipment.

Intel, India 2006-2008
Software Engineer
BU: Intel Financial Enterprises Services Group

- Designed data-warehousing and data mining ETL products for Intel's Planning Group
- Developed algorithms and data models for optimal BOM-Routing and Schedules planning.
- Designed software applications (Oracle and Visual Basic) for Intel's Planning group to enable large scale inventory planning and scheduling.
- Responsible for planning and deploying migration of critical Tier-1 inventory system from Oracle9i/Red-Hat Linux to Oracle10g/SUSE-Linux; enabled the phase-out of legacy servers by replicating report functionality on SAP; awarded the Divisional Recognition Award
- **Member of Intel India's Innovation Group (6-month job rotation)**: Architected a novel circuit technique to allow any class of USB devices to transfer power between each other. This technique allowed a compute device (like a laptop) to charge another compute device (another laptop)
- **Awarded the Best Software Developer in the division (2007)** for developing innovative software designs and efficient product deployments that significant impact to Intel's Inventory and Reporting Services. Techniques developed reduced business application setup time by 80% and reduced application setup errors by 90%

Undergraduate Intern 2004 – 2005
Defense Research and Development Organization (DRDO), Bangalore

- Developed an Ultra-Low Power Hand-held Three-electrode Potentiostat based Hazardous Aerosol Detector; 10mW 7cmx7cm ATMega128 μC based design with a 2mW fully custom TI op-amp based signal generator.
  - ✓ Tools - AVR Programmer, ORCAD Schematic, ORCAD PCB Layout and LabVIEW
- Developed a mathematical model for dynamic Pulse Cancellation schemes for Moving Target Detectors in Radar systems using MATLAB.

TECHNICAL KILLS

Programming: System Verilog, Python, C++, MATLAB, SQL (Teradata, Oracle)

Applications/Technologies: UVM, OVM, VCS

Platforms: Linux

VOLUNTEER ACTIVITIES

Pianist and Usher at local church