2Ror1W AMP Memory IP Core

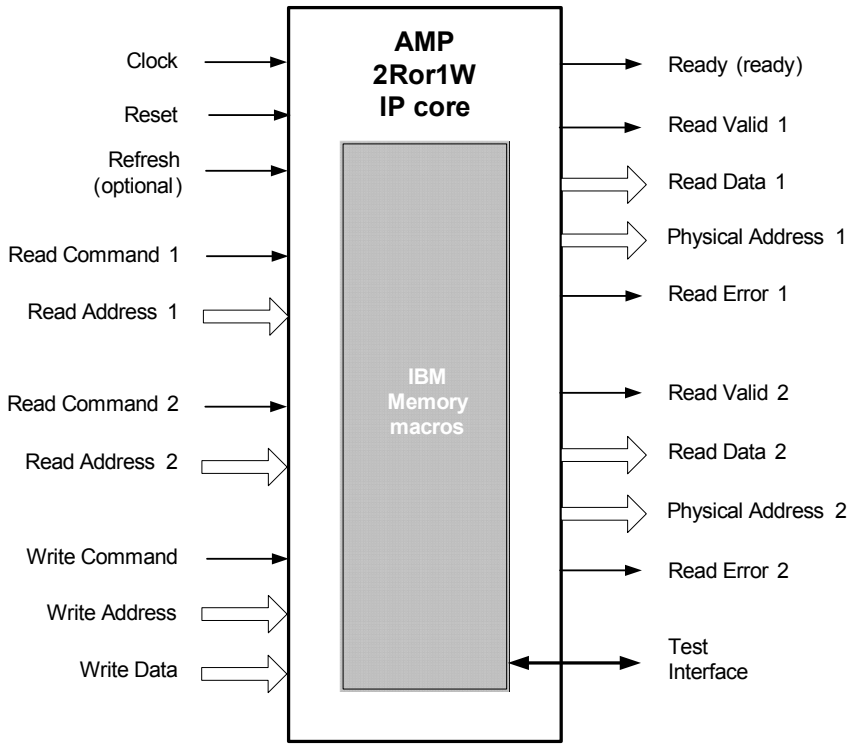
The 2Ror1W AMP memory IP core wraps around standard IBM single-port memory macros (RFs,SRAMs or eDRAMs) to support three-port functionality. The core appears to the user as a full-featured memory block with two read ports, one write port, and a simple pipelined SRAM interface.

The core can accept two independent reads simultaneously or one independent write, in every clock cycle, to any memory address. The operations of read ports are mutually exclusive with those of the write port. This performance is fully deterministic, with no exceptions, and does not have any restrictions on traffic patterns.

Each of the two read interfaces accepts an address and returns read data with a fixed delay time. The write interface accepts an address and corresponding data in the same clock cycle. The core is offered as a compiler-based soft core in which memory depth and width are specified by the user. All diagnostic and test features of the IBM base memory macros are supported as pass-through signals on the Test Interface.

This databook describes a core with an optional Refresh interface. This interface is applicable only to those AMP cores built with IBM eDRAM as base macros.

Figure 1. Block Diagram



Functional Summary

- Parameterized number of address words and data widths.
- Pipelined SRAM-like random-access interface.
- IP-core operation synchronized to master-clock (Clock) input.
- Unidirectional data-input bus and data-output bus.
- Fixed read latency irrespective of address/data patterns.
- 0.8 V to 1.05 V operation.
- Power-up: No reads or writes until the 2Ror1W core asserts its Ready output.
- Full test interface is passed through to the base macros, as specified in the IBM DRAM Databook.

Signal Definitions

Figure 2 shows the signal interface for the 2Ror1W IP core. Table 1 summarizes the function and use of the signals shown in Figure 2.

Figure 2. 2Ror1W Signal Interface

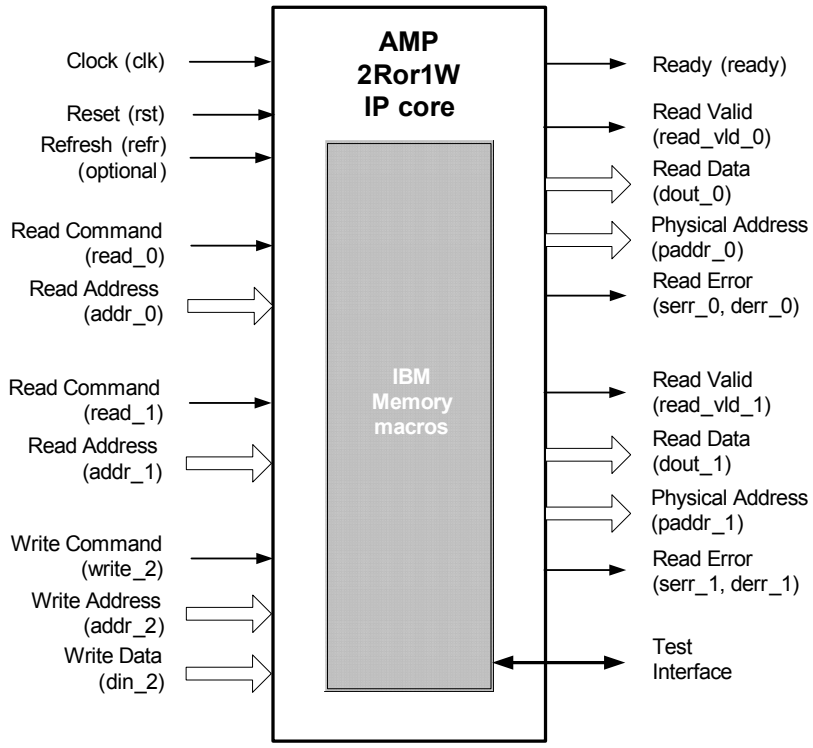


Table 1. Signal Descriptions

Function	Signal(s)	Count	Description	Input/Output
Clock	clk	1	Master clock.	Input
Read1	read_0	1	A read command is valid.	Input
Read1 Address	addr_0	1 to N	Read address bits (width *N* bits) to denote up to 2^N addresses. N is a parameter.	Input
Read1 Data Valid	read_vld_0	1	Valid read data.	Output
Read1 Error	serr_0, derr_0	1	A read data error occurred. The read data is invalid.	Output
Physical Address 1	paddr_0	M	Physical address bits associated with read data. M is a parameter. There can be up to 2^M physical addresses.	Output
Read1 Data	dout_0	W	Data associated with the Read Address. The Read Data and the Read Data Valid signals appear after a fixed latency. W is a parameter.	Output
Read2	read_1	1	A read command is valid.	Input
Read2 Address	addr_1	1 to N	Read address bits (width *N* bits) to denote up to 2^N addresses. N is a parameter.	Input
Read2 Data Valid	read_vld_1	1	Valid read data.	Output
Read2 Error	serr_1, derr_1	1	A read data error occurred. The read data is invalid.	Output
Physical Address 2	paddr_1	M	Physical address bits associated with read data. M is a parameter. There can be up to 2^M physical addresses.	Output
Read2 Data	dout_1	W	Data associated with the Read Address. The Read Data and the Read Data Valid signals appear after a fixed latency. W is a parameter.	Output
Write	write_2	1	A write command is valid.	Input
Write Address	addr_2	1 to N	Write address bits (width *N* bits). Parameter *N* is the same as that used for Read Address. N is a parameter.	Input
Write Data	din_2	W	Data associated with the Write Address. W is a parameter.	Input
Ready	ready	1	The 2Ror1W is core ready for a new read or write access. When Ready is asserted high, it stays high until a Reset or other interrupting event (like a two-bit ECC error) occurs. When Ready is negated low, a Reset is required to reassert Ready high.	Output
Refresh	refr	1	A refresh command is valid. (Optional input valid only for cores built with eDRAM base memories.	Input

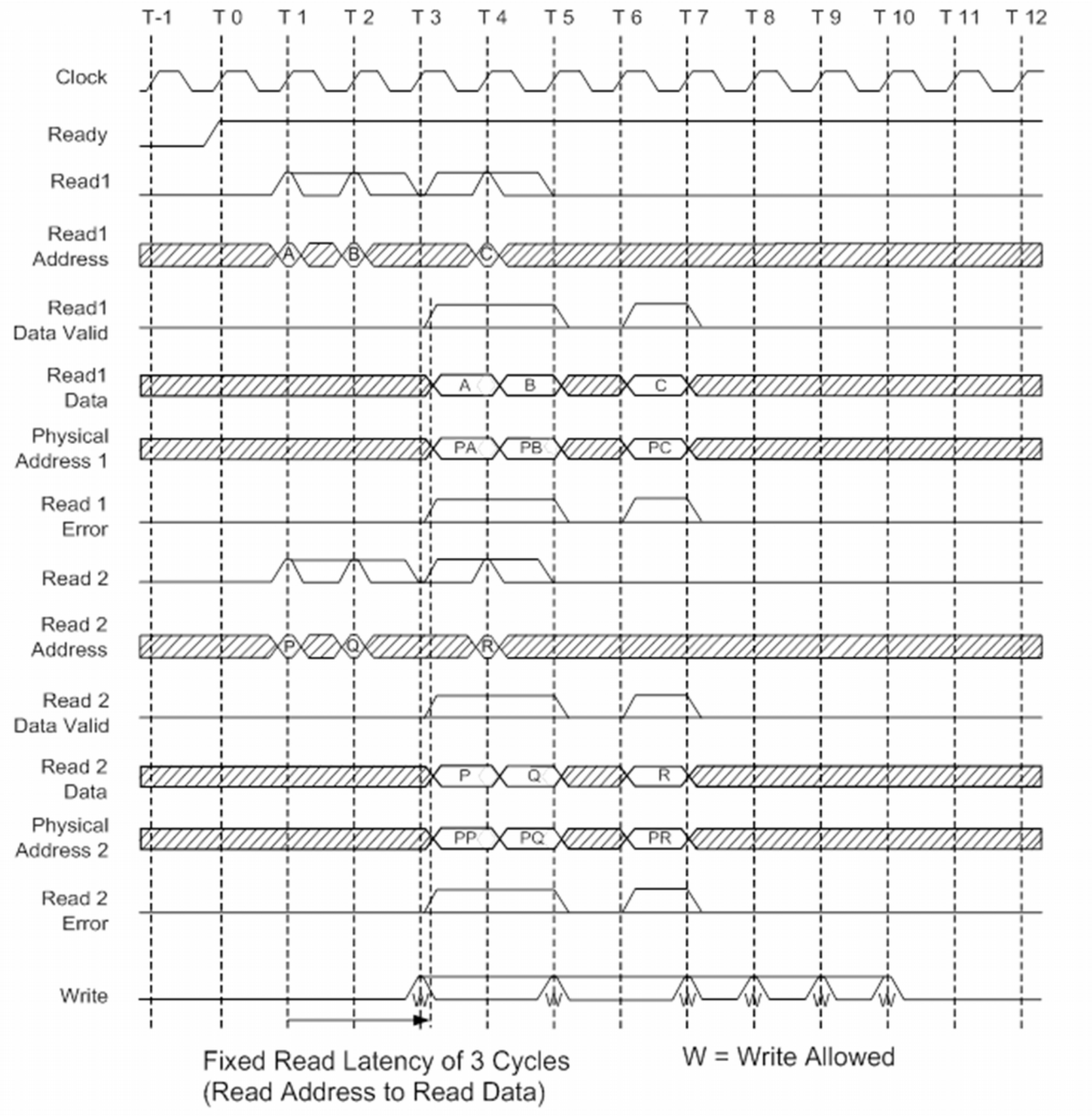
Function	Signal(s)	Count	Description	Input/Output
Reset	`rst`	1	Reset the 2Ror1W core. Initialize the base memories according to the IBM specification before asserting Reset to the 2Ror1W core.	Input
Test Interface	Same as described in the corresponding IBM base memory Databook			

Timing Diagrams

Figure 3 through Figure 6 show timing diagrams for the 2Ror1W core. For timing on the Test Interface, see the corresponding IBM base memory Databook.

Read Timing

Figure 3. Read Timing



All inputs should stay at valid signal levels and not switch unnecessarily.
Addresses are random when shown in crosshatched pattern.

Figure 3 shows six read operations—A, B, C and P, Q, R—with a read latency of three clock cycles. This latency is always fixed for a given core, irrespective of address patterns on either port. It is equal to the latency of the base memories used to build the core. The first pair of operations reads addresses A and P simultaneously in clock cycle T1; data is returned after the rising edge of clock cycle T3. The second pair of operations reads address B and

Q simultaneously in clock cycle T2; data is returned after the rising edge of clock cycle T4. The third pair of operations reads C and R simultaneously in clock cycle T4; data is returned after the rising edge of clock cycle T6.

Any number of contiguous reads can be sent, in sequential clocks, as in an SRAM interface. The reads can be done as single reads (Read1 or Read2) or in pairs of reads (Read1 and Read2). Writes are allowed only when Read1 and Read2 are both inactive.

Read Error

The 2Ror1W core implements data integrity checks on its internal metadata structures (part of the core logic). Any error detected here likely renders the read data invalid, leading to the assertion of the Read Error output(s). Assertion of *serr_x* (x = 0,1) indicates the detection of a single bit error while assertion of *derr_x* indicates a detection of multi-bit error.

Error-recovery options are described in more detail in the User Guide. The 2Ror1W core does not maintain data-integrity checks on the user data. That is the responsibility of the user. The user can choose to add ECC bits as part of data itself.

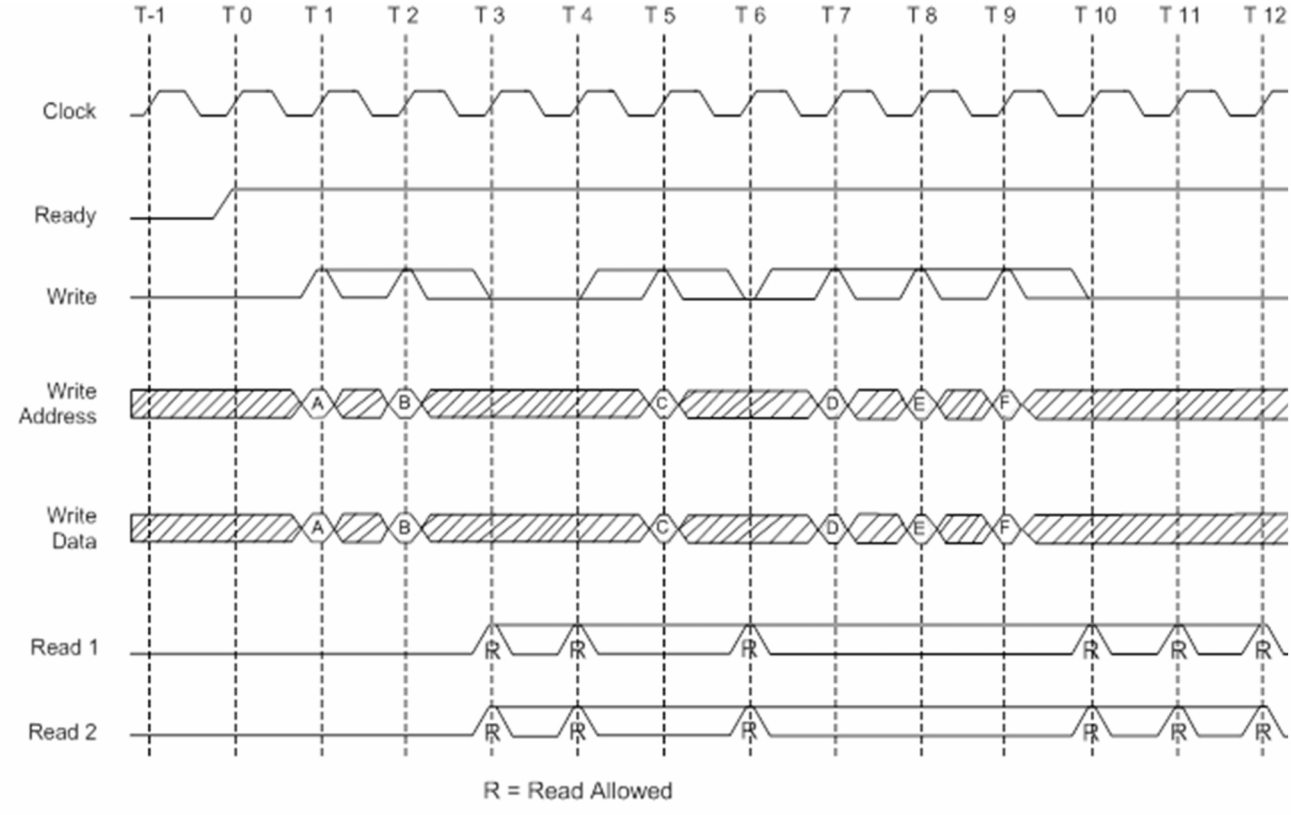
Physical Address

Figure 3 shows physical addresses associated with each read data. Due to address-mapping schemes deployed within the 2Ror1W core, the physical location of read data may not be the same as the location implied by the user provided address. The physical address is provided to help with address logging in case of ECC error events on user data (ECC management and data logging is the responsibility of the user).

In the event of a Read error, the physical address reflects the address of location where the error was detected. The details of physical address interpretation are described in the User Guide.

Write Timing

Figure 4. Write Timing



All inputs should stay at valid signal levels and not switch unnecessarily.
Addresses are random when shown in crosshatched pattern.

Figure 4 shows six write operations—A, B, C, D, E, and F. The first operation writes to address A in clock cycle T1. The second operation writes to address B in clock cycle T2. Similarly the write operations to addresses C, D, E, and F are done in clock cycles T5, T7, T8, and T9, respectively.

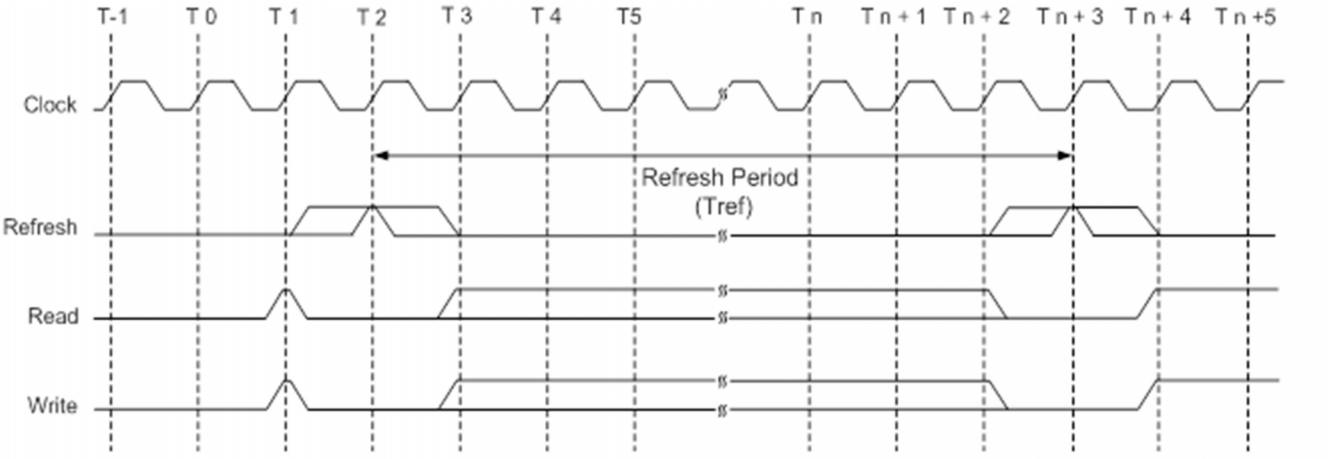
Any number of writes can be sent contiguously, in sequential clocks, as in an SRAM interface. Up to two read operations are allowed only when the Write signal is inactive.

Read and Write Interaction

A read and a write cannot occur in the same clock cycle. Thus there are no read-write conflicts, and memory operations are considered to be executed atomically in the order they are received on the read and write memory interfaces. Data written to an address is available to be read immediately from that address in the next clock.

Refresh Timing (Optional)

Figure 5. Refresh Timing



All inputs should stay at valid signal levels and not switch unnecessarily.

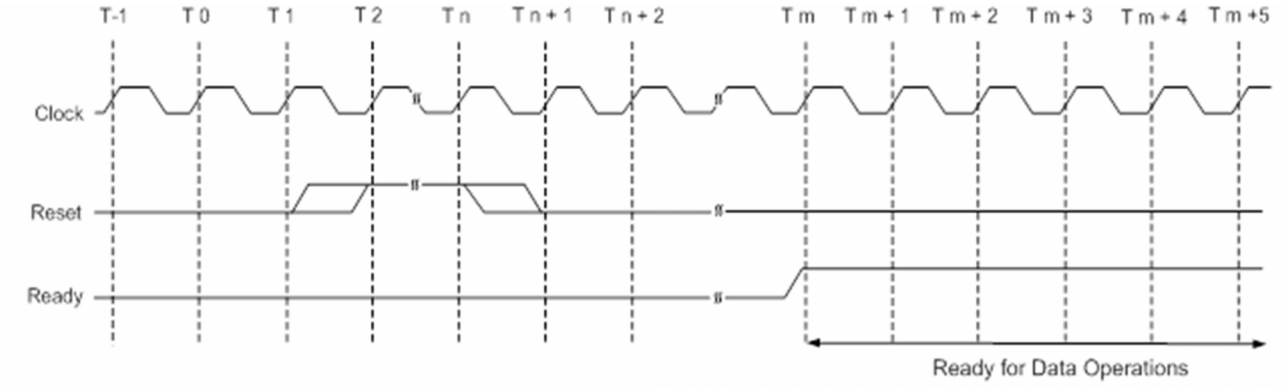
Figure 5 shows the Refresh sequence. This interface is provided only for those 2Ror1W AMP cores built with IBM eDRAM base memory macros.

The Refresh signal refreshes the DRAMA instantiated inside the core.

The user should not assert either the Read or Write command when Refresh is asserted. Doing so will result in an erroneous read or write operation. Assertion of Refresh does not affect the neighboring Read or Write operation in any way. For example, the refresh operation does not change the read-data latency for a Read command issued just prior to or after the Refresh command. It is the responsibility of the user to provide the minimum number of refreshes during the specified Refresh retention interval, T_{ref}.

Reset Timing

Figure 6. Reset Timing



All inputs should stay at valid signal levels and not switch unnecessarily.

Figure 6 shows the Reset sequence for the 2Ror1W core. The Reset signal must be held high for more than one cycle. Read or Write should not be asserted until the 2Ror1W core asserts its Ready output. The 2Ror1W core is ready to accept data operations on the next rising clock edge after Ready is asserted.

The base memory macros must be initialized according to the specification in the respective IBM Databook before Reset is asserted to the 2Ror1W core.