Algorithm f32 Microarchitecture Document

logo.png

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This document provides functional information for the f32 Algorithmic Memory® core.

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Algorithm f32 Microarchitecture

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| Date | Reviewer | Comments |
| May 12 2014 | \_\_ | Initial Release. |

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# Functional Overview

The 1r1w\_a127 IP provides 1R1W (2 port) functionality. It is built using bulk of single port memories (1RW) and a small amount of 2 port memoires (1R1W). Given the bulk of this IP is built on 1 port memories the area and power footprint of this IP is smaller than a traditional 2 port memory. The one port memory is mainly used to store the data. The two port memory stores the internal state needed by the IP logic.

This IP is implemented to reduce the read latency (Reduced Latency or RL). The target latency for this IP is gated by the latency of reading the data out from the T1 memory. The state lookup and all the relevant decisions are made in parallel and no additional cycle of latency is added on the read data path. This IP supports the following features:

|  |  |
| --- | --- |
| **Options Available** | **Description** |
| Flopping options | There are four main flopping options available in this IP – FLOPIN, FLOPOUT, FLOPMEM and FLPCMD. FLOPIN and FLOPOUT are flop stages to flop the input commands and output data. FLOPMEM flops the read data from the memory macros and the FLOPCMD flops the command to the memory macros. Typically FLOPCMD controls the flop insertion after the ECC logic and FLOPMEM controls the flop insertion right after the MEM data read. Depending on the physical design requirements they can be placed at different stages in the IP logic. For details of where these flops can be placed, look at the detailed sub-block description. |
| Sub-packing options | is supported by 1r1w\_a127. Using this option memogen can optimize the macro sizes by packing multiple logical words in one physical row. This option enables the platform to choose more optimal physical macros when the width of the required memory is small. |
| Word Write Enable | 1r1w\_a127 is the algorithm that implements the word write enable functionality on top of reduced latency 1R1W algorithm (RL). There are 8 word write enables implemented for this IP. The data width is divided into 8 words and each word write is controlled by the one bit of the write enable primary input. |
| ECC options | 1r1w\_a127 protects its internal state using double error correct ECC coding. The user data is not ECC protected. The user is responsible to add ECC overhead bits to the data and perform the ECC check and generation outside the IP. |

# Interface description

The algo\_top’s main interfaces include the clking ports; the read and write ports, which talk to the primary interface; the t1 ports which talk to the single port (T1) memories; and the t2 ports which talk to the 2 port (T2) memories.

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Pin Type | Description | Notes |
| Clock and Initialization | | | |
| clk | Input | Clock | Clock input pin |
| rst | Input | Reset | Reset pin |
| refresh | Input | Refresh | Signal to the controller that eDRAM can be refreshed in this cycle. Only needed when IP uses eDRAM. (Optional) |
| ready | Output | Ready | Assertion implies memory core ready for functional operation |
| Read Ports | | | |
| rd\_adr | Input | Read Address | Address bits (width N bits) to denote up to 2N addresses;  N is parameter. Same value for all ports |
| read | Input | Read Valid | Denotes that a Read command is valid |
| rd\_dout | Output | Read Data | Data (width W) associated with a read address;  W is parameter. Same value for all ports |
| rd\_vld | Output | Read Data Valid | Denotes valid read data |
| rd\_serr rd\_derr | Output | Read Error | Denotes read data error. Data on *dout* pins is invalid |
| rd\_padr | Output | Physical Address | Physical Address (width P bits) associated with the read. Parameter P depends on the physical address space of the memory core |
| Write Ports | | | |
| wr\_adr | Input | Write Address | Address bits (width N bits). Parameter N is the same as that used for Read address. |
| write | Input | Write Valid | Denotes that a write command is valid |
| wren | Input | Write Enable | Write data enable. Only selected data will be written to the memory and rest will be masked out. |
| din | Input | Write Data | Data (width W bits) associated with a write command; Parameter W is same that for Read data. |
| **T1 Ports** | | | |
| t1\_readA | Output | Read Valid | Denotes that the read command is valid for T1 memories |
| t1\_writeA | Output | Write Valid | Denotes that the write command is valid for T1 memories |
| t1\_addrA | Output | Address | Address bits (width N bits.) Address for both read and write command for the single port memory |
| t1\_bwA | Output | Bit write | Bit-wise write enable signal for the write data |
| t1\_dinA | Output | Write data | Write data Input to T1 memories |
| t1\_doutA | Input | Read data | Data associated with a read address; from T1 memories |
| **T2 Ports** | | | |
| t2\_writeA | Output | Write Valid | Denotes that the write command is valid for the respective T2 memory. |
| t2\_addrA | Output | Write Address | Address bits for write command |
| t2\_bwA | Output | Bit write | Bit –wise write enable signal for the write data |
| t2\_dinA | Output | Write data | Write Data input to T2 memories |
| t2\_readB | Output | Read valid | Denotes that the read command is valid for the respective T2 memory. |
| t2\_addrB | Output | Read address | Address bits for read command |
| t2\_doutB | Input | Read data | Data associated with a read address |

# Algos.txt

The memogen software uses this file to evaluate and estimate the best-fit memories for the given algo.

*# Combined Tag and Cache with 8 Word Enables*

*1R1W\_A127(f, w, b) [RL]*

*vars        : n  \_\_ bank\_count(1)*

*ws \_\_ words\_array(n,w)*

*b' \_\_ bits(b)*

*formulae    : p  = TAG\_BITS(n+1024)*

*w' = ws.max()*

*macros:*

*type1(BASE)       : n \* 1RW(f, ws, b')*

*type2             : 2 \* 1R1W(f, w', b'+p)*

The above algorithmic description defines the characteristics (frequency, depth and width) of the memory macros used for 1r1w\_a127. There are two types of memories in the IP that memogen software has to pick – type 1 (T1) and type2 (T2). The software uses the process information, user-defined parameters and the algorithmic description to decide which memories will best suit the requirements.

* **T1 Memory:** This memory is the bulk of the memory used in the 1r1w\_a127 and is used for the primary data storage. The size of this memory is equal to total capacity requirement of the algorithmic memory. The depth of the memory is equal to the depth of required memory and the width is equal to the width of the IP. In 1r1w\_a127 1RW (single port memory) is used as physical memory for T1 memory.
  + f – target frequency of T1 memory. This parameter is user defined.
  + n – is the optimal number of T1 macros or number of banks, in which the complete memory depth/capacity will be split. This parameter is optimized based on the physical library.
  + ws – The optimal depth of the T1 memory macros. For IP sizes which are non-power-of-two the tool can optimize the area using different size T1 macros. This parameter is optimized based on the physical library.
  + b’ – data width of the IP. This parameter is user defined.
* **T2 Memory:** This memory is used for two types of data – regular data that cannot be written in the T1 banks due to read and write collision, and the state data. The regular data is referred to as the cache data and the state data is referred to as the tag data. Reads are given higher priority on T1 reads. In case of a collision, write data is written to the T2 memory. The tag for 1r1w\_a127 consists of the bank number and the write enable signals associated with the writes. Note that this structure is protected by ECC (SECDEC).
  + f – target frequency of T1 memory. This parameter is user defined.
  + w’ – The maximum depth of the T1 memory macros. For IP sizes which are non-power-of-two the tool can optimize the area using different size T1 macros. w’ would be the depth of the deepest t1 macro used. This parameter is optimized based on the physical library.
  + b’ – data with of the IP. This parameter is user defined.
  + p – is the width of the tag, the write enable and state info, ECC protected.

# Block level description

An algo\_1r1we\_rl2\_pseudo\_top instantiates:

1. a1\_loop (algo) : This module consists of the two modules – core\_1r1we\_rl2 and mux. The core consists of the bulk of the algorithm and the mux translates the data from the logical p-interfaces and s-interfaces to physical T1 interfaces and T2 interfaces. The core flops the primary inputs depending on the FLOPIN parameter and dispatches read commands to both T1 and T2 memories. If a write was scheduled to the same T1 bank as a read then read gets the priority, and the write gets sent to the T2 memory, along with the state information, i.e. which bank the data belongs to, and the write enable.
2. For t1\_loop (t1 memories): This module consists of an instance of infra\_align\_bw\_pseudo, an instance of infra\_stack\_1r1w, and NUMXBNK (NUMVBNK/4) instances of infra\_stack\_pseudo. NUMVBNK is a top level parameter which is optimized by the software. It defines the number of T1 banks. The infra\_stack\_pseudo module talks to the T1 memory macros and enables the word write functionality. This last stage has a 4:1 muxing of rd data.
3. For t2s\_loop (t2 state memories): Two instances of infra\_align\_ecc\_1r1w and two instances of infra\_stack\_1r1w. Each instance controls the access to one of the two T2 memory macros. One is for read tag, other for write tag.
4. For t2d\_loop (t2 data memories): Two instances of infra\_align\_bw\_1r1w and two instances of infra\_stack\_1r1w. One instance is for Read cache, and other for write cache. The two instances sit closest to the T2 memory macros.

****

**Figure1: Block diagram for Algo\_top**

# Key Parameters

The 1r1w\_a127 algo uses the following key parameters:

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Description** | **Software Controlled** | **Hadware controlled** |
| WIDTH | Data width of the IP; It defines width of the data bus | <To be filled> | <To be filled> |
| NUMADDR | Depth of memory IP; Total address space for the IP |  |  |
| NUMVROW | Number of Virtual Rows; Number of rows in the T1 bank |  |  |
| NUMVBNK | Number of Virtual Banks; Number of T1 banks |  |  |
| BITPADR | Number of bits sufficient for all the banks in the design (T1 and T2 banks), used for physical address interface |  |  |
| NUMWRDS | Align Parameter |  |  |
| NUMSROW | Number of rows for select address; Select address is used for formal verification convergence |  |  |
| NUMWBNK | T2 packing parameter. Internally: T1 Number of banks per stack |  |  |
| SRAM\_DELAY | Delay to access T1 banks |  |  |
| DRAM\_DELAY | Delay to access T2 banks |  |  |
| FLOPIN | Controls the flopping option on input command signals. |  |  |
| FLOPOUT | Controls the flopping option on output signals. |  |  |
| FLOPCMD | Controls the option to flop the command to memory. |  |  |
| FLOPMEM | Controls the flopping option of data from memory. |  |  |
| ECCBITS | Controls the ECC bits in the state memory |  |  |

# Formal

The Cadence’s formal tool (ifv) is run using the frun.sh script which takes run\_ifv as it’s input. It is run under run\_sample/fv/<cut> directory. It pulls tcl scripts from the tree and runs all the formal proofs. To run a specific proof, frun.sh can be run with –r <check> option. And to run in gui mode, a –gui option may be used.

Following are the primary design constraints and the assertions for the 1r1w\_a127 algo:

Primary design constraints:

Leaf nodes/assertions to prove:

*des.algo\_top.a1\_loop.algo.ip\_top\_sva.assert\_dout\_check*

*des.algo\_top.a1\_loop.algo.ip\_top\_sva.assert\_fwrd\_check*

*des.algo\_top.a1\_loop.algo.ip\_top\_sva.assert\_padr\_check*

**Memoir ip**

FAKEMEM

FAKEMEM

FAKEMEM

FAKEMEM

FAKEMEM

FAKEMEM

FAKEMEM

FAKEMEM

1RW SRAM

1R1W SRAM

Logic Cone

1R1W SRAM

Logic Cone

Logic Cone

Read Data Bus (dout)

dout check

FAKEMEM

Golden Reference Model

Assertion

Write path

Read path

Write Data Bus

The diagram above shows the logical view of how the IP is verified formally. The complete IP is sliced into several logic cones. Each cone has a corresponding golden memory model (fakemem). When a write request is launched at the input of any logic cone, it gets captured in the golden memory. On a read, we compare the read data returned by the logic cone with golden memory. The read check happens on the interface of the cone of logic. This check is captured in the form of an SVA assertion or a property. Formal verification when run, will try to prove or break these assertions. The assertions cover the complete code, including the logic inside each cone and all the interfaces between the cones.

The diagram below zooms into one of the logical cones. It shows a simplified golden memory model and a simplified code for a read dout assertion. The formal tool exhaustively toggles all the (primary) input pins, complying with the constraints, to try and break the assertions.

rd\_dout

rd\_addr, read

wr\_adr, bw, din

Logic cone 1

FAKEMEM

Golden Memory for

Logic cone 1

Logic cone 2

FAKEMEM

Golden Memory for

Logic cone 2

***assert rd\_dout\_check: assert property (@(posedge clk) disable iff (rst) (read && (rd\_adr == select\_addr)) |-> ##(MEM\_DEL) (fakememinv || (rd\_dout[select\_bit] == fakemem)));***

dout check assertion

for logic cone 1

***reg fakememinv;  
reg fakemem;  
always @(posedge clk)  
  if (rst)  
    fakememinv <= 1'b1;  
  else if (write && (wr\_adr == select\_addr) ) begin  
    fakememinv <= 1'b0;  
    fakemem <= din[select\_bit];  
  end***

To evaluate the formal coverage of the design, we have a post processing flow developed inhouse. The fchkr.sh script retrieves all the checks/assertions in the design. Then it parses all the logfiles to make sure that all the assertions are (formally) proven to give us a 100% coverage of our design. It prints out the constraints, asssertions and proven assertion for each run. To report more information, use –ll option with the fchkr.sh script.

Several design for verification techniques have been used to guarantee that formal tool is able to converge proofs completely on the IPs. The simple semantic of memory IPs (i.e. read data to an address should be the last data written to that address) have also been a key in the formal results we achieve for the IP. The goal of the techniques mentioned above is to reduce the state space both temporally and spacially. We use these to help the formal tool converge the properties exhaustively.

# Dynamic Simulation

Random traffic bombards the input pins and is stored in a golden memory. On the read, output data is compared against the golden memory.

# Revision Change Log

|  |  |  |
| --- | --- | --- |
| Version | Date of Release | Notes |
| V1.0 | Apr 16 2014 | Initial Release. |

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