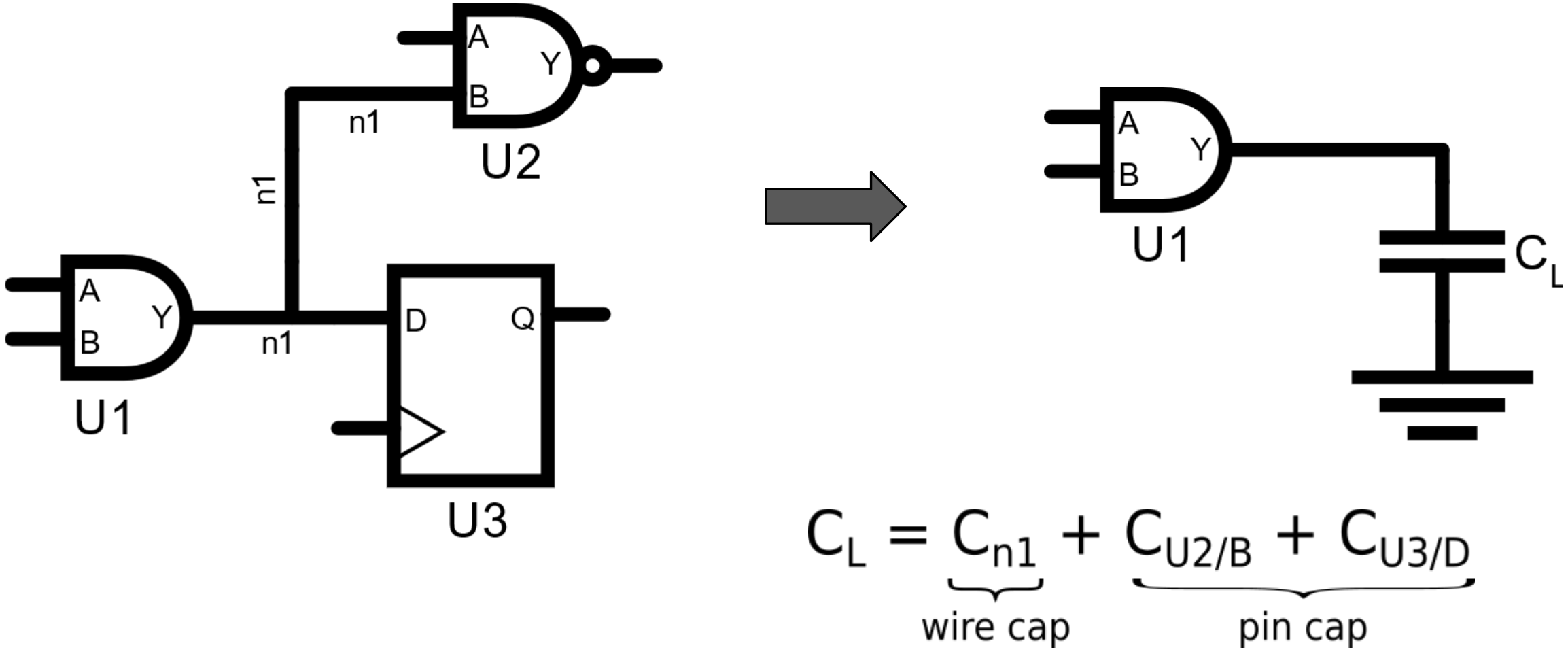
Power Consumption

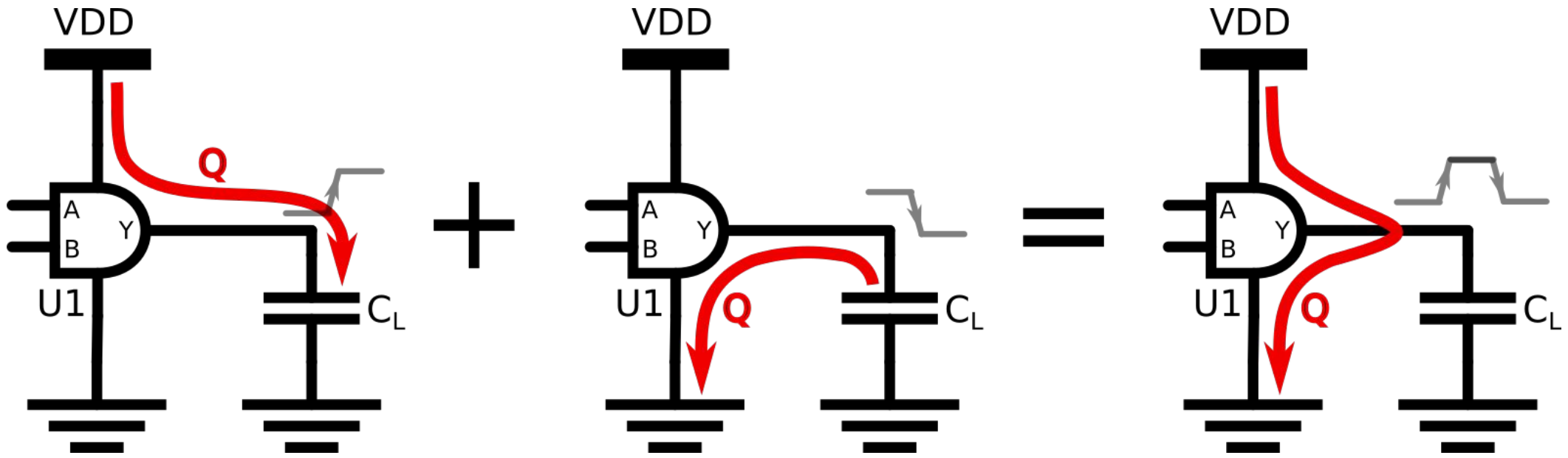
SPECIAL TOPIC 2

Load Capacitance of a Gate



$$C_L = \underbrace{C_{n1}}_{\text{wire cap}} + \underbrace{C_{U2/B} + C_{U3/D}}_{\text{pin cap}}$$

Switching Activity: Charge Flow



Low-to-High (L-H)

High-to-Low (L-H)

Pulse (L-H + H-L)

- $Q = C_L V_{dd}$
- For every pulse, charge Q flows from VDD to GND

Switching Activity: Power Dissipation

- Energy dissipated for every pulse, when charge Q flows from VDD to GND:

$$E = QV_{dd} = (C_L V_{dd})V_{dd} = C_L V_{dd}^2$$

- Power is energy dissipated per second.
- If there are n_p pulses per second at a gate's output, switching power dissipation of the gate is:

$$P = C_L V_{dd}^2 n_p$$

Switching Power for Clocks & Data

- For a clock with frequency f, $n_p = f$
  - Switching power dissipation of a buffer driving clock is:

$$P = C_L V_{dd}^2 f$$

- For data signals, we define an activity factor, α:

$$\alpha = n_p / f$$

  - Switching power for driver of such a signal is:

$$P = C_L V_{dd}^2 f \alpha$$

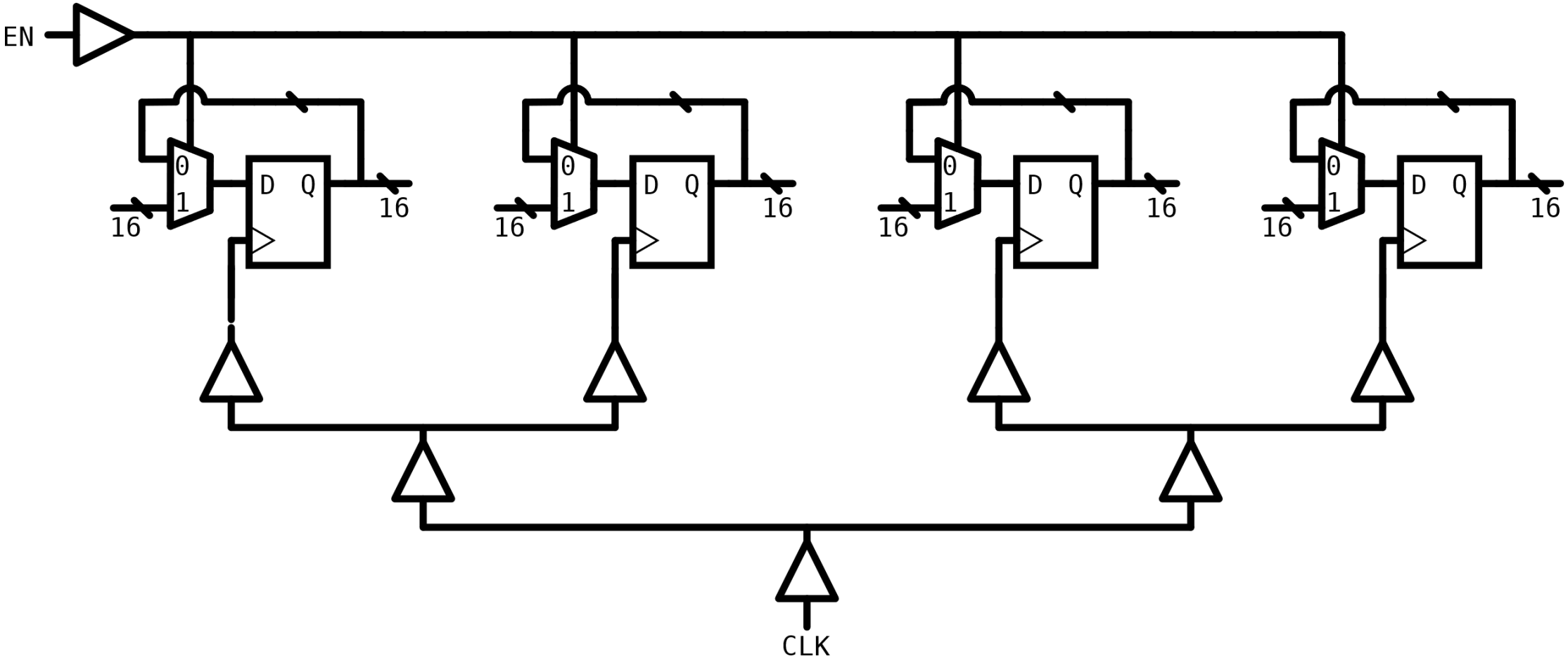
  - Generally, $\alpha << 1$ and clock is the most active signal in the circuit

Clock Gating

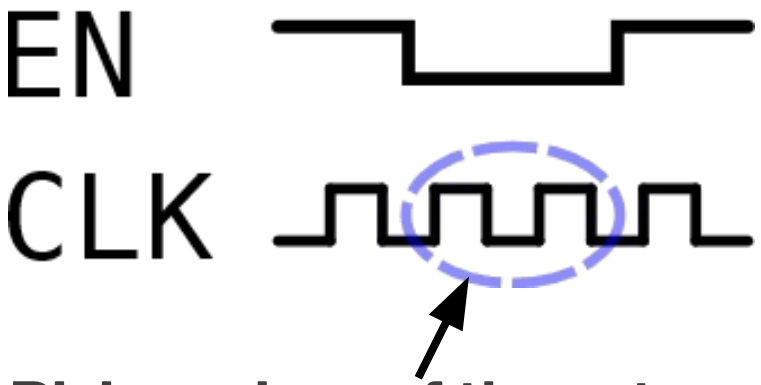
SPECIAL TOPIC 3

Clock Gating

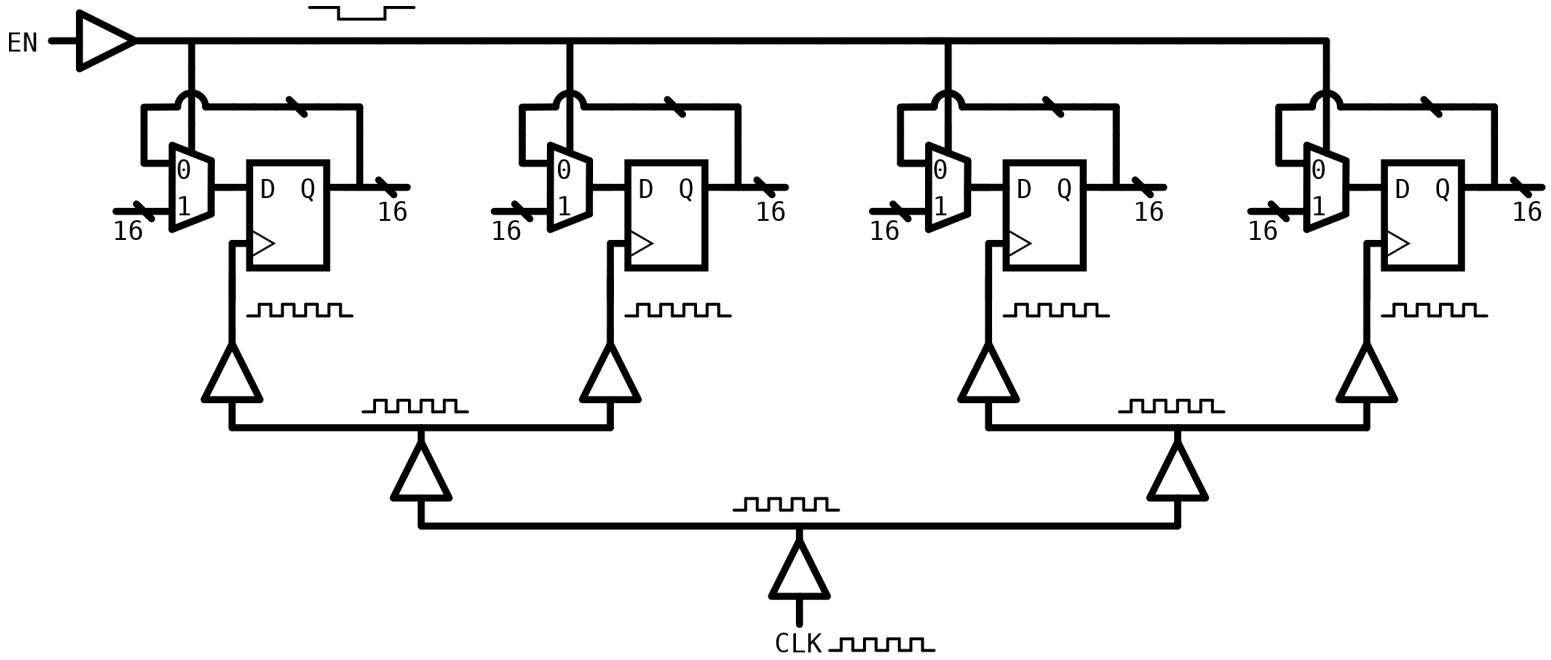
64-bit register which changes state only when some enable signal, EN, is high:



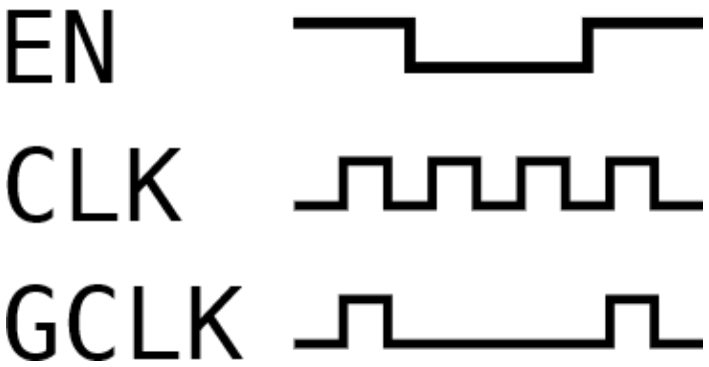
Circuit without Clock Gating

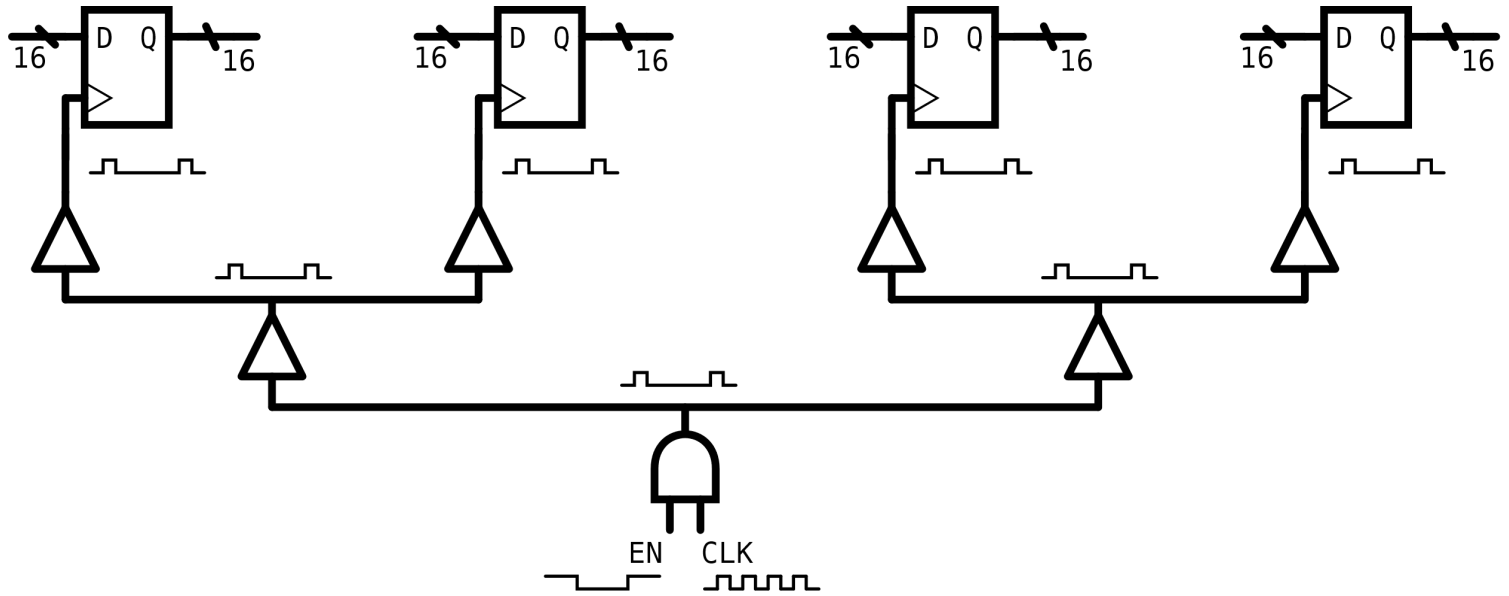


Rising edges of these two pulses do no work since E is low ⇨ pulses can be eliminated to save power



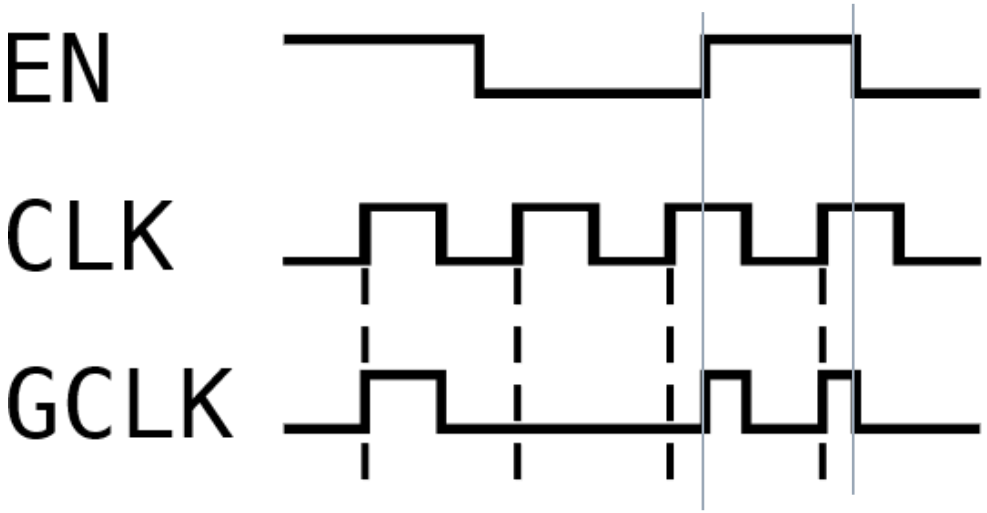
Circuit with Clock Gating

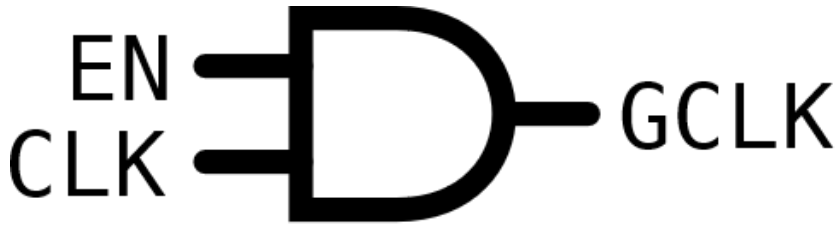




GCLK: gated clock

Problem with using AND gate for clock gating

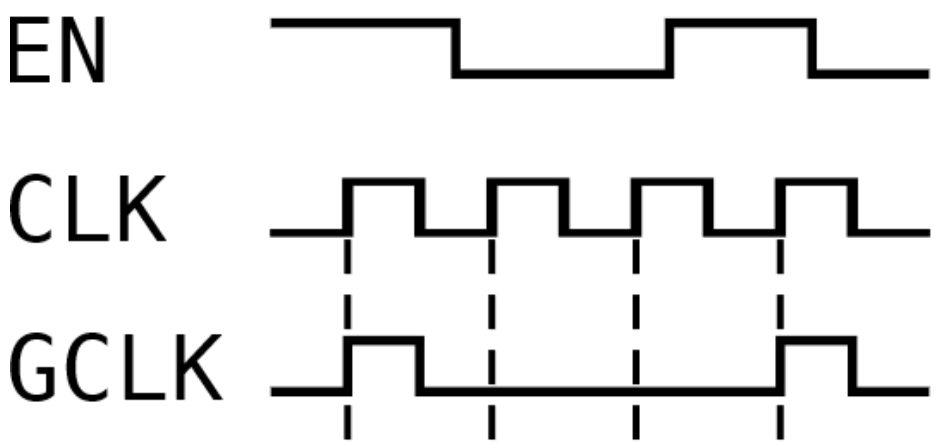


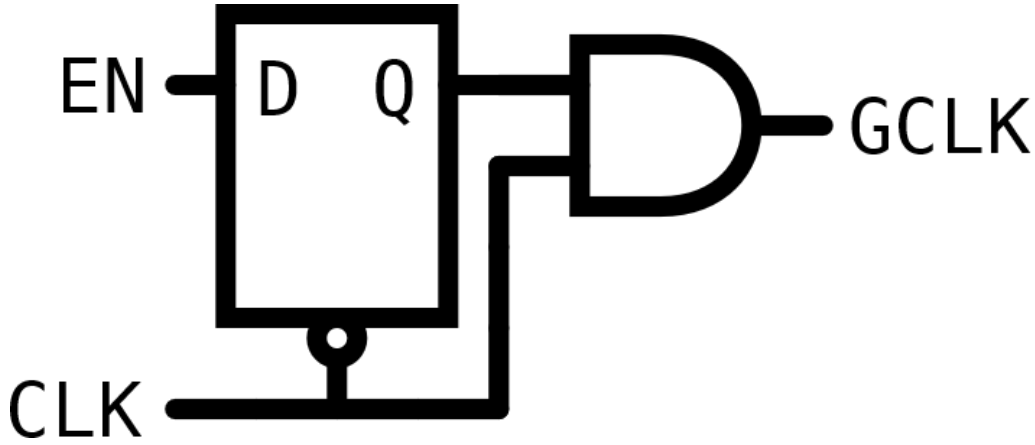


- **If EN changes when CLK is high, we get incorrect clock edges:**
  - **Cannot let EN change when CLK is high**

Integrated Clock Gating Cell (ICG)

- **Cannot let EN when CLK is high: use latch (level-sensitive) to block EN when CLK is high**
  - **Latch is transparent when CLK is low**
- **Combination of latch and AND gate is called an "Integrated Clock Gating" cell (ICG)**

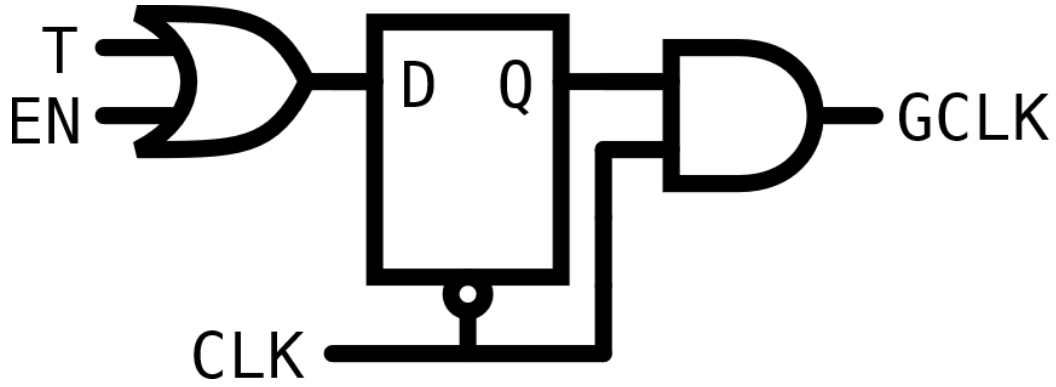


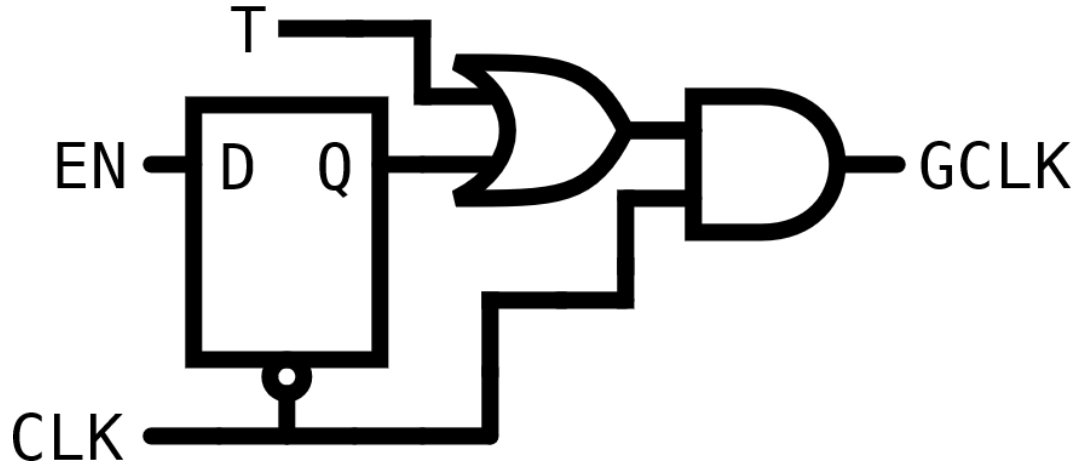


- **EN does not go through to the AND gate when CLK is high**
  - **Latch is transparent with CLK is low**

ICG with Test Feature

- When chip is being tested, clock must be ungated regardless of value of EN
  - Add “test” input (T) to ICG to bypass EN during test:

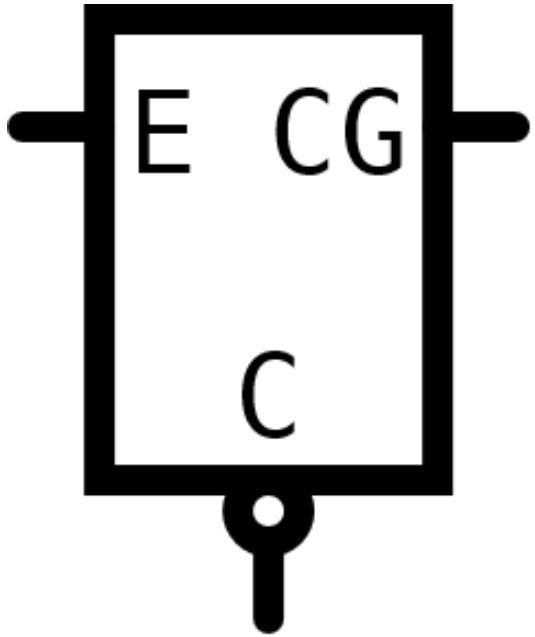




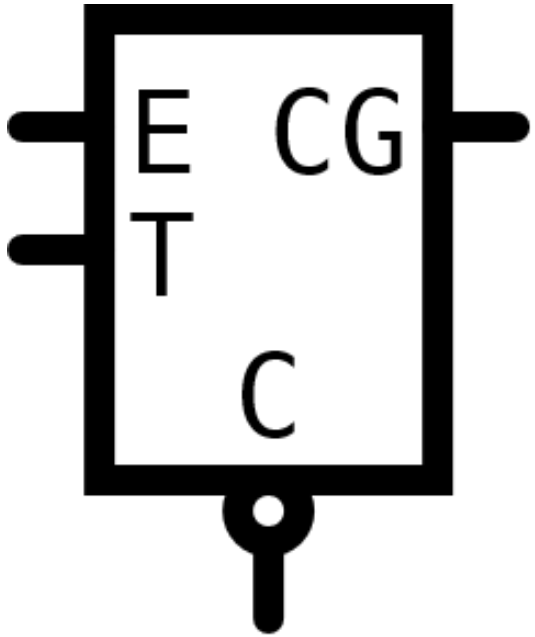
- T = 1 when circuit is being tested
- ICG is transparent to CLK when T = 1, regardless of value of EN

Symbol for ICG

- There is no standard symbol for an ICG
- We will use the following as symbols for ICGs in this class:



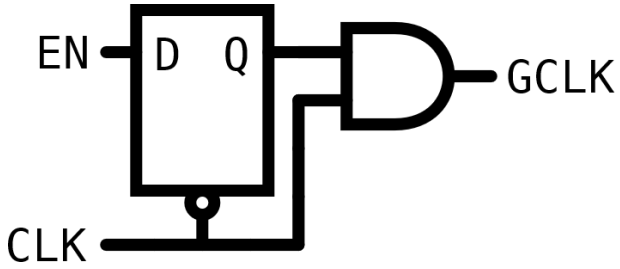
ICG without test input



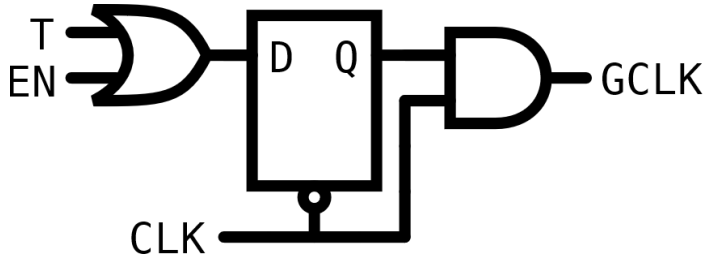
ICG with test input

ICGs in Standard Cell Libraries

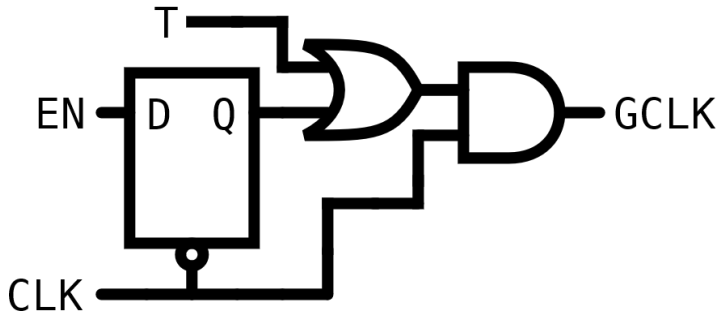
- Most standard cell libraries contain ICGs
- In the dotlib, ICGs, and only ICGs, must have the attribute “clock_gating_integrated_cell” defined



clock_gating_integrated_cell : latch_posedge;



clock_gating_integrated_cell : latch_posedge_precontrol;



clock_gating_integrated_cell : latch_posedge_postcontrol;