```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   03:21:09 12/18/2025
8   // Design Name:   sync_counter
9   // Module Name:   E:/New folder/sync_counter/tb_sync_counter.v
10  // Project Name:  sync_counter
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: sync_counter
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24  module tb_sync_counter;
25  reg clk, reset;
26  wire [3:0] count;
27  sync_counter uut (.clk(clk), .reset(reset), .count(count));
28  initial begin
29      clk = 0;
30      forever #5 clk = ~clk;   // 10ns clock period
31  end
32  initial begin
33      $display("Time   Reset   Count");
34      reset = 1; #10;
35      reset = 0;
36   repeat(20) begin
37          #10 $display("%0dns    %b       %b", $time, reset, count);
38      end
39      $stop;
40  end
41  endmodule
42
43
```