Vellore Institute Of Technology, Chennai

B.Tech (5th Semester (2020-2021))

CAT II Examination

Parallel Distribution System(CSE4001)

Max Marks : 30 Time : 3 Hours

Note: There are three Questions in this paper . All Questions are compulsory.

Max marks for all Question are 10

Attempt ALL Questions.

Question 1: Using shared memory programming model, write a program to generate the following series in the given range 1 to N. Series: 1,5,4,9,9,15,16,23,25,33,...Find sum of all numbers in the series once the series is generated

Question 2: Apply suitable decomposition technique for the problem given below and justify. Draw task dependency graphs. Comment on the maximum degree of concurrency and granularity.

Question 3: For the following question assume that the pipeline contains 5 stages: IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). Each stage except EX requires one clock cycle. System contains 4 functional units for floating point (FP) operations for FP-load / store, FP-addition / subtraction, FP-multiplication and FP-division.
EX-stage for Load / Store operations contains 1 clock cycle

(EX); for ADDD or SUBD operations contains 1 clock cycle (A or S); for MULTD operation contains 3 clock cycles (M1, M2, M3), and for DIVD operation contains 4 clock cycles (D1, D2, D3, D4).