SIKSHA 'O' ANUSANDHAN

(DEEMED TO BE UNIVERSITY)

Department of Electronics and Communication Engineering (ECE)

Institute of Technical Education and Research

COMMUNICATION SYSTEM - I

(EET3061)

DESIGN PROJECT

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DECLARATION

I certify that

a. The work contained in this report is original and has been done by me.
b. I have followed the guidelines provided by the Institute in preparing the report.
c. I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.
d. I have tried to complete the work with minimum possible cost.
e. Whenever I have used materials (data, theoretical analysis, figures, and text) from other sources, I have given due credit to them by citing them in the text of the report and giving their details in the references.

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PROBLEM STATEMENT

The project aims to design and implement a circuit capable of down-converting the frequency of an input signal from 2 kHz to 1 kHz using a combination of analog components, including a 555 Timer IC and an AD633AN Analog Multiplier IC, while ensuring accurate and stable operation. The system should effectively filter unwanted higher-frequency components to output a 1 kHz signal, adhering to the following conditions:

1.**Input Signal:** A 2 kHz sine wave.

2.**Reference Signal:** A stable 1 kHz sine wave generated using a 555 Timer configured in astable mode.

3.**Multiplier:** An AD633AN IC will be used to mix the input and reference signals, creating a composite signal with both sum and difference frequencies.

4.**Output Signal:** A low-pass filter will isolate the desired 1 kHz signal, ensuring a clean sine wave output for further processing or analysis

CIRCUIT OPERATING CONSTRAINTS

IC's :-

555 Timer:

Operates typically between **4.5V to 15V**.

Ensure the supply voltage matches the specifications of both the 555 timer and the AD633AN.

Noise or instability in the supply voltage may cause frequency instability in the 555 timer output.

AD633AN:

The typical supply voltage range is **±8V to ±15V** for dual supplies.

Ensure proper decoupling capacitors near the power pins to reduce noise.

Frequency Limitations :-

Input Signal Frequency (2 kHz):

The AD633AN can handle signals in the audio frequency range. Ensure that 2 kHz falls within its linear operational frequency range.

Reference Signal (1 kHz):

The 555 timer must generate a stable and accurate 1 kHz sine wave.

Low-Pass Filter Components :-

Ensure the RC values are accurate to set the cut off frequency near 1 kHz.

Low-Pass Filter Design :-

Cut off Frequency:

Ensure the cut off frequency is accurately set to 1 kHz to remove higher-frequency components (e.g., 3 kHz) while retaining the desired 1 kHz signal.

Environmental Factors :-

Temperature:

Both the 555 timer and AD633AN have temperature-dependent characteristics. Avoid extreme temperatures to maintain stable operation.

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THEORETICAL BACKGROUND

1.INTRODUCTION :-

Frequency down-conversion is a critical technique in signal processing, communication systems, and audio engineering, where higher-frequency signals need to be shifted to a lower frequency for easier analysis, transmission, or further processing. This project focuses on designing a circuit that down-converts a 2 kHz input signal to 1 kHz using a combination of analog components, including a 555 Timer IC and an AD633AN Analog Multiplier IC. The design leverages the versatility of these components to achieve accurate and efficient frequency manipulation. The 555 Timer, configured in astable mode, generates a stable 1 kHz sine wave as a reference signal. This reference signal is then fed into the AD633AN, a precision analog multiplier, alongside the 2 kHz input signal. The multiplier outputs a signal containing both sum (3 kHz) and difference (1 kHz) frequencies. To extract the desired 1 kHz signal, a carefully designed RC low-pass filter is used to suppress the higher-frequency components, leaving a clean 1 kHz output.

IC 555 Timer:

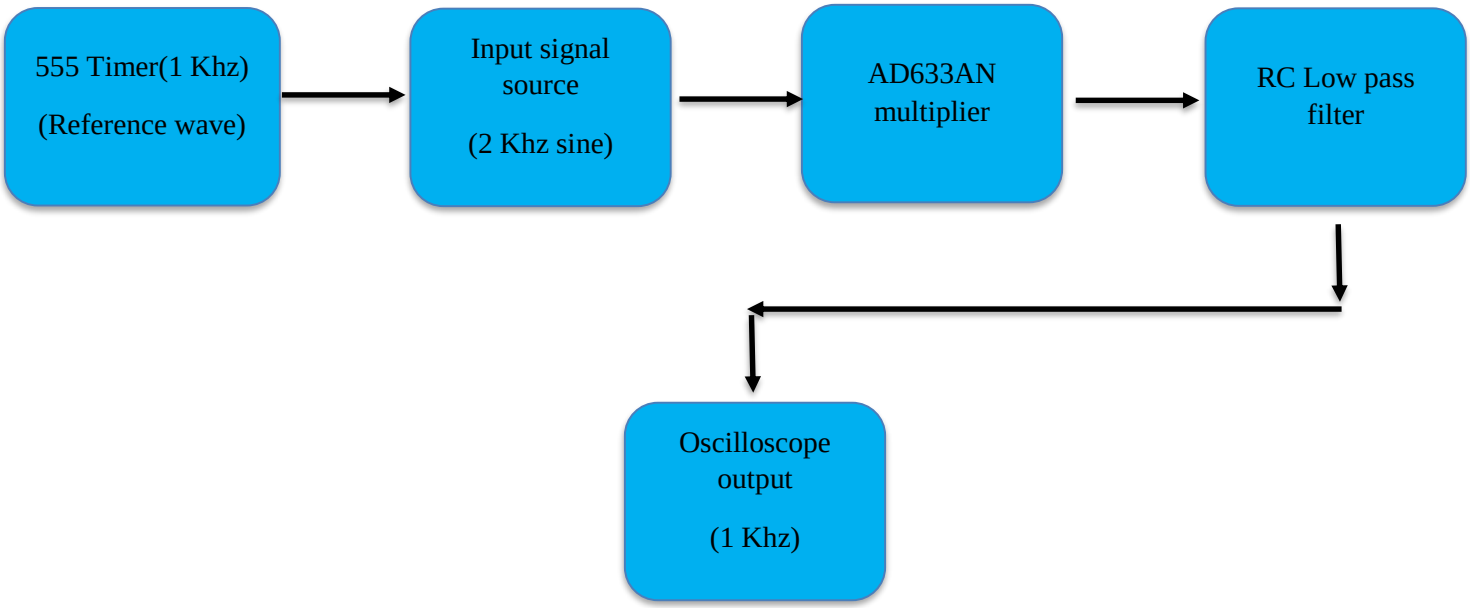
The 555 Timer IC is a widely used and versatile component in electronics, known for its simplicity and reliability in generating precise timing and waveform signals. In this project, the 555 Timer plays a crucial role as a frequency generator to produce a stable 1 kHz sine wave signal, which serves as the reference signal for the frequency down-conversion process.

IC AD633AN:

The AD633AN is a precision analog multiplier IC commonly used in signal processing applications. In this project, it plays a key role in the frequency down-conversion process, where it multiplies the input signal (2 kHz sine wave) with a reference signal (1 kHz sine wave) to produce sum and

difference frequencies. The ability of the AD633AN to handle precise signal multiplication makes it an ideal choice for implementing this function.

2.BLOCK DIAGRAM :-



3.MATHEMATICAL MODELLING / ANALYSIS :-

The formula to get the values of resistor and capacitor in 555 timer is:-

$$f=1.44/(R1+2R2)*C$$

Let the value of capacitor be C=0.01uf and the value of f is 1khz as we want to generate a 1khz signal.

So now solving this we get R1+2R2=144000 ohm or 144 kohm

From this let R1=44 kohm

So R2=50 kohm

Now we have to find the values of resistor and capacitor for the RC low pass circuit.

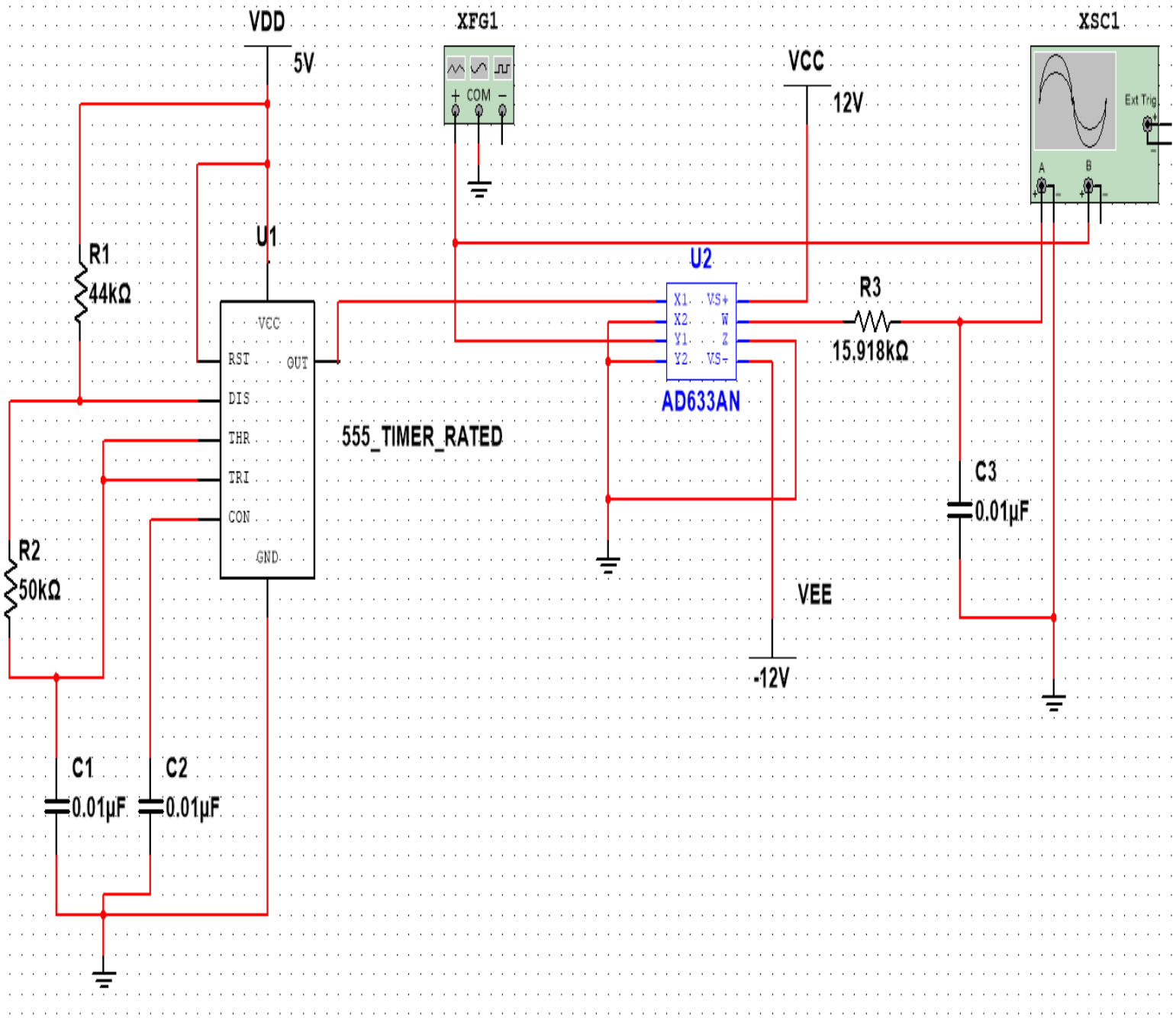
We know that in a LPF circuit,

fc=1/2*pi*R*C

let C=0.01uf and here fc is 1khz

so R=15.918 kohm

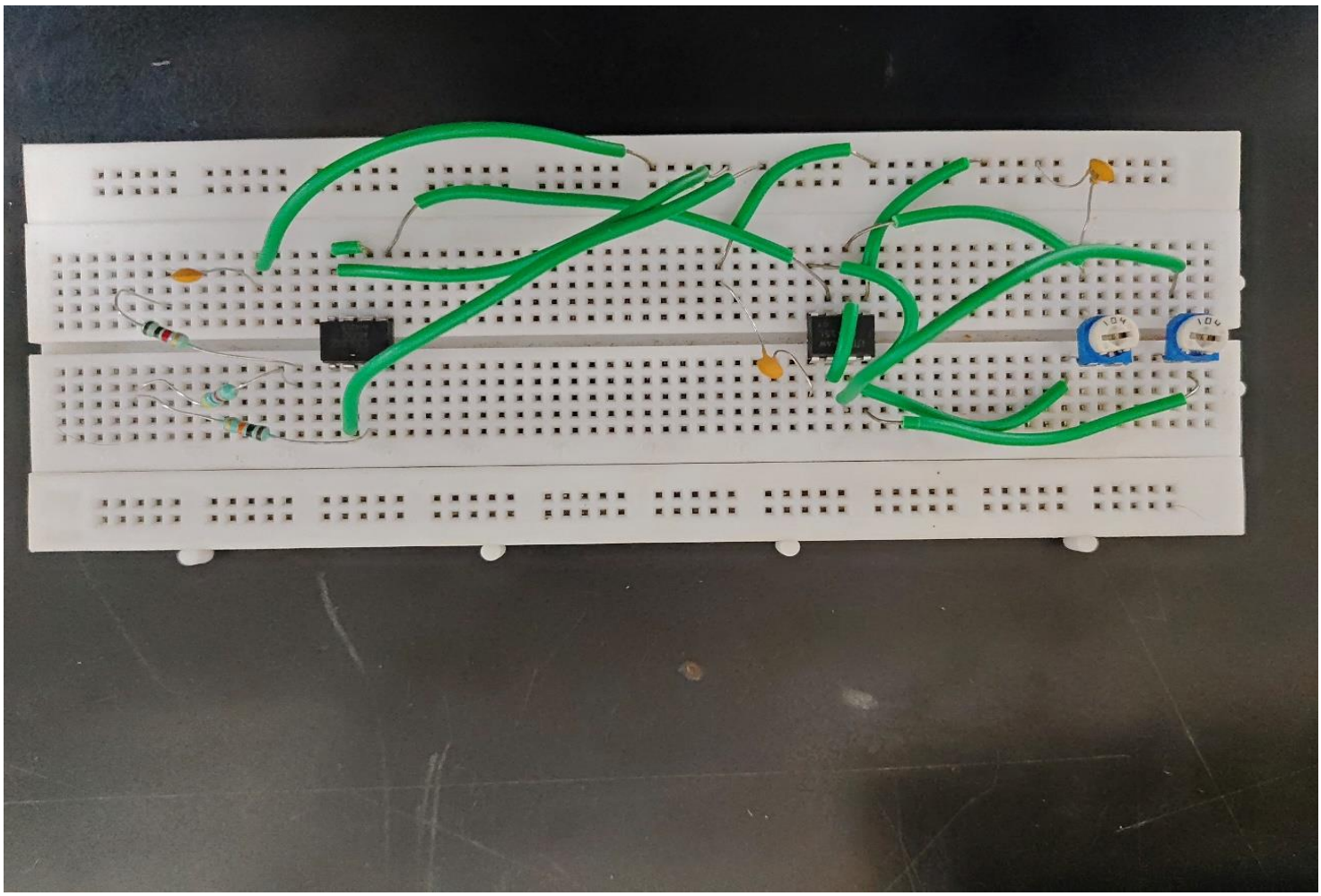
CIRCUIT DIAGRAM

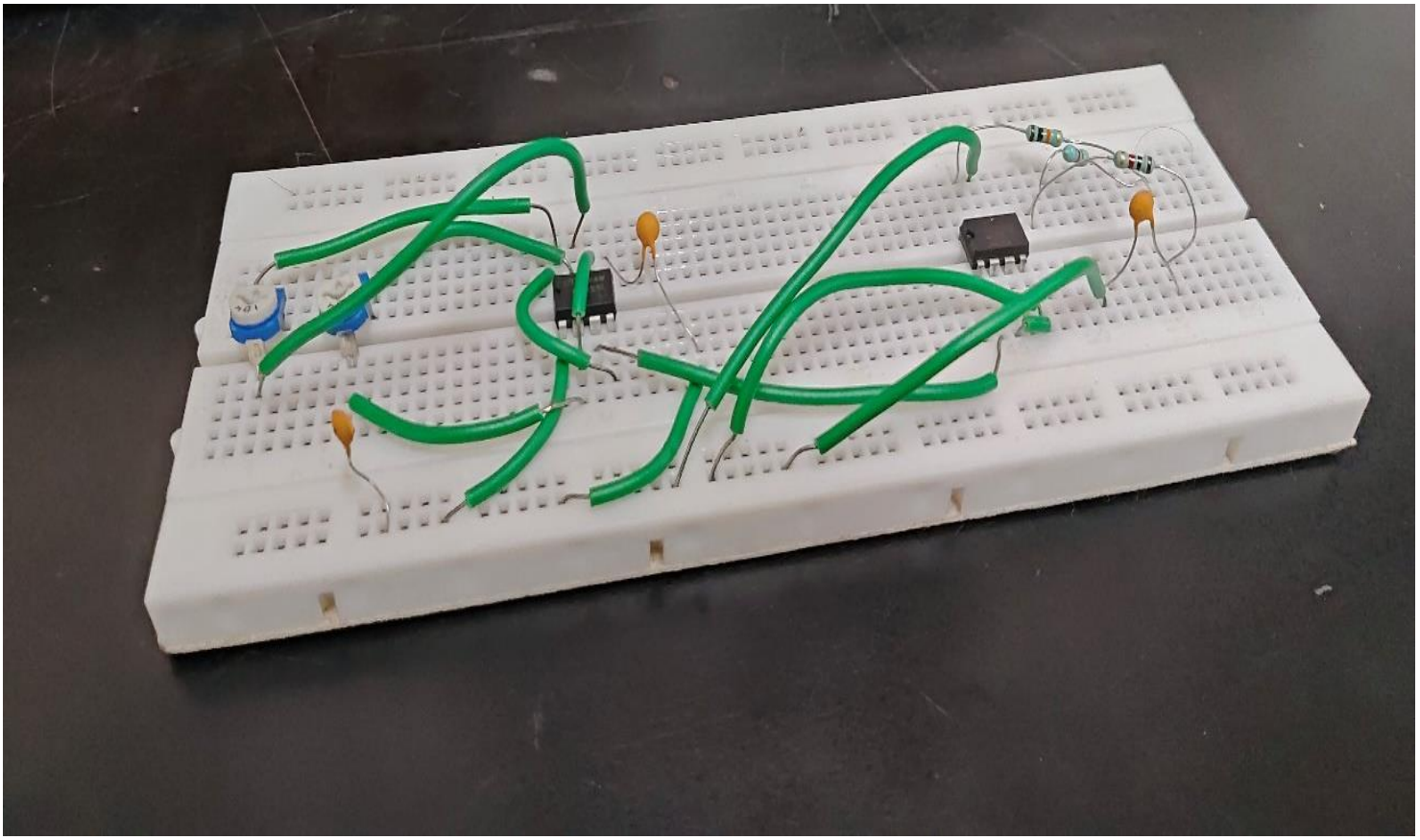


DESIGN SPECIFICATION

Sl. No	Component Name	Specification	No. of units	Price Per Unit
1.	555 Timer IC	NE555	1	10
2.	Potentiometer	100kohm	2	10
3.	Resistors	10k,4.7k,1k	3	10
4.	Capacitor	0.01uf	3	10
5.	Analog Multiplier	AD633AN	1	450
6.	Connecting Wires	23SWG	3 meter	10

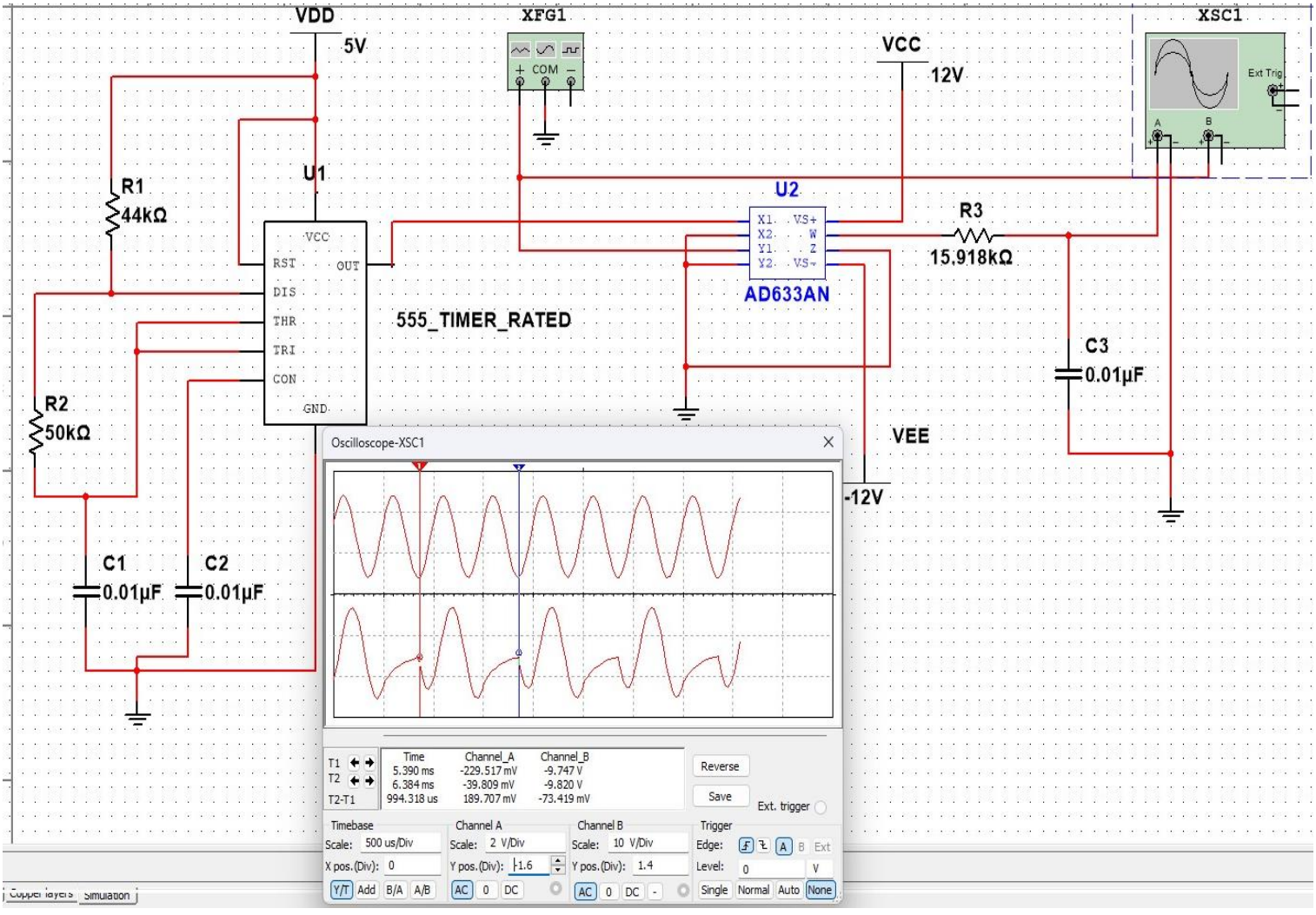
HARDWARE SETUP



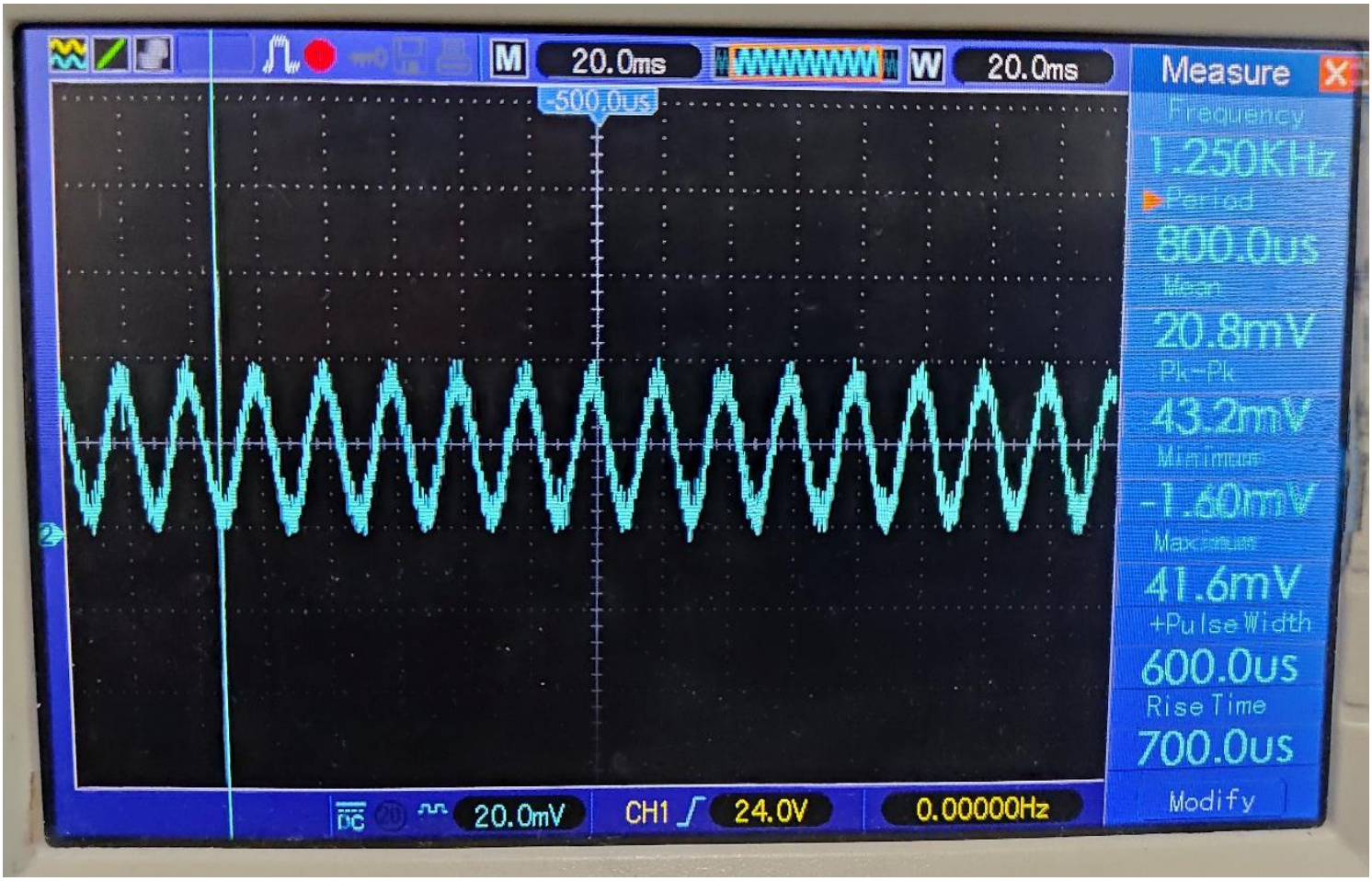


RESULT

Multisim Result:



Hardware output:



COMMENTS

In this experiment, we successfully designed and tested a circuit for frequency down-conversion from 2 kHz to 1 kHz using a combination of a 555 Timer IC, an AD633AN Analog Multiplier, and a Low-Pass Filter (LPF). The 555 Timer was utilized to generate a stable 1 kHz sine wave, while the AD633AN was used for frequency mixing, allowing us to produce both sum and difference frequencies from the 2 kHz input signal. The low-pass filter effectively isolated the desired 1 kHz frequency, demonstrating the power of simple analog circuits for frequency conversion.

This experiment provided valuable insights into the practical application of analog components such as oscillators, multipliers, and filters. We also learned the process of achieving frequency conversion through modulation techniques and the importance of filtering to eliminate unwanted frequencies. The success of the circuit confirms the reliability and versatility of these components in signal processing applications.

REFERENCE

1. https://www.wikipedia.org/
2. https://www.edaboard.com/threads/1k-to-2khz-frequency-converter.402508/
3. https://www.quora.com/How-do-I-design-a-high-frequency-inverter-to-obtain-a-frequency-of-1khz-using-either-IRFP150-or-IRFP450
4. https://www.ti.com/
5. https://eee.poriyaan.in/topic/ad633-multiplier-ic-11973/

DATA SHEET

LM555 Timer

1 Features

- Direct Replacement for SE555/NE555
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output
- Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

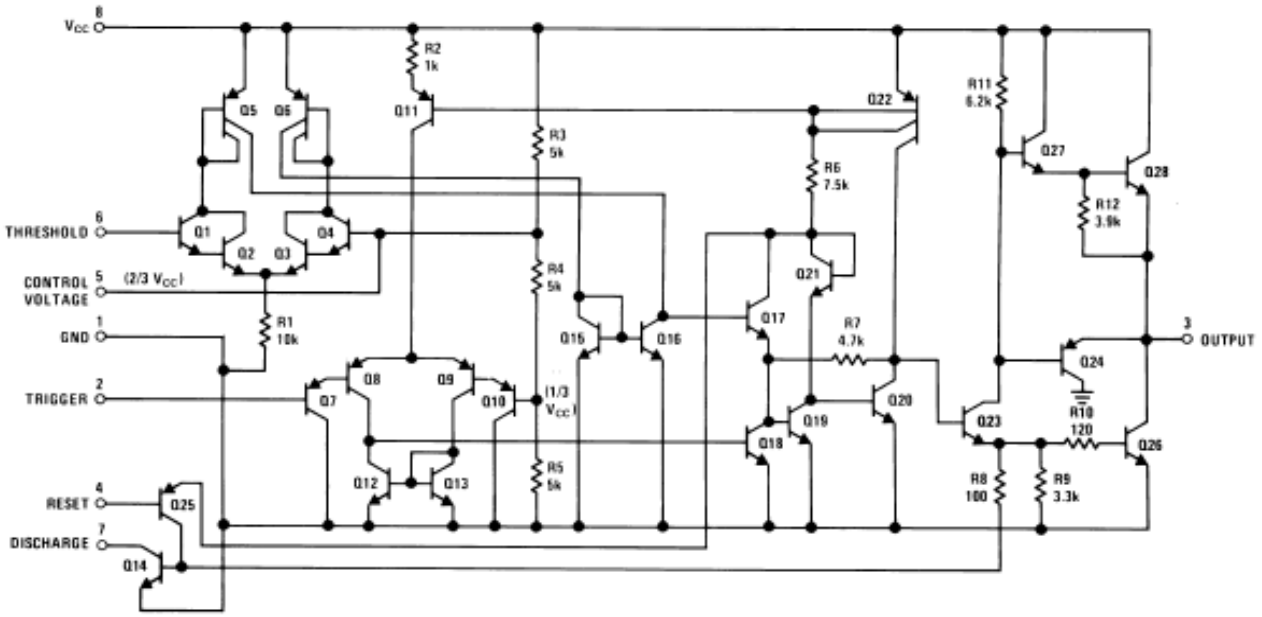
The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM555	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	VSSOP (8)	3.00 mm × 3.00 mm

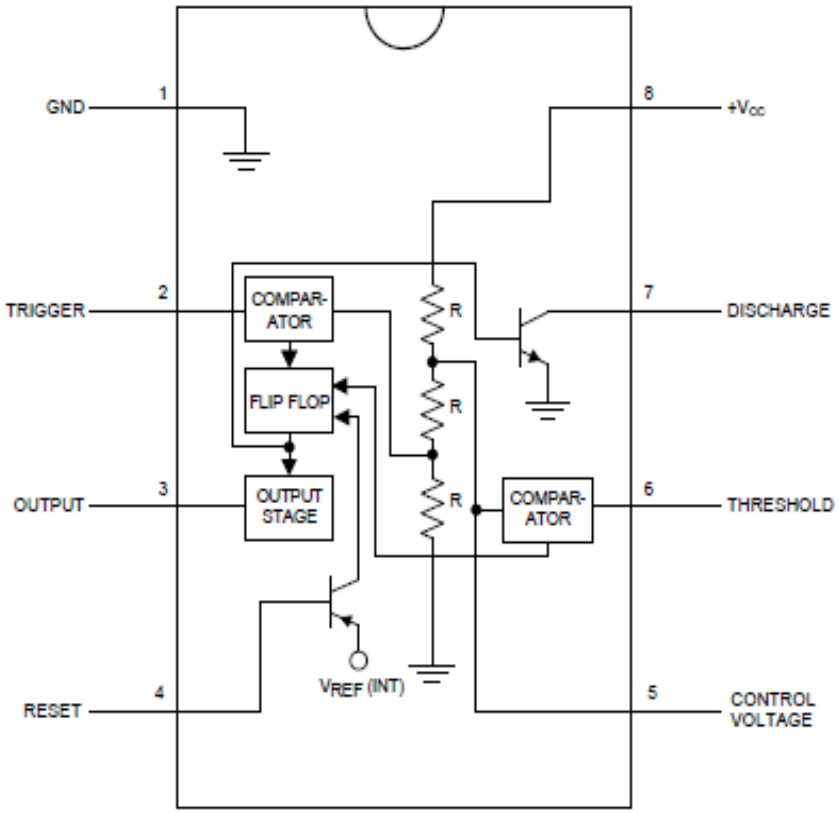
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram



5 Pin Configuration and Functions

D, P, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	Control Voltage	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform
7	Discharge	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage
1	GND	O	Ground reference voltage
3	Output	O	Output driven waveform
4	Reset	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering
6	Threshold	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop
2	Trigger	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin
8	V^+	I	Supply voltage with respect to GND

Low Cost Analog Multiplier

Data Sheet

AD633

FEATURES

4-quadrant multiplication
Low cost, 8-lead SOIC and PDIP packages
Complete—no external components required
Laser-trimmed accuracy and stability
Total error within 2% of full scale
Differential high impedance X and Y inputs
High impedance unity-gain summing input
Laser-trimmed 10 V scaling reference

APPLICATIONS

Multiplication, division, squaring
Modulation/demodulation, phase detection
Voltage-controlled amplifiers/attenuators/filters

FUNCTIONAL BLOCK DIAGRAM

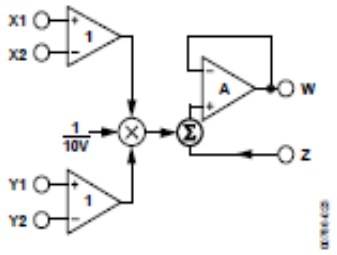


Figure 1.

GENERAL DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs, and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead PDIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 µV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/µs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The versatility of the AD633 is not compromised by its simplicity. The Z input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications. For further information, see the Multiplier Application Guide.

The AD633 is available in 8-lead PDIP and SOIC packages. It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the −40°C to +85°C industrial temperature range (A Grade).

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-lead SOIC and PDIP packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

Rev. K
Document Feedback

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

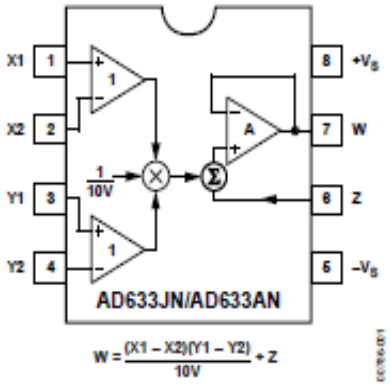

Figure 2. 8-Lead PDIP

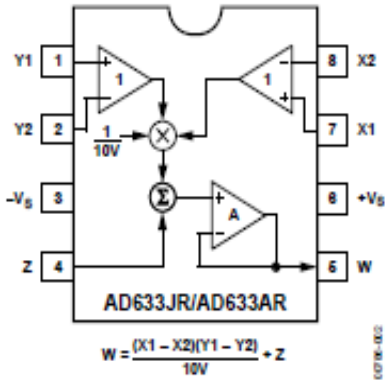

Figure 3. 8-Lead SOIC

Table 4. 8-Lead PDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	X Multiplicand Noninverting Input
2	X2	X Multiplicand Inverting Input
3	Y1	Y Multiplicand Noninverting Input
4	Y2	Y Multiplicand Inverting Input
5	$-V_S$	Negative Supply Rail
6	Z	Summing Input
7	W	Product Output
8	$+V_S$	Positive Supply Rail

Table 5. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Y Multiplicand Noninverting Input
2	Y2	Y Multiplicand Inverting Input
3	$-V_S$	Negative Supply Rail
4	Z	Summing Input
5	W	Product Output
6	$+V_S$	Positive Supply Rail
7	X1	X Multiplicand Noninverting Input
8	X2	X Multiplicand Inverting Input