JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.18, NO.5, OCTOBER, 2018 ISSN(Print) 1598-1657
https://doi.org/10.5573/JSTS.2018.18.5.602 ISSN(Online) 2233-4866

Novel XNOR-based Approximate Computing for Energy-efficient Image Processors

Sunghyun Kim and Youngmin Kim*

Abstract—**Approximate computing, which has a trade-off between accuracy and performance, has emerged as a promising solution for energy-efficient designs in error-tolerant applications. In this paper, the design of a novel approximate adder and multiplier is studied and proposed. First, a new approximate adder based on XNOR gates and a hybrid adder using them to reduce the error rate is proposed. Then, a new high-performance and energy-efficient approximate binary multiplier with acceptable error metrics is investigated. The proposed multiplier shows better error metrics than other previous approximate multipliers and significantly improvements area, delay, and power consumption by up to 20% compared to the exact binary multiplier. Finally, we apply the approximate binary multipliers to the JPEG encoder and achieve a significant reduction in the area, speed, and power consumption with a negligible quality loss of the output image. So, the proposed approximate arithmetic computing logics are suitable for high-performance and energy-efficient hardware designs.**

Index Terms—**Approximate computing, energy-efficient, XNOR-based adder, approximate multiplier, image processing, JPEG**

I. INTRODUCTION

Nowadays, electronic devices are facing rapid increases in the amount of data to be processed. In addition, since the devices are getting smaller, especially for wearable devices, a highly energy-efficient design is required. Energy efficiency is the product of power and delay. To improve energy efficiency, both power consumption and computing time must be reduced simultaneously. However, many methods for reducing power consumption have a negative effect on the performance. In other words, in order to reduce power consumption, performance (or speed) has to be decreased, and devices consume more power for higher performance.

One of the techniques to solve this problem is the approximate computing [1, 2], which can both reduce power consumption and improve performance by compromising the accuracy of the computation. Thus, the approximate computing is well suited for applications involving human senses, since a loss of accuracy that is not perceived by humans does not affect the functionality of the application. Approximate computing has a trade-off between accuracy and power consumption; hence, error metrics [3], such as an error rate and error distance, are important. In addition, the error distance is one of the metrics for the quality of the output results in image processing [4].

Many studies have been conducted on the approximate adder design, in which the trade-off between power consumption and accuracy is optimized [5-11]. In [5], a Lower-part-OR Adder (LOA) used for a bio-related circuit is proposed. LOA is an adder composed of a precise adder for the upper bits and an approximate adder (i.e., simple OR and AND logics) for the lower bits. In [6], a timing-starved adder model and a synthesis technique have been studied to optimize the trade-off between image quality and power consumption. An

Manuscript received Apr. 5, 2018; accepted Aug. 12, 2018
School of Computer & Information Engineering, Kwangwoon University, Kwangwoon-ro 20, Nowon-gu, Seoul 01897, Korea
E-mail : youngmin@kw.ac.kr

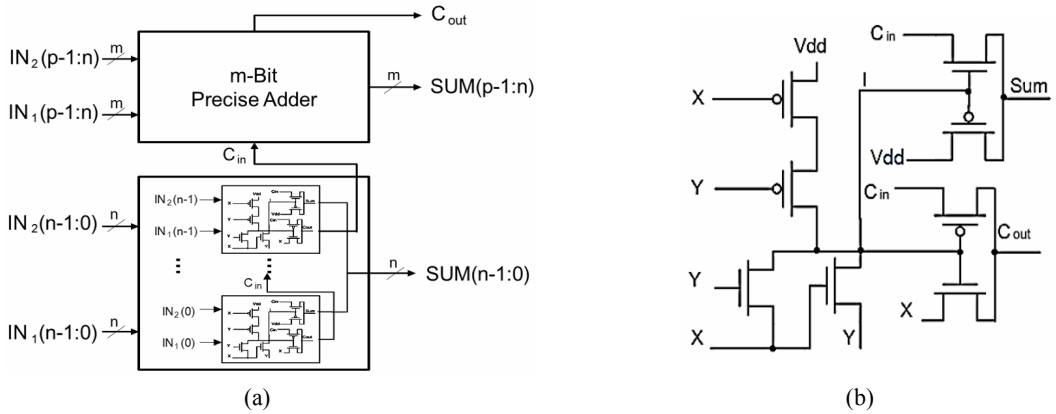

Fig. 1. (a) Hybrid adder [10], (b) Vdd-connected 1-bit Approximate XNOR-based Adder (VAXA) [10].

accuracy-configurable adder, which can adjust the accuracy of the results during runtime according to accuracy requirements, is proposed in [7]. An approximate XOR/XNOR-based Adder (AXA) is proposed to reduce the number of transistors by performing inexact computations [8]. A 1-bit full adder in the AXA is designed based on a 4-transistor XNOR gate. Thus, the number of transistors can be reduced to six, compared to 10 in the conventional accurate full adder [12]. However, four cases out of the eight input combinations can cause errors in the sum or carry-out bits because of the approximation. In [9], several approximate mirror adders are introduced to reduce the power consumption of digital signal processing (DSP) architectures (e.g., discrete cosine transform).

In addition, various studies have been conducted on multiplier design using an approximation approach [13-16]. The approximate multiplier can be designed by using either approximating internal adders or an architectural approximation of the multiplier itself. A high-performance multiplier with error-tolerance using a partial-error recovery method based on an OR gate has been proposed in [13]. This approximate multiplier improves speed by replacing the internal accurate adder with an approximate adder. In [14], an approximate multiplier structure called DRUM (Dynamic Range Unbiased Multiplier), in which the number of input bits of a multiplication operation is reduced, is introduced. The bit truncation is operated by finding the position of the first '1' from the most significant bit and discarding the remaining bits, leaving only the k-bits down from that position. More recently, the approximation by reducing the number of partial products using the OR gates has been proposed and analyzed [15].

The LOA technique is simple and provides advantage in power, area, and delay over the accurate adder. The benefit is greater when the number of bits in the approximate adder part (lower bit part) increases. However, the error rate is too high because of the simple OR-ing for the lower bits.

In this paper, Section II explains a novel structure of a 1-bit approximate adder to reduce the error rate of the LOA architecture and proposes a multi-bit adder design using it [10]. Section III presents a high-performance and energy-efficient approximate binary multiplier [16] using a Vdd-connected approximate XNOR-based adder (VAXA) [10] with simulation results for error metrics, performance, and power consumption. A design method for energy-efficient image processor applications using the proposed approximate binary multiplier is studied in Section IV. Simulation results regarding output image quality, performance, and energy-efficiency of the proposed image processor are also discussed. Finally, Section V concludes the paper.

II. NOVEL XNOR-BASED APPROXIMATED ADDER

1. Basic Structures

In this subsection, we describe the proposed hybrid adder by applying 1-bit approximate adders [10]. As shown in Fig. 1(a), the hybrid adder consists of the *m*-bits precise adder in higher bits and the *n*-bits approximate adder which is the novel XNOR-based

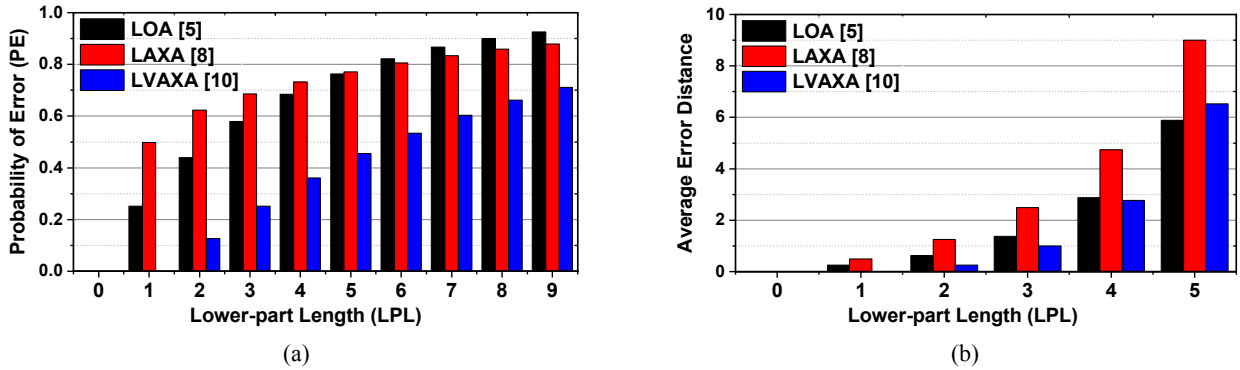

Fig. 2. (a) Comparison of error rates for LOA, LAXA, and LVAXA [10], (b) Comparison of AED for LOA, LAXA, and LVAXA [10].

adder for the lower bits. The approximation bit length (*n*-bit) is configurable for accuracy.

Fig. 1(b) shows a schematic of the Vdd-connected 1-bit approximate XNOR-based adder (VAXA) that modified the approximate XNOR-based adder 3 (AXA3) in [8]. VAXA replaces the ground (Gnd) connection to the PMOS involved in Sum of AXA3 with the Vdd to reduce the error rate and error distance (ED) [3] for a multi-bit approximate adder. An error occurs only when C_{in} is 0 and X and Y are different in the AXA3, whereas VAXA results in an error only when C_{in} is 1 and X and Y are different. Since the carry-in of the least significant bit in the multi-bit adder is always 0, no error can occur for these cases by using of the VAXA. Therefore, using the VAXA structure for a multi-bit approximate adder can reduce the error rate significantly in the approximate adder design.

2. Simulation Results

A logic-level simulation is performed using NC-Verilog in order to compare the error characteristics of the several approximate adders; LOA, Lower-part AXA3 (LAXA), and the proposed Lower-part VAXA (LVAXA). 200,000 randomly generated inputs are used in the simulation. Fig. 2(a) shows the error rate of each adder. Among the tested adders, the proposed LVAXA shows the lowest error rate for various lower-part lengths (LPL) and no error for 1-bit LPL. With the LVAXA, an error rate of less than 50% can be achieved up to LPL 5-bits. As shown in Fig. 2(b), the average error distance (AED) of the LVAXA is always smaller than that of LAXA and smaller than that of the LOA up to 4 bits. The transistor count, the probability of error (PE), and the mean error distance (MED) of a 16-bits adder when LPL is 4 bits is summarized in Table 1. Using the proposed approximate adder, the number of transistors becomes 5% smaller than in the accurate adder (ACA) [12]. Also, the PE and AED numbers are 47% and 4% smaller than the LOA-based design, respectively.

Table 1. Comparison of transistor count and error characteristics of 16-bits approximate adders (LPL = 4)

	ACA [12]	LOA [5]	LAXA [8]	LVAXA [10]
Transistor Count	160	150	152	152
Probability of Error (PE)	0	68%	73%	36%
Mean Error Distance (MED)	0	2.88	4.75	2.76

Table 2. Comparison of transistor count, power, and delay of conventional full adder and VAXA

	Conv. full adder	VAXA [10]	Savings
Transistor Count	28	8	71.4%
Power (μW)	1.964	1.184	39.7%
Delay (ps)	64.63	30.82	52.3%

A transistor-level simulation is performed using HSPICE in order to more accurately evaluate area, delay, and power consumption of the VAXA-based adder. Simulation is conducted by exploiting of the 45-nm Nangate cell libraries [17]. Table 2 summarizes the area, performance, and power of the conventional full adder and the VAXA. As shown, 71.4% of the area, 39.7% of the power, and 52.3% of the delay can be saved in the proposed VAXA compared to the conventional full adder.

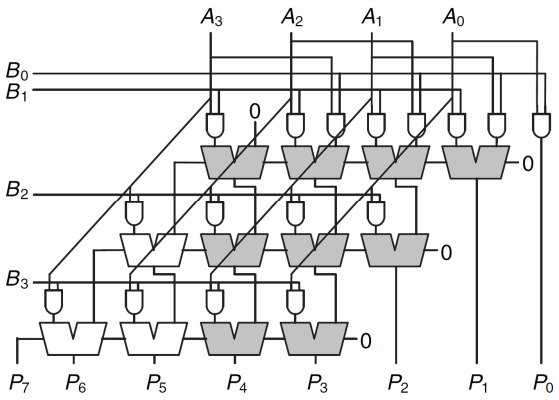

Fig. 3. 4×4 approximate binary multiplier with LPL of 5 bits (The full adders in gray represent the VAXA) [16].

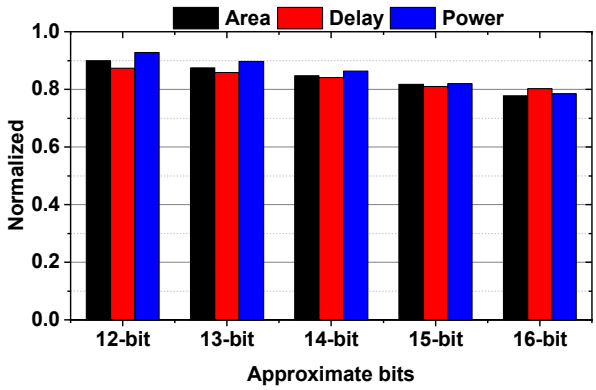

Fig. 4. Normalized graph of area, delay, and power of the proposed multiplier as the LPL increases.

Table 3. The error metrics of the proposed approximate multiplier for various LPL bits

lower-part length (LPL)	MRED (%)	NMED (%)	Max RED
12-bits	0.0131	0.0002	0.9952
13-bits	0.0275	0.0005	0.9952
14-bits	0.0562	0.0011	1.0297
15-bits	0.1109	0.0026	1.4570
16-bits	0.2133	0.0058	1.4570

III. Approximate Multiplier

1. Basic Structure

The conventional binary multiplier consists of the AND gates and full adders, which makes the partial products and calculates the sum of the partial products, respectively [18]. The N×M multiplier has two input bits for a multiplicand and a multiplier. It generates M partial products of N-bits, and the final result becomes N+M bits. We propose an approximate multiplier, in which the full adders of some lower bits (lower part) are replaced with the VAXA explained in the previous section [16]. Fig. 3 shows the structure of a 4×4 approximated binary multiplier with a lower-part length (LPL) of 5 bits. A and B are 4-bits inputs, and P is 8-bits output. The full adder blocks filled with gray represent the VAXA.

2. Simulation Results

The simulation for various error metrics is performed using an NC-Verilog tool, and the design is synthesized using the 45-nm Nangate library in Design Compiler.

Table 4. Error rate and MED comparison of various 5-bit approximate multipliers

	Using LOA	Using LAXA	Using proposed LVAXA
Probability of Error (PE)	58.9%	93.5%	33.1%
Mean Error Distance (MED)	15.4	68.3	12.2

The multiplier is fixed to calculate a 16×16 multiplication, and simulation is conducted with one million random inputs for verification of the various error metrics, such as mean relative error distance (MRED) and normalized mean error distance (NMED) [3].

Table 3 summarizes the error metrics for the proposed approximate binary multiplier as the LPL (or approximation) bit increases. As shown, the MRED and NMED values are doubled for each 1-bit LPL increment with a slight increase in the maximum RED value. Fig. 4 shows the normalized area, delay, and power savings of the proposed approximate multiplier compared to the accurate binary multiplier. As expected, area, delay, and power saving are improved as the LPL bit increases, because the circuit becomes simpler and faster for more bit approximation. For example, when LPL is 15 bits out of a total 32 bits, approximately 20% of the area, delay, and power are reduced compared to the conventional multiplier. PE and MED values are compared in Table 4 for various approximate adders when the LPL is 5 bits. As shown, the proposed approximate multiplier shows better results than other approximate multipliers.

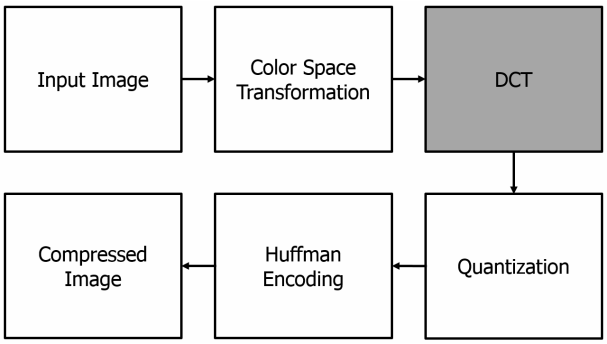

Fig. 5. General process of a JPEG encoder.

IV. Energy-efficient Image Processor

To validate the benefit of the energy consumption of the proposed approximate adder and multiplier in a real-world application, we design an approximate JPEG encoder by using the proposed modules. Image quality and basic design metrics (i.e., area, delay, power, and energy) are analyzed and compared between a general JPEG encoder (i.e., using accurate adders and multipliers) and the approximate JPEG encoder. The JPEG encoder is designed using Verilog and synthesized by using the 45-nm Nangate open cell library in Design Compiler for performance measurement.

Fig. 5 shows the general process of the JPEG encoder. The discrete cosine transform (DCT) block filled with gray is selected for approximation calculation because accurate values are not important and there are many multiplications and additions. The input image enters as an uncompressed image file (e.g., TIF format). Color Space Transformation converts RGB (red, green, blue) values into corresponding luminance and chrominance (Y, Cb, Cr) values by multiplication of a fixed decimal point. The next step is to perform DCT, in which the image is divided into 8×8 blocks. The DCT formula for Y value is defined as DY = T × Y × inv(T), where T is a DCT matrix, Y is a matrix of Y values for the 8×8 image block, inv(T) means an inversion of the T matrix, and DY is a result matrix after the DCT operation. The separate DCT for Cb and Cr should be calculated as well. Then, quantization, followed by the Huffman encoding is performed for each of the Y, Cb, and Cr results. Finally, the Y, Cb, and Cr Huffman codes are combined for each 8×8 block of the image and inserted into the bit stream to produce an output of the compressed image.

(a) (b)

Fig. 6. Compressed images of the JPEG encoders (a) using accurate multipliers (the reference image), (b) using approximate multipliers (LPL = 15 bits). Note, the PSNR of image (b) is 32.98 dB.

Table 5. The design characteristics of the JPEG encoders after synthesis

	Using accurate multiplier	Using LOA [5] multiplier	Using approx. multiplier	Saving w.r.t. accurate multiplier	Saving w.r.t. LOA multiplier
Area (μm^2)	192,070	183,826	162,702	15.3%	11.5%
Delay (ns)	7.45	7.31	5.88	21.1%	19.6%
Power (mW)	7.22	7.11	6.93	4.1%	2.5%
Energy (pJ)	53.79	52.00	40.75	24.2%	21.6%

Fig. 6 shows the compressed images using JPEG encoders; by the accurate multiplier (a) and the proposed approximate multiplier of 15-bit LPL (b). The relative power signal noise ratio (PSNR) of the proposed approximate JPEG encoder with respect to the image after accurate JPEG encoder is 32.98 dB. As shown in the resulting images and the PSNR number [15], the penalty by the reasonable reduction in accuracy using of the proposed approximate multiplier is negligible. Table 5 summarizes the design characteristics after synthesis of the JPEG encoders using accurate multipliers, LOA [5] multipliers, and the proposed approximate multipliers. As shown, 15.3% of the area, 21.1% of the delay, and 4% of the power are saved compared to accurate multipliers when we apply the approximation in the only DCT calculation. Moreover, up to 24.2% of the energy can be reduced because of the faster calculation with less power by the approximated JPEG encoder. In addition, our proposed approximate multiplier-based JPEG encoder offers a reasonable benefit over the LOA-based JPEG encoder in all design characteristics.

V. CONCLUSIONS

In this study, we propose a novel approximate adder structure and investigate design characteristics, such as power, delay, and area, and error metrics, such as error rate and error distance. The proposed VAXA adder can achieve more than a 40% improvement in power consumption, 71% in transistor count, and 52% in speed-up compared to the conventional full adder. An approximate binary multiplier is also proposed by adopting the VAXA in the lower bits, which provides more than a 20% improvement in power, area, and delay over the conventional one for a half bits approximation.

A design for the image processing application using the proposed approximate multipliers is conducted to validate the proposed approximate blocks. The approximate JPEG encoder has a significant benefit in area, delay, power, and energy values compared to the accurate one with negligible loss in the image quality. Therefore, the proposed approximate adders and multipliers can be applied to energy-efficient hardware designs for mobile and embedded environments, in which some well-controlled errors are acceptable.

ACKNOWLEDGMENTS

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2017R1D1A1B03028065). This work was supported in part by the Research Grant of Kwangwoon University in 2018. EDA tools were partially supported by IDEC at KAIST.

REFERENCES

[1] J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," *European Test Symp.* pp. 1-6, 2013.

[2] Q. Xu, T. Mytkowicz, and N. S. Kim, "Approximate Computing: A Survey," *IEEE Design & Test,* vol. 33, no. 1, pp. 8-22, 2016.

[3] J. Liang, et al., "New metrics for the reliability of approximate and probabilistic adders," *IEEE Transactions on Computers*, vol. 62, no. 9, pp. 1760-1771, 2013.

[4] I. S. Chong, et al., "New quality metric for multimedia compression using faulty hardware," *International Workshop on Video Processing and Quality Metrics for Consumer Electronics*, pp. 267-272, Jan. 2006.

[5] H. R. Mahdiani, et al., "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," *IEEE Transactions on Circuits and Systems I*, vol. 57, no. 4, pp. 850-862, 2010.

[6] J. Miao, et al. "Modeling and synthesis of quality-energy optimal approximate adders," *International Conference on Computer-Aided Design (ICCAD)*, pp. 728-735, Nov. 2012.

[7] A. B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," *Design Automation Conference (DAC)*, pp. 820-825, June 2012.

[8] Z. Yang, et al., "Approximate xor/xnor-based adders for inexact computing," *IEEE International Conference on Nanotechnology*, pp. 690-693, Aug. 2013.

[9] V. Gupta, et al., "Low-power digital signal processing using approximate adders," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1, pp. 124-137, 2013.

[10] S. Kim and Y. Kim, "Energy-Efficient Hybrid Adder Design by Using Inexact Lower Bits Adder," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 355-357, Oct. 2016.

[11] S. Kim and Y. Kim, "Adaptive Approximate Adder (A3) to Reduce Error Distance for Image Processor," *IEEE International Conference on SoC Design (ISOCC)*, pp. 295-296, Oct. 2016.

[12] J. F. Lin, et al., "A novel high-speed and energy efficient 10-transistor full adder design," *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 5, pp. 1050-1059, 2007.

[13] C. Liu, et al., "A low-power, high-performance approximate multiplier with configurable partial error recovery," *IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 1-4, Mar. 2014.

[14] S. Hashemi, et al.:"DRUM: a dynamic range unbiased multiplier for approximate applications,"

IEEE/ACM ICCAD (2015) 418–425.

[15] I. Qiqieh, et al., "Energy-efficient approximate multiplier design using bit significance-driven logic compression," *IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE),* pp. 7-12, Mar. 2017.

[16] S. Kim and Y. Kim: "High-Performance and Energy-Efficient Approximate Multiplier for Error-Tolerant Applications," *IEEE International Conference on SoC Design (ISOCC)*, pp. 278-279, Oct. 2017.

[17] Nangate: 45nm Open Cell Library http:/www.nangate.com.

[18] D. M. Harris and S. L.Harris, "Digital Design and Computer Architecture," 2nd ed., pp. 252–253, *Elsevier*, 2013.

Sunghyun Kim received B.S. and M.S. degree in computer engineering from Kwangwoon University, Seoul, Korea, in 2016 and 2018, respectively. His research interests include SoC designs, CAD, embedded system designs, and low-power SoC designs.

Youngmin Kim received the B.S. degree in electrical engineering from the Yonsei University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the university of Michigan, Ann Arbor, in 2003 and 2007, respectively. He has held a senior engineer position in the Qualcomm, San Diego, CA. He is currently an Associate Professor in Kwangwoon University, Seoul, South Korea. Prior to joining Kwangwoon University, he was with the school of electrical and computer engineering at the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea. His research interests include embedded systems, variability-aware design methodologies, design for manufacturability, and design and technology co-optimization methodologies, and low-power and 3D IC designs.