DIGITAL LOGIC DESIGN LAB (EET1211)

LAB I: Introduction to different ICs and examine the operation of logic gates

Siksha 'O' Anusandhan (Deemed to be University), Bhubaneswar

Branch: CSE	Section: 2341211	Subgroup No.: 07
Name	**Registration No.**	**Signature**
Suryamadhab Moharana	2341013398	Suryamadhab Moharana

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE:-

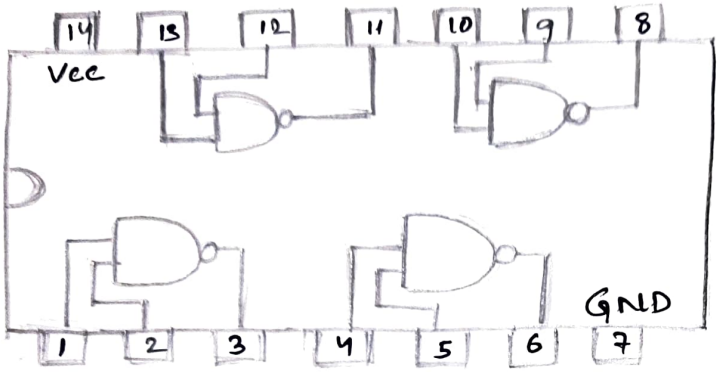
1. Investigation of the logic gates ~~of~~ behaviour of various gates.
   a) 7400 quadruple two-input NAND gate.
   b) 7402 quadruple two-input NOR gate.
   c) 7404 hex inverters.
   d) 7408 quadruple two-input ~~AND~~ AND gate.
   e) 7432 quadruple two-input OR gate
   f) 7486 quadruple two-input XOR gate.

2. Using a single 7400 IC, connect a circuit ~~that~~ produces
   a) An inverter
   b) A two-input AND
   c) A two-input OR
   d) A two-input XOR

II. PRE-LAB :-

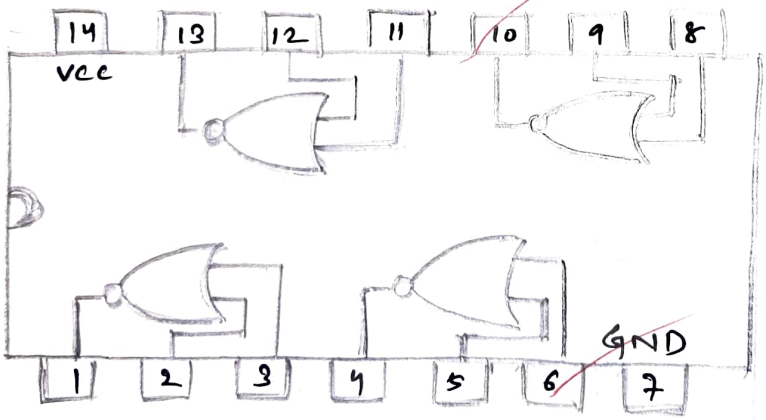
1. Logic behaviours of Logic gates.

a. Quad two-input NAND gate.



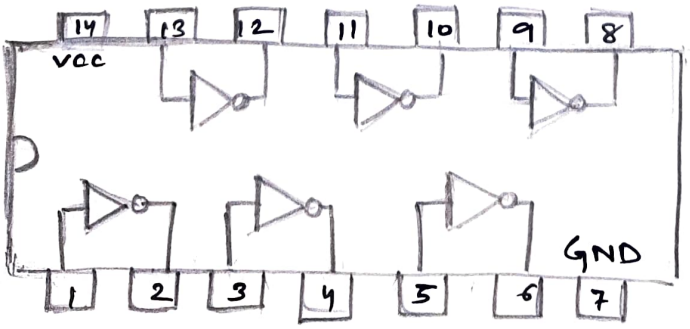
A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

b) Quad two-input NOR gate



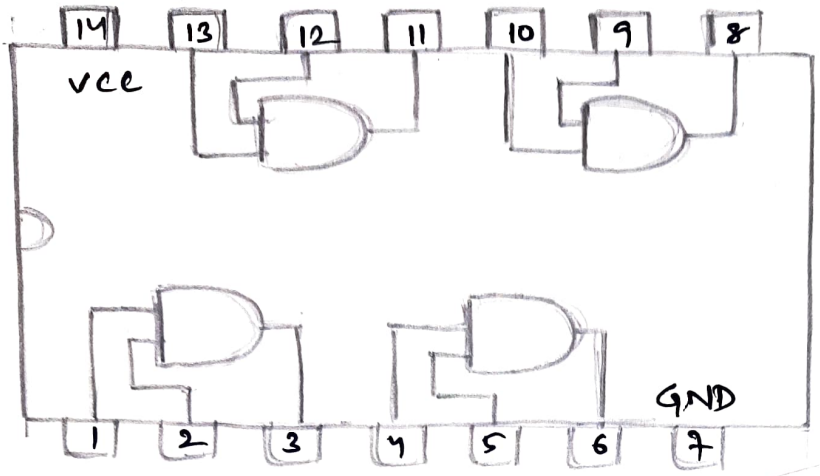
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

c) Hex inverters :-



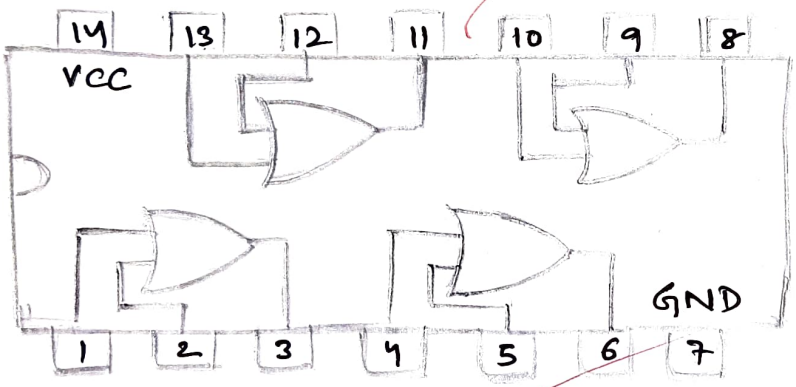
A	F
0	1
1	0

d) Quad two-input AND gate:



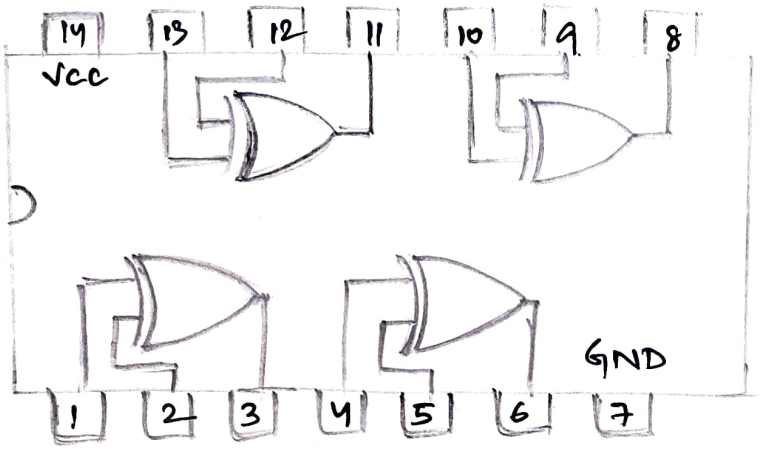
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

e) Quad two-input OR gate:



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

f) Quad two-input XOR gate:

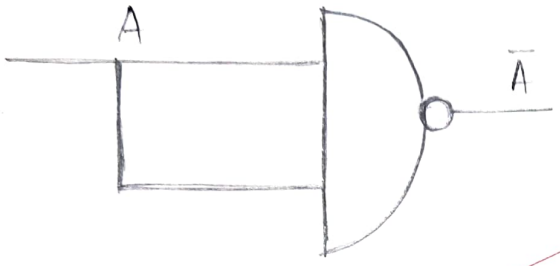


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

II. PRE - LAB :-

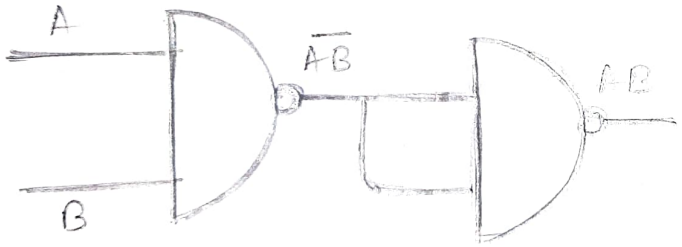
2. Draw the circuit diagram and obtain truth table for objective 2.

a) An inverter using 7400 IC.



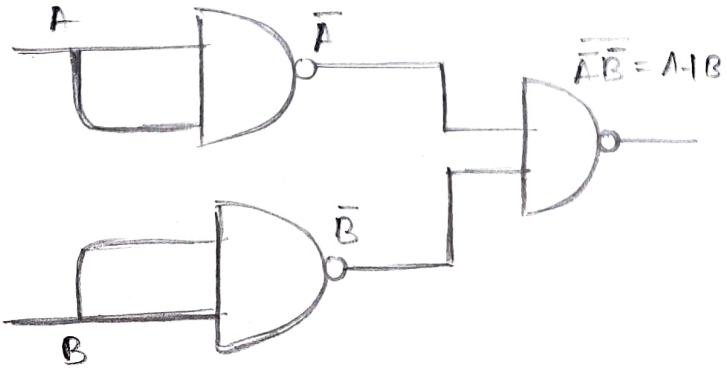
A	F
0	1
1	0

b) A two-input AND using single 7400 IC.



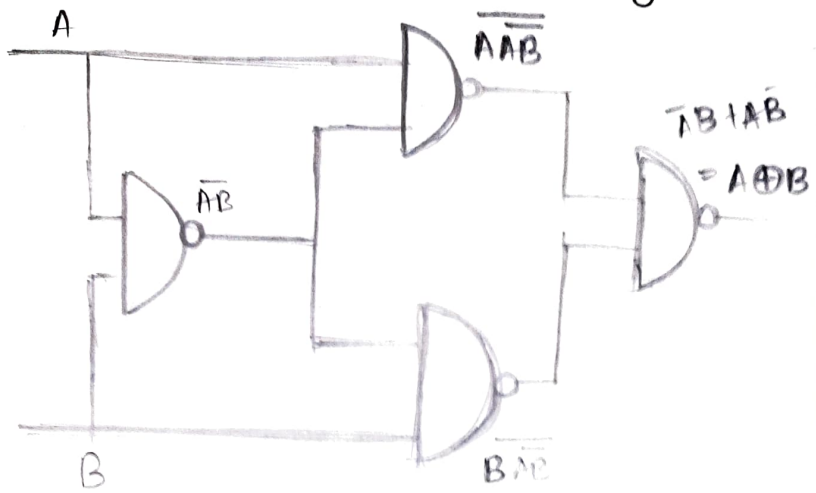
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

c) A two input OR using single 7400 IC.



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

d) A two-input XOR using 7400 IC.



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

III LAB :-

Components Required :-

Sl.no	Name of the Component	Specification	Qty.
1	Universal Trainer Kit	Microlab II	1
2	Quad two input-NAND gate	IC7400	1
3	Quad two-input NOR gate	IC7402	1
4	Quad two-input NOT gate	IC7404	1
5	Quad two-input AND gate	IC7408	1
6	Quad two-input OR gate.	IC7432	1
7	Quad two input XOR gate	IC7486	1
8	Connecting wire	23 swg	As per requirement

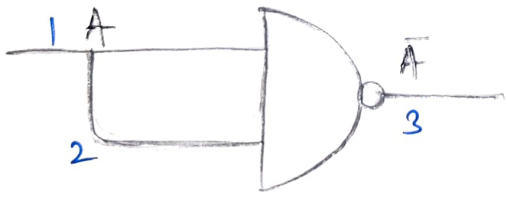
Observation :-

Objective 1 :-

Sl. no.	IC	Pin No.		Status
		I/P	O/P	
1	7400	1, 2	3	Working
2	7402	2, 3	1	Working
3	7404	1	2	Working
4.	7408	13, 12	11	Working
5	7432	4, 5	6	Working
6.	7486	10, 9	8	working

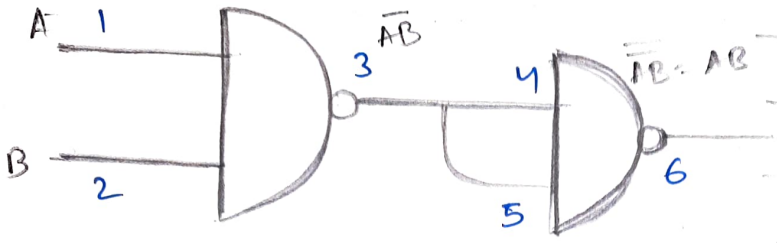
Objective-2 :-

a) An inverter using single 7400 IC.



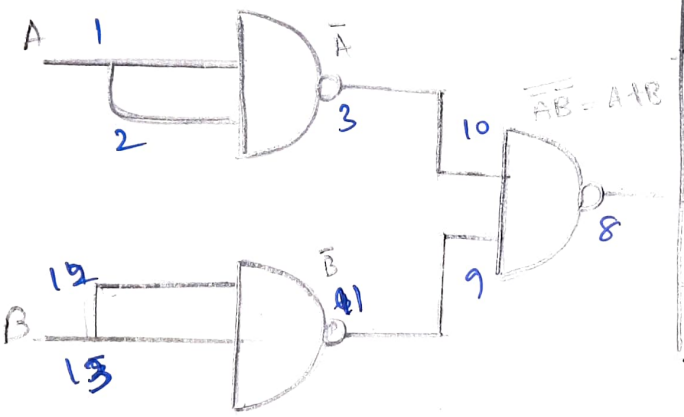
A	F
0	1
1	0

b) A two input AND gate using single 7400IC.



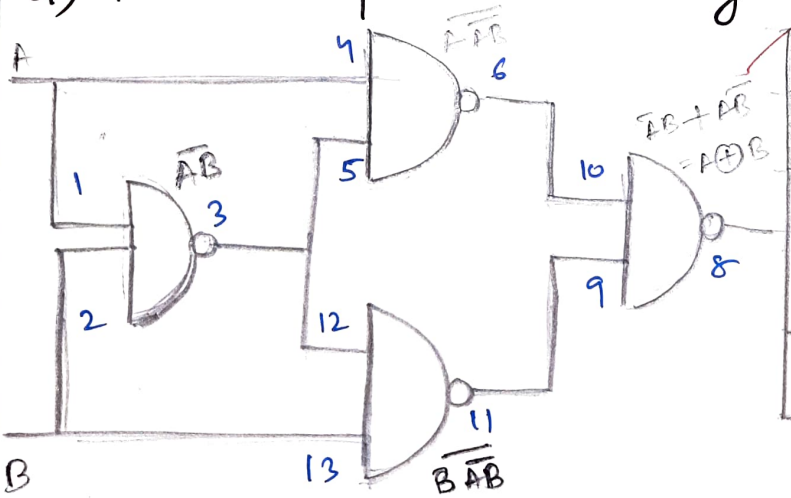
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

c) A two input OR using 7400IC.



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

d) A two input XOR using 7400IC.



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

IV CONCLUSION:-

1. In objective 1, we have concluded that all the pins at the provided ICs are working properly and showing the proper output.
2. In objective 2; we have concluded that NAND gate is an universal gate because using it, we can construct AND gate, NOT gate, OR gate, and XOR gate.
3. Also, we have concluded ~~that~~ by analyzing their working and found out their respective truth table.

V. POST LAB :-

1. What is the voltage range for operation of digital circuits ?

Ans. is the voltage range for operation of digital circuits.

2. What is the significance of ground and Vcc connection ?

Ans. Ground is connected to 0V, connected at pin No. 7, used to establish a

common reference point for all voltage measurement.

V_{cc} is connected to 5 V at pin no. 14 which provides voltage to the circuit.

∴ V_{cc} is higher wrt. ground, it may be +ve or -ve.

3. Which gates are known as universal gates and why ?

Ans. NAND gate and NOR gates are called universal gates because by using these, we can form / construct all other gates.