External Project Report on Digital Logic Design (EET1211)

DESIGN A 32X1 MULTIPLEXER USING 8X1 MULTIPLEXER AND 4X1 MULTIPLEXER

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Declaration

We, the undersigned students of B. Tech. of **(CSE)** Department hereby declare that we own the full responsibility for the information, results etc. provided in this PROJECT titled "**DESIGN A 32X1 MULTIPLEXER USING 8X1 MULTIPLEXER AND 4X1 MULTIPLEXER**" submitted to **Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar** for the partial fulfillment of the subject **Digital Logic Design (EET 1211)**. We have taken care in all respect to honor the intellectual property right and have acknowledged the contribution of others for using them in academic purpose and further declare that in case of any violation of intellectual property right or copyright we, as the candidate(s), will be fully responsible for the same.

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Abstract

This project presents the design and simulation of a 32x1 multiplexer using 8x1 and 4x1 multiplexers in a software environment. The proposed design utilizes four 8x1 multiplexers to select one out of 32 input signals, which are then fed into a 4x1 multiplexer to produce the final output. The design is simulated using a digital logic simulator, and the functionality is verified through simulation results. The proposed design demonstrates a cost-effective and efficient approach to implementing a 32x1 multiplexer, making it suitable for various digital circuit applications. The project showcases the potential of using smaller multiplexers to implement larger ones.

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1. INTRODUCTION

*MULTIPLEXER:

A multiplexer is a device that selects one of several input signals and forwards the selected signal to a single output line.

A multiplexer receives multiple input signals, each representing a different data source. The multiplexer receives selection inputs, which determine which input signal to select and forward to the output. The selected input signal is forwarded to the output line.

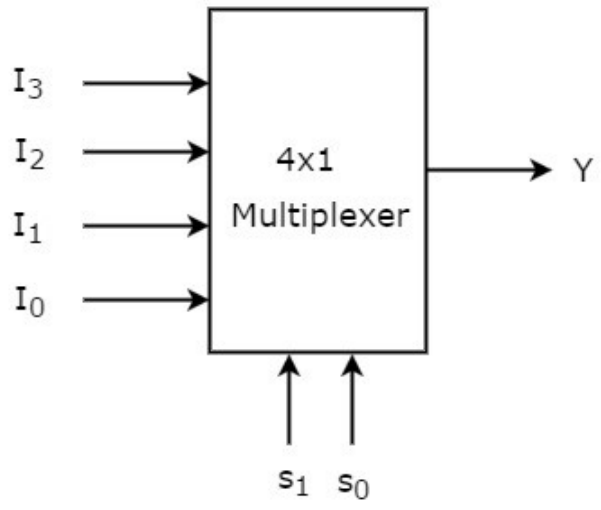
No. of input line=2^n

No. of select lines=n

No. of output=1

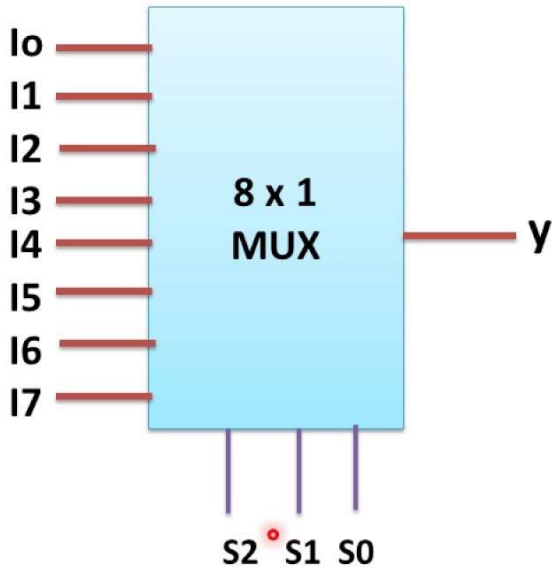
*4X1 MULTIPLEXER:

It has four input line, typically labeled as I0, I1, I2, I3 with two select lines labeled as S0, S1 and one output line labeled as Y.



*8X1 MULTIPLEXER:

It has 8 input lines, labeled as I0, I1,…,I7 and 3 select lines, labeled as S0, S1, S2 and one output Y.



*32x1 MULTIPLEXER:

It has 32 no, of inputs lines, with 5 select lines and one output Y.

2. Problem Statement

I) Explanation of problem and identification of input and output variables.
II) Highlighting the constraints.

EXPLANATION:

In this problem, we are using 32 input lines and four 8×1 multiplexers (MUX), each controlled by three select lines named S2, S1, and S0. Each 8×1 MUX processes 8 input lines and provides an output. These outputs are then passed as inputs to a 4×1 MUX, which is controlled by two additional select lines, S3 and S4. Finally, the 4×1 MUX produces the overall output, Y.

Input: I0, I1, I2, ..., I31.

Output: The output depends on the select lines S0, S1, S2, S3, and S4.

CONSTRAINTS:

- **The Boolean expression for the output must be derived using K-map, or other methods and then simplified using Boolean algebra theorems to get the output.**
- **Use four 8x1 multiplexers to create a 32x1 multiplexer.**
- **Use the 4x1 multiplexer to select one of the 4 outputs from the 8x1 multiplexers.**
- **Use the 5 select lines (S4-S0) to control the multiplexers.**
- **The functionality of the circuit must be verified by testing with different input values and checking the output.**

3. Methodology

I) Generating the solution to the problem by the use of Truth table/excitation table, K- map and (or) Boolean algebra.

II) Finding out the different digital ICs to be used in the optimized design.

S4	S3	S2	S1	S0	Y
0	0	0	0	0	I0
0	0	0	0	1	I1
0	0	0	1	0	I2
0	0	0	1	1	I3
0	0	1	0	0	I4
0	0	1	0	1	I5
0	0	1	1	0	I6
0	0	1	1	1	I7
0	1	0	0	0	I8
0	1	0	0	1	I9
0	1	0	1	0	I10
0	1	0	1	1	I11
0	1	1	0	0	I12
0	1	1	0	1	I13
0	1	1	1	0	I14
0	1	1	1	1	I15
1	0	0	0	0	I16
1	0	0	0	1	I17
1	0	0	1	0	I18
1	0	0	1	1	I19
1	0	1	0	0	I20
1	0	1	0	1	I21
1	0	1	1	0	I22
1	0	1	1	1	I23
1	1	0	0	0	I24
1	1	0	0	1	I25
1	1	0	1	0	I26
1	1	0	1	1	I27
1	1	1	0	0	I28
1	1	1	0	1	I29
1	1	1	1	0	I30
1	1	1	1	1	I31

BOOLEAN EXPRESSION:

Y = (S4′S3′S2′S1′S0′)I0 + (S4′S3′S2′S1′S0)I1 + (S4′S3′S2′S1S0′)I2 + (S4′S3′S2′S1S0)I3 + (S4′S3′S2S1′S0′)I4 + (S4′S3′S2S1′S0)I5 + (S4′S3′S2S1S0′)I6 + (S4′S3′S2S1S0)I7 + (S4′S3S2′S1′S0′)I8 + (S4′S3S2′S1′S0)I9 + (S4′S3S2′S1S0′)I10 + (S4′S3S2′S1S0)I1 + (S4′S3S2S1′S0′)I12 + (S4′S3S2S1′S0)I13 + (S4′S3S2S1S0′)I14 + (S4′S3S2S1S0)I15 + (S4S3′S2′S1′S0′)I16 + (S4S3′S2′S1′S0)I17 + (S4S3′S2′S1S0′)I18 + (S4S3′S2′S1S0)I19 + (S4S3′S2S1′S0′)I20 +(S4S3′S2S1′S0)I21 + (S4S3′S2S1S0′)I22 + (S4S3′S2S1S0)I23 + (S4S3S2′S1′S0′)I24 + (S4S3S2′S1′S0)I25 + (S4S3S2′S1S0′)I26 + (S4S3S2′S1S0)I27 + (S4S3S2S1′S0′)I28 + (S4S3S2S1′S0)I29 + (S4S3S2S1S0′)I30 + (S4S3S2S1S0)I31

DIFFERENT IC’s USED:

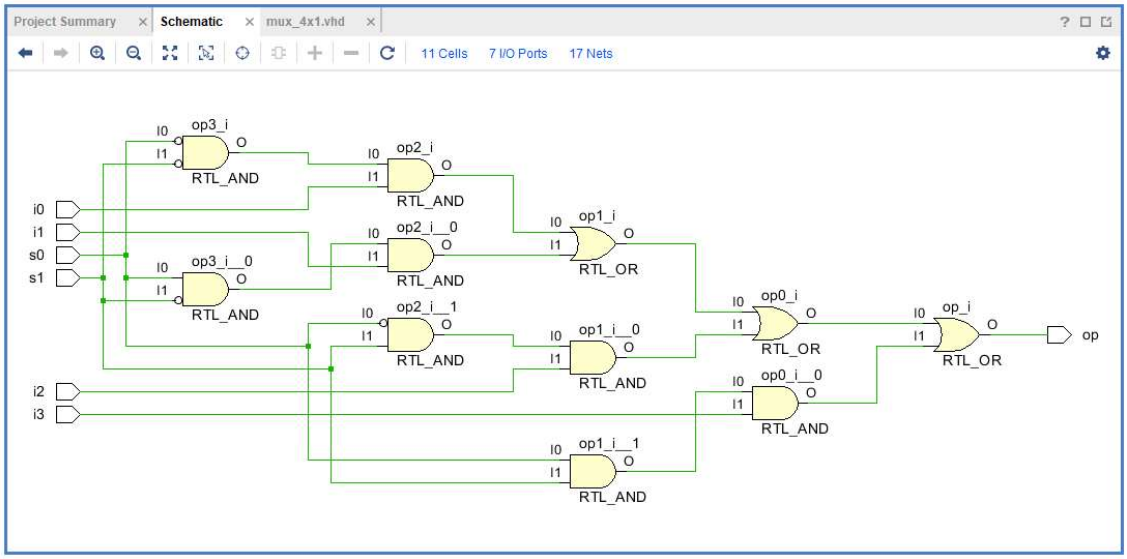
- **74HC151 8-INPUT 8X1 MUX**
- **74HC153 4-INPUT 4X1 MUX**

4. Implementation

I) **Drawing the logic diagram using different logic gates.**

II) **Program**

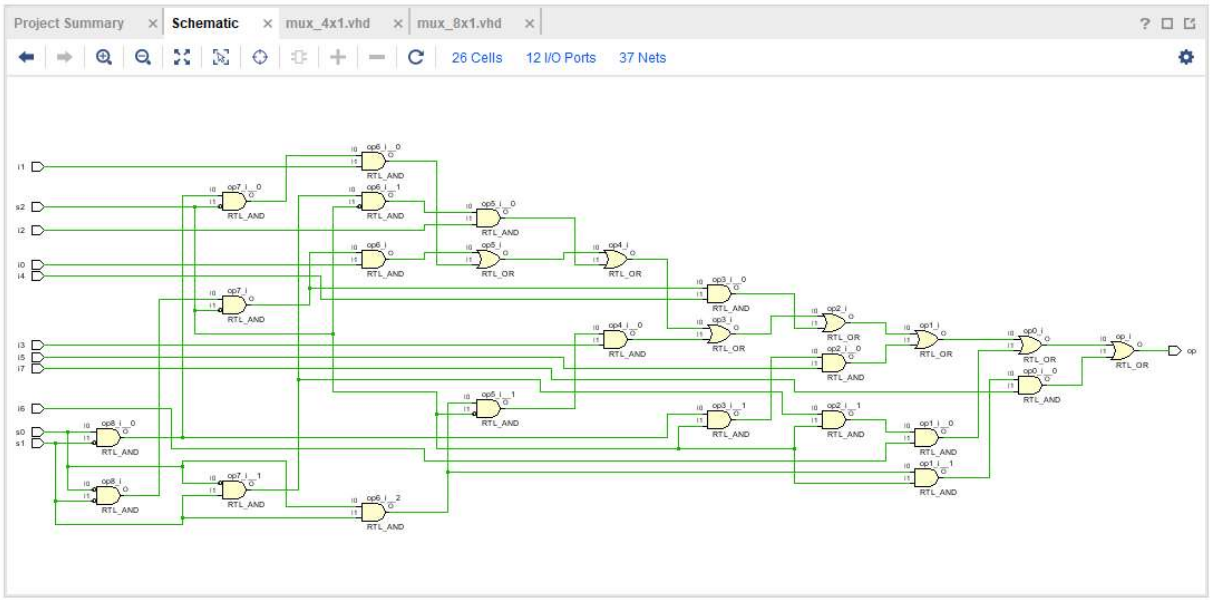
FOR 4X1 MUX:



Source Code for 4x1 Multiplexer

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux_4x1 is
   Port ( i0,i1,i2,i3 : in STD_LOGIC;
          s0,s1 : in STD_LOGIC;
          op : out STD_LOGIC);
end mux_4x1;

architecture dataflow of mux_4x1 is

begin
op<=(not s0 and not s1 and i0) or (s0 and not s1 and i1) or (not s0 and  s1 and
i2) or (s0 and s1 and i3);
end dataflow;
```

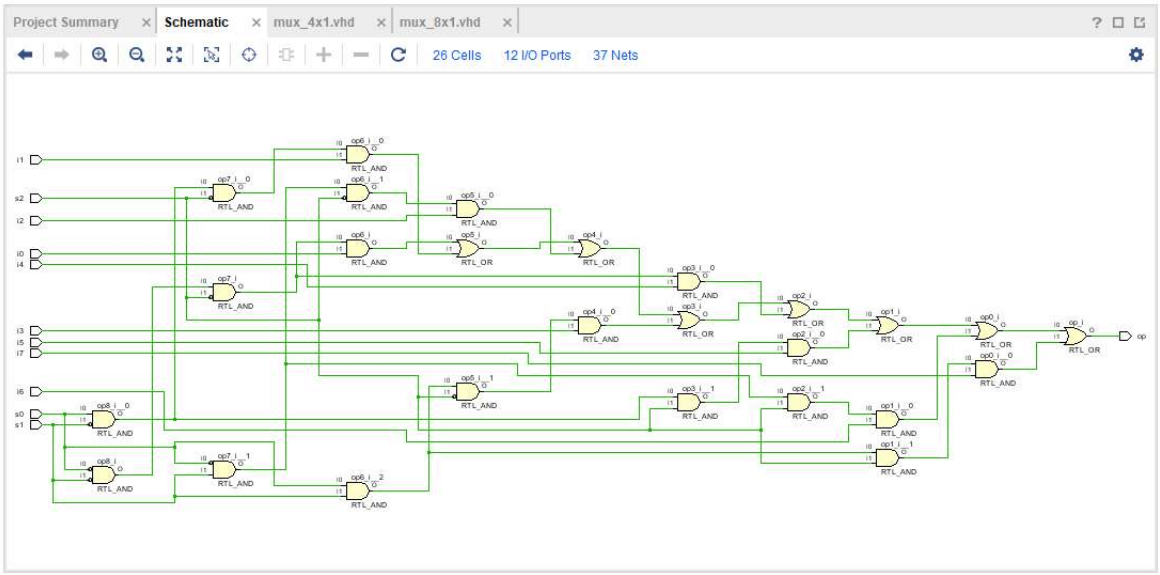
FOR 8X1 MUX:



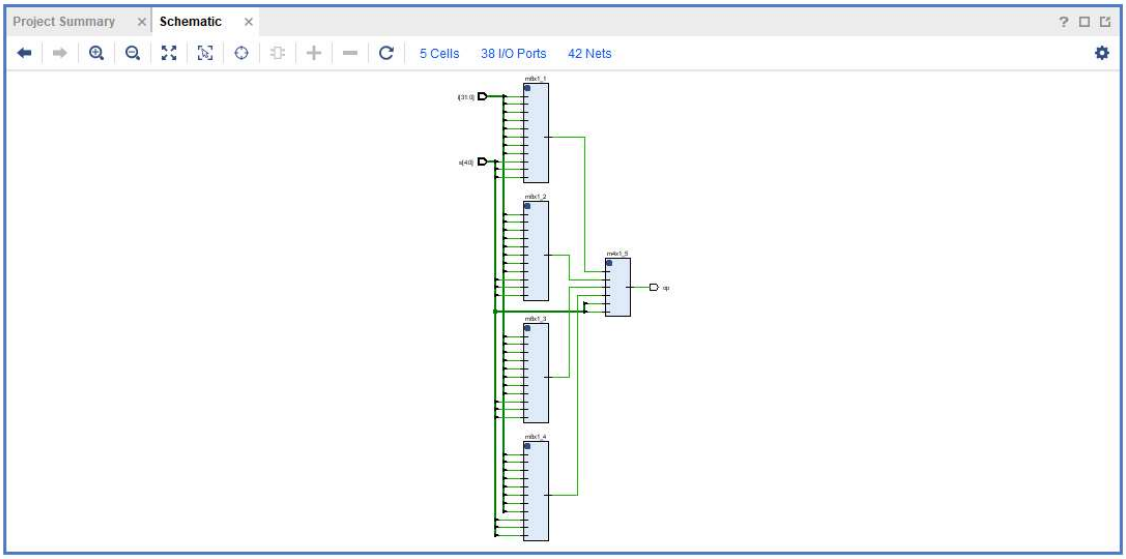
Source Code for 8x1 Multiplexer

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity mux_8x1 is
 Port ( i0,i1,i2,i3,i4,i5,i6,i7 : in STD_LOGIC;
        s0,s1,s2 : in STD_LOGIC;
        op : out STD_LOGIC);
end mux_8x1;

architecture dataflow of mux_8x1 is

begin
op<=(not s0 and not s1 and not s2 and i0) or (s0 and not s1 and not s2 and i1)
or (not s0 and s1 and not s2 and i2) or (s0 and s1 and not s2 and i3) or (not s0
and not s1 and not s2 and i4)or ( s0 and not s1 and s2 and i5) or (not s0 and  s1
and  s2 and i6) or ( s0 and  s1 and s2 and i7);

end dataflow;
```

FOR 32X1 MUX:



RTL Schematic of 32x1 Multiplexer



Source Code for 32x1 Multiplexer

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity mux_32x1 is
    Port ( i : in STD_LOGIC_VECTOR (31 downto 0);
           s : in STD_LOGIC_VECTOR (4 downto 0);
           op : out STD_LOGIC);
end mux_32x1;

architecture structural of mux_32x1 is
component mux_8x1 is
 Port ( i0,i1,i2,i3,i4,i5,i6,i7 : in STD_LOGIC;
          s0,s1,s2 : in STD_LOGIC;
          op : out STD_LOGIC);
end component;
component mux_4x1 is
    Port ( i0,i1,i2,i3 : in STD_LOGIC;
           s0,s1 : in STD_LOGIC;
           op : out STD_LOGIC);
end component;
signal t:std_logic_vector (3 downto 0);
begin
m8x1_1:mux_8x1 port map(i(0),i(1),i(2),i(3),i(4),i(5),i(6),i(7),s(2),s(3),s(4),t(0));
m8x1_2:mux_8x1 port
map(i(8),i(9),i(10),i(11),i(12),i(13),i(14),i(15),s(2),s(3),s(4),t(1));
m8x1_3:mux_8x1 port
map(i(16),i(17),i(18),i(19),i(20),i(21),i(22),i(23),s(2),s(3),s(4),t(2));
m8x1_4:mux_8x1 port
map(i(24),i(25),i(26),i(27),i(28),i(29),i(30),i(31),s(2),s(3),s(4),t(3));
m4x1_5:mux_4x1 port map(t(0),t(1),t(2),t(3),s(0),s(1),op);

end structural;
```

5. Results & Interpretation

I) Verification of the output for different inputs that satisfies the problem statement by the use of truth table.

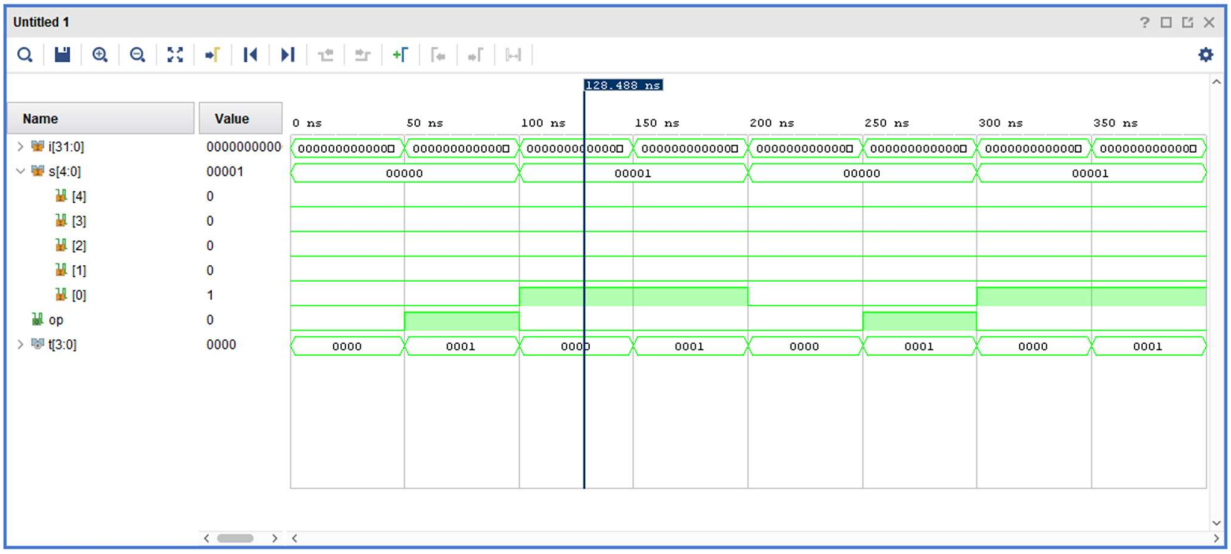
EXPECTED OUTPUT:

S4	S3	S2	S1	S0	Y
0	0	0	0	0	I0
0	0	0	0	1	I1
0	0	0	1	0	I2
0	0	0	1	1	I3
0	0	1	0	0	I4
0	0	1	0	1	I5
0	0	1	1	0	I6
0	0	1	1	1	I7
0	1	0	0	0	I8
0	1	0	0	1	I9
0	1	0	1	0	I10
0	1	0	1	1	I11
0	1	1	0	0	I12
0	1	1	0	1	I13
0	1	1	1	0	I14
0	1	1	1	1	I15
1	0	0	0	0	I16
1	0	0	0	1	I17
1	0	0	1	0	I18
1	0	0	1	1	I19
1	0	1	0	0	I20
1	0	1	0	1	I21
1	0	1	1	0	I22
1	0	1	1	1	I23
1	1	0	0	0	I24
1	1	0	0	1	I25
1	1	0	1	0	I26
1	1	0	1	1	I27
1	1	1	0	0	I28
1	1	1	0	1	I29
1	1	1	1	0	I30
1	1	1	1	1	I31

OBSERVED OUTPUT:

S4	S3	S2	S1	S0	Y
0	0	0	0	0	I0
0	0	0	0	1	I1
0	0	0	1	0	I2
0	0	0	1	1	I3
0	0	1	0	0	I4
0	0	1	0	1	I5
0	0	1	1	0	I6
0	0	1	1	1	I7
0	1	0	0	0	I8
0	1	0	0	1	I9
0	1	0	1	0	I10
0	1	0	1	1	I11
0	1	1	0	0	I12
0	1	1	0	1	I13
0	1	1	1	0	I14
0	1	1	1	1	I15
1	0	0	0	0	I16
1	0	0	0	1	I17
1	0	0	1	0	I18
1	0	0	1	1	I19
1	0	1	0	0	I20
1	0	1	0	1	I21
1	0	1	1	0	I22
1	0	1	1	1	I23
1	1	0	0	0	I24
1	1	0	0	1	I25
1	1	0	1	0	I26
1	1	0	1	1	I27
1	1	1	0	0	I28
1	1	1	0	1	I29
1	1	1	1	0	I30
1	1	1	1	1	I31

TBW:


Untitled 1
128.488 ns
Name
Value
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
i[31:0]
0000000000
s[4:0]
00001
00000
00001
00000
00001
[4]
0
[3]
0
[2]
0
[1]
0
[0]
1
op
0
t[3:0]
0000
0000
0001
0000
0001
0000
0001
0000
0001

6. CONCLUSION:

The design and simulation of a 32x1 multiplexer using 8x1 and 4x1 multiplexers was successfully accomplished. The proposed design demonstrated a cost-effective and efficient approach, reducing complexity and cost. The simulation results verified the functionality, showcasing the potential of using smaller multiplexers to implement larger ones.

7. REFERENCES:

- **Charles H. Roth Jr.; Larry L. Kinney: "FUNDAMENTALS OF LOGIC DESIGN", 7th Edition.**
- **M. Morris Mano; Michael D. Cileti: "DIGITAL DEDIGN WITH AN INTRODUCTION TO THE VERILOG, HDL, VHDL, and SYSTEM VERILOG", 6th Edition.**

8. APPENDICES:

74HC151; 74HCT151

8-input multiplexer

Rev. 11 — 11 March 2024 Product data sheet

1. General description

The 74HC151; 74HCT151 is an 8-bit multiplexer with eight binary inputs (I0 to I7), three select inputs (S0 to S2) and an enable input (E). One of the eight binary inputs is selected by the select inputs and routed to the complementary outputs (Y and $\overline{Y}$). A HIGH on $\overline{E}$ forces the output Y LOW and output $\overline{Y}$ HIGH. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC151: CMOS level
  - For 74HCT151: TTL level
- Non-inverting data path
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
- • HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC151D 74HCT151D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC151PW 74HCT151PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC151BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

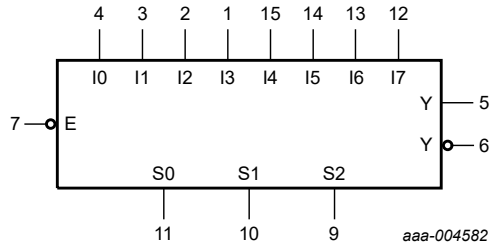


Fig. 1. Logic symbol

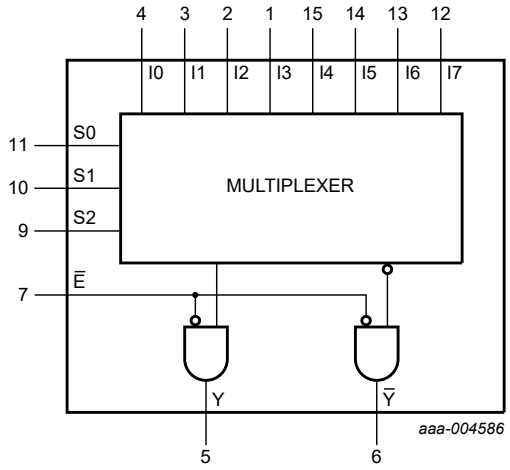


Fig. 2. Functional diagram

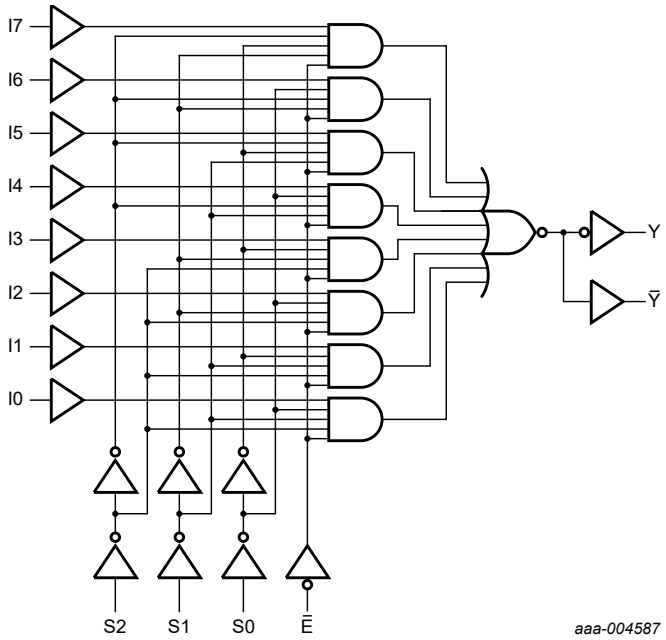
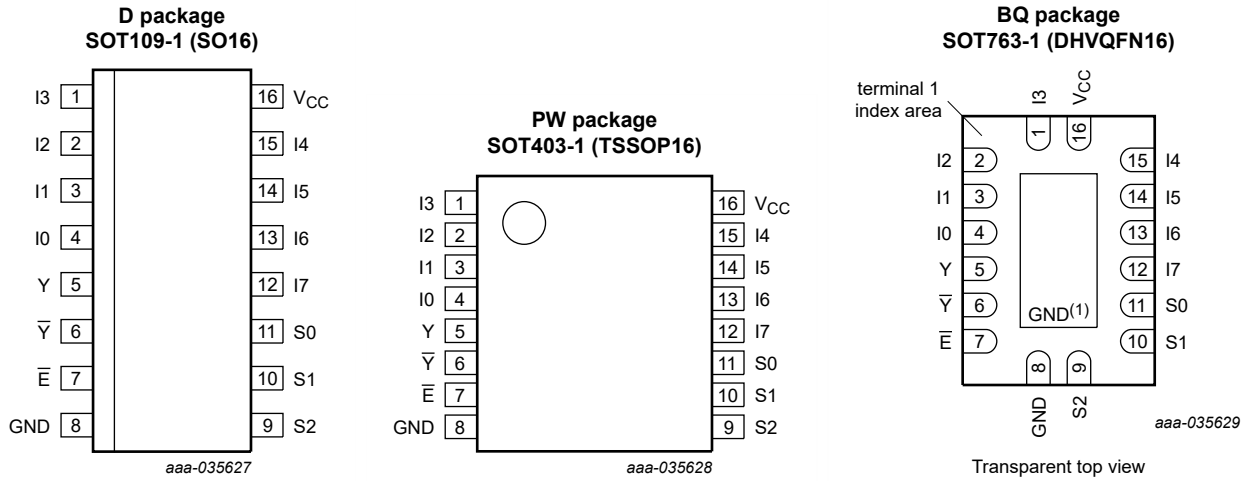


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
I0, I1, I2, I3, I4, I5, I6, I7	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Y	5	multiplexer output
$\overline{Y}$	6	complementary multiplexer output
$\overline{E}$	7	enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input												Output	
$\overline{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC151			74HCT151			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC151										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT151										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; In inputs	-	45	162	-	203	-	221	µA
		per input pin; $\overline{E}$ input	-	30	108	-	135	-	147	µA
		per input pin; Sn input	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

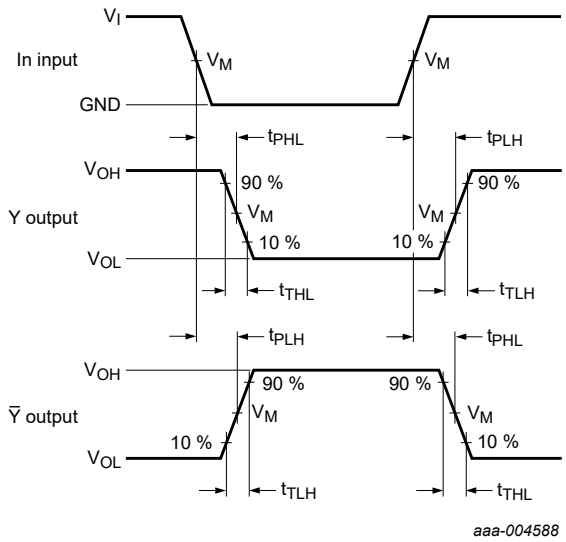
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC151										
t_{pd}	propagation delay	In to Y; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	52	170	-	215	-	255	ns
		V_{CC} = 4.5 V	-	19	34	-	43	-	51	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	29	-	37	-	43	ns
		In to $\overline{Y}$; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	58	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	21	37	-	46	-	56	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	17	31	-	39	-	48	ns
		Sn to Y; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	61	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	31	-	39	-	48	ns
		Sn to $\overline{Y}$; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	61	205	-	255	-	310	ns
		V_{CC} = 4.5 V	-	22	41	-	51	-	62	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	35	-	43	-	53	ns
		$\overline{E}$ to Y; see Fig. 5								
		V_{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	21	-	26	-	32	ns
		$\overline{E}$ to $\overline{Y}$; see Fig. 5								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
t_t	transition time	Y, $\overline{Y}$; see Fig. 4 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	40	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT151										
t_{pd}	propagation delay	In to Y; see Fig. 4 [1]								
		V_{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		In to $\overline{Y}$; see Fig. 4 [1]								
		V_{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		Sn to Y; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	23	41	-	51	-	62	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		Sn to $\overline{Y}$; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		$\overline{E}$ to Y; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	16	29	-	36	-	44	ns
		V_{CC} = 5 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		$\overline{E}$ to $\overline{Y}$; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
t_t	transition time	Y, $\overline{Y}$; see Fig. 4 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V [3]	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

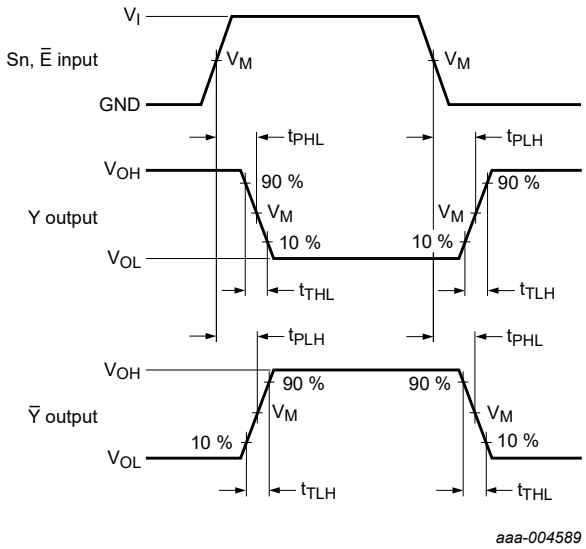
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delay input (In) to output (Y, $\overline{Y}$) and the output (Y, $\overline{Y}$) transition time



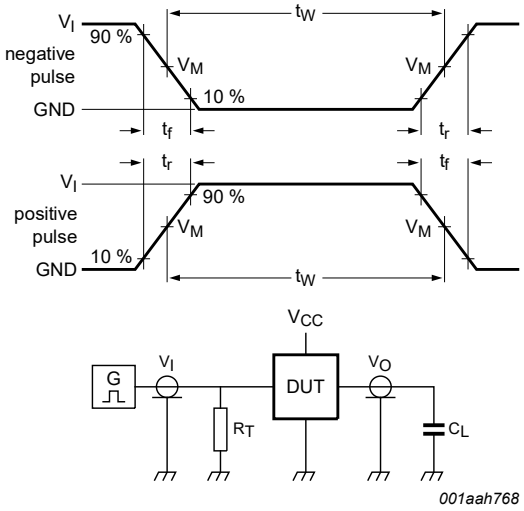
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (Sn, $\overline{E}$) to output (Y, $\overline{Y}$) and output (Y, $\overline{Y}$) transitions time

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC151	0.5 × V_{CC}	0.5 × V_{CC}
74HCT151	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

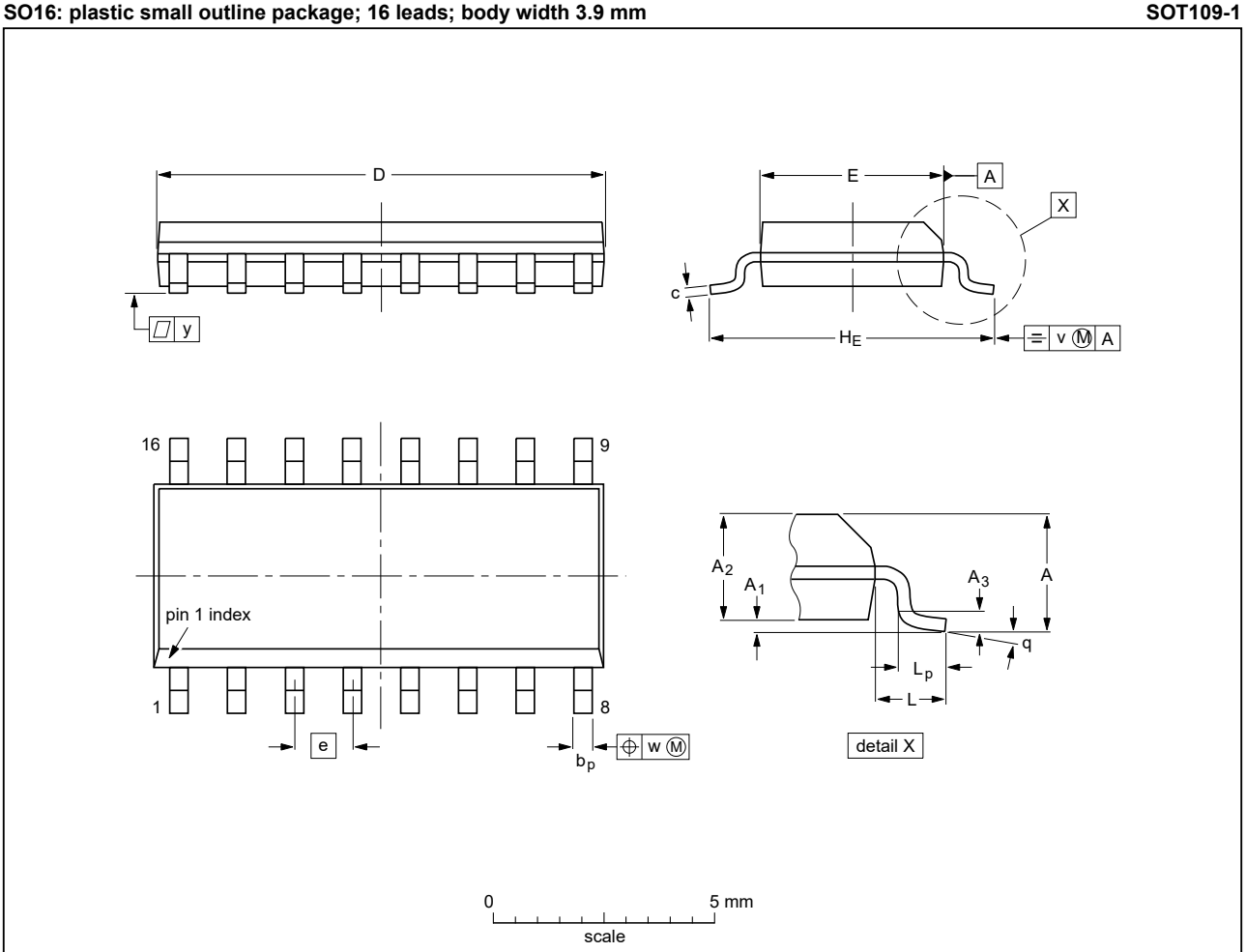
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC151	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT151	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

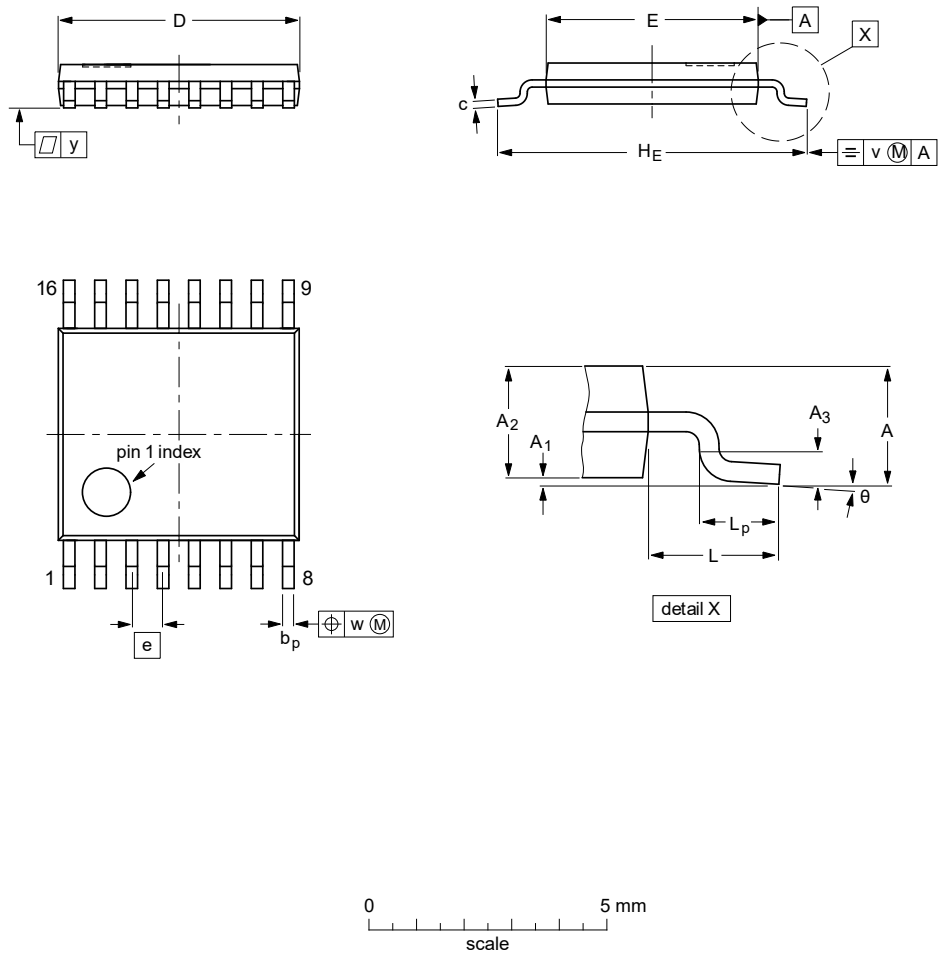
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

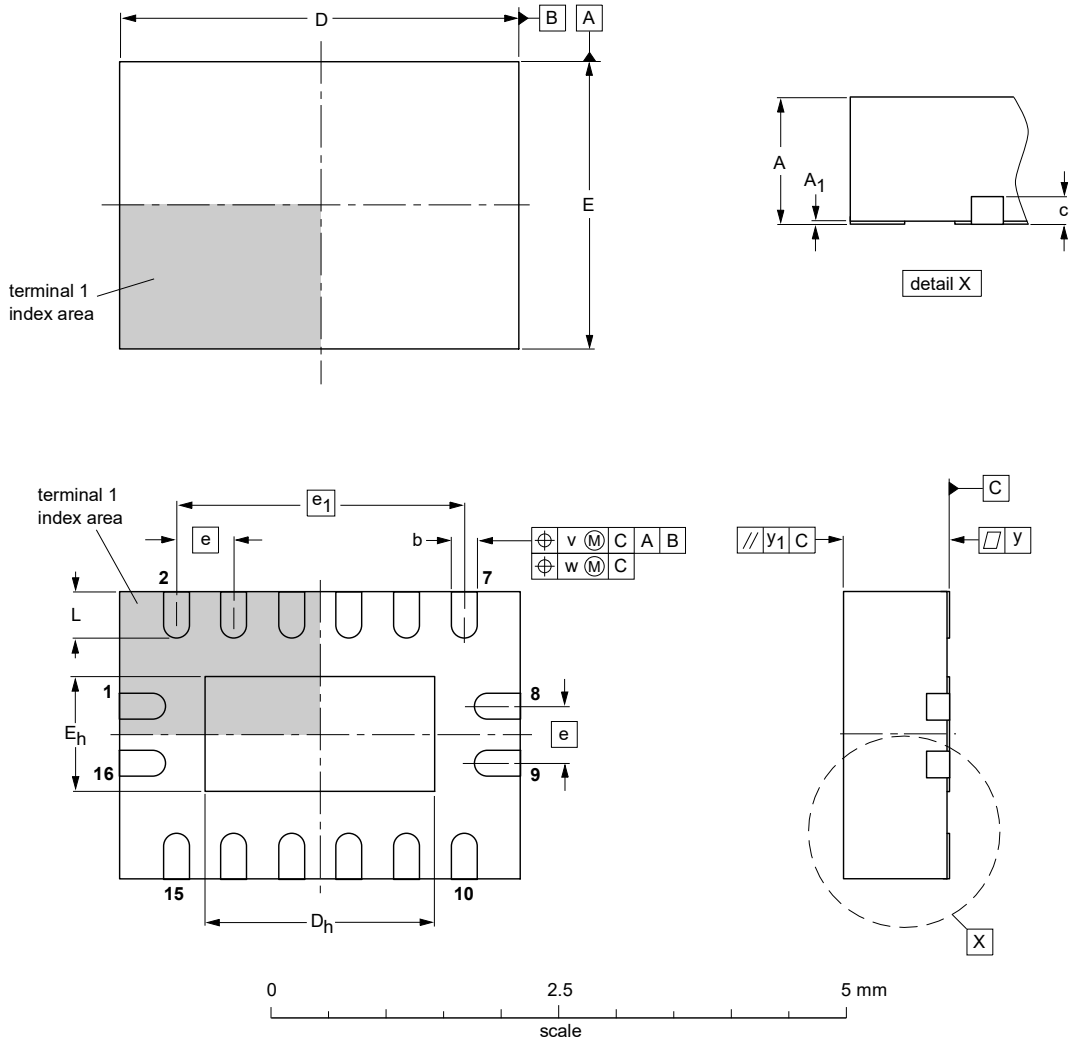
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 9. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT151 v.11	20240311	Product data sheet	-	74HC_HCT151 v.10
Modifications:	• Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT151 v.10	20221019	Product data sheet	-	74HC_HCT151 v.9
Modifications:	• Type number 74HC151BQ (SOT763-1/DHVQFN16) added.			
74HC_HCT151 v.9	20220706	Product data sheet	-	74HC_HCT151 v.8
Modifications:	• Section 2 updated. • Type number 74HC151DB (SOT338-1/SSOP16) removed.			
74HC_HCT151 v.8	20210318	Product data sheet	-	74HC_HCT151 v.7
Modifications:	• Type number 74HC151DB (SOT338-1/SSOP16) added.			
74HC_HCT151 v.7	20210114	Product data sheet	-	74HC_HCT151 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC151DB and 74HCT151DB (SOT338-1/SSOP16) removed. • Section 7: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT151 v.6	20151228	Product data sheet	-	74HC_HCT151 v.5
Modifications:	• Type numbers 74HC151N and 74HCT151N (SOT38-4) removed.			
74HC_HCT151 v.5	20150126	Product data sheet	-	74HC_HCT151 v.4
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT151 is corrected.			
74HC_HCT151 v.4	20130211	Product data sheet	-	74HC_HCT151 v.3
Modifications:	• New descriptive title (errata).			
74HC_HCT151 v.3	20120919	Product data sheet	-	74HC_HCT151_CNV v.2
74HC_HCT151_CNV v.2	19970827	Product specification	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 11 March 2024

74HC153; 74HCT153

Dual 4-input multiplexer

Rev. 11 — 11 March 2024 Product data sheet

1. General description

The 74HC153; 74HCT153 is a dual 4-input multiplexer. The device features independent enable inputs ($n\overline{E}$) and common data select inputs (S0 and S1). For each multiplexer, the select inputs select one of the four binary inputs and routes it to the multiplexer output (nY). A HIGH on $\overline{E}$ forces the corresponding multiplexer outputs LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC153: CMOS level
  - For 74HCT153: TTL level
- Non-inverting outputs
- Separate enable input for each output
- Common select inputs
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC153D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT153D				
74HC153PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT153PW				

4. Functional diagram

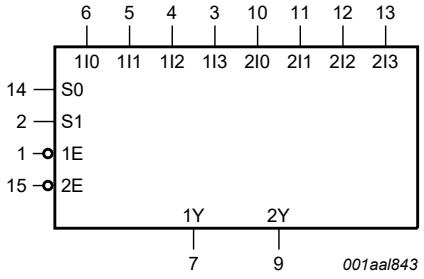


Fig. 1. Logic symbol

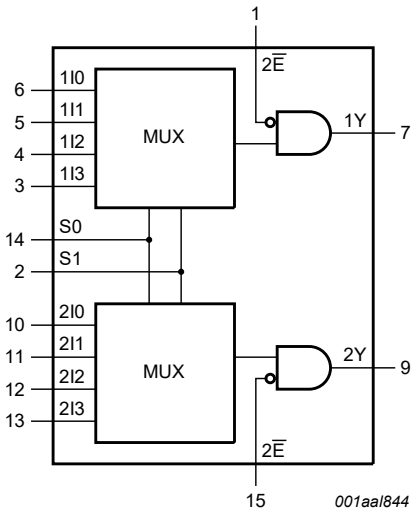


Fig. 2. Functional diagram

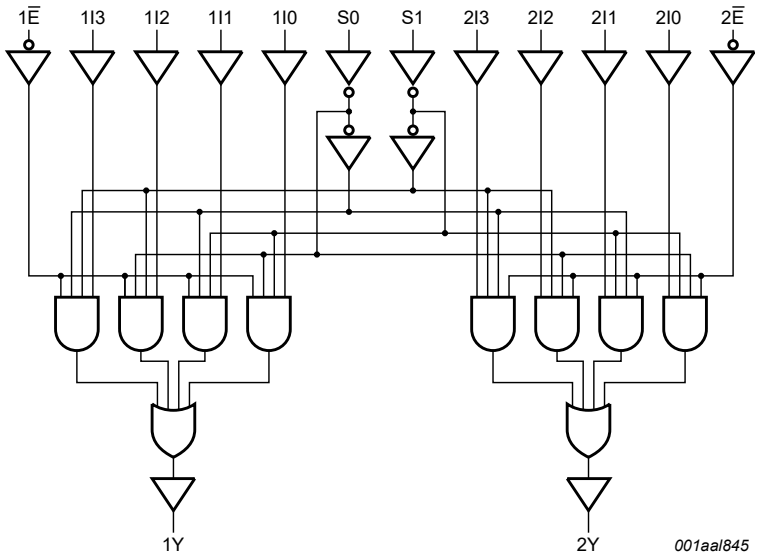


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

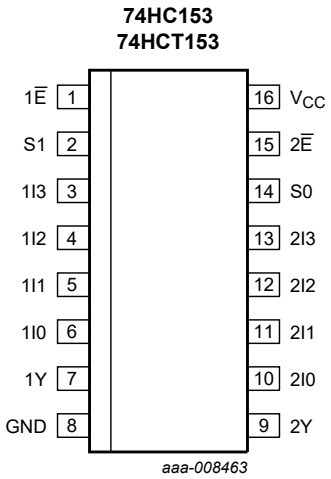


Fig. 4. Pin configuration SOT109-1 (SO16)

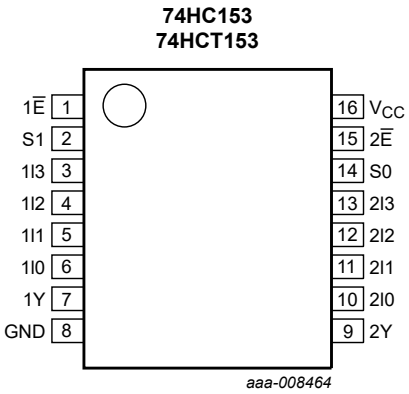


Fig. 5. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{E}$, $2\overline{E}$	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
1I0, 1I1, 1I2, 1I3	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
2I0, 2I1, 2I2, 2I3	10, 11, 12, 13	data inputs source 2
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

select Inputs		data inputs				output enable	output
S0	**S1**	**nI0**	**nI1**	**nI2**	**nI3**	**nE̅**	**nY**
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC153			74HCT153			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC153										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT153										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		1In, 2In	-	45	162	-	203	-	221	µA
		$n\overline{E}$	-	60	216	-	270	-	294	µA
		Sn	-	135	486	-	608	-	662	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

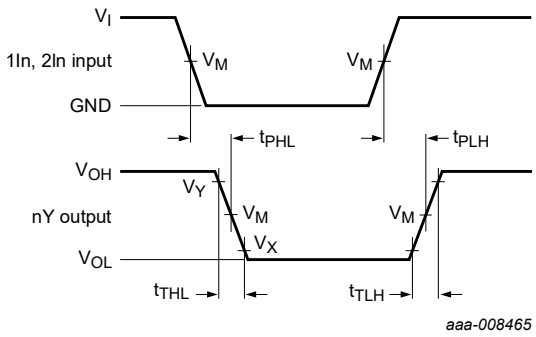
Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; for test circuit, see Fig. 8; unless otherwise specified

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC153										
t_{pd}	propagation delay	1In to nY, 2In to nY; see Fig. 6 [1]								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		Sn to nY; see Fig. 7								
		V_{CC} = 2.0 V	-	50	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	18	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns
		$n\overline{E}$ to nY; see Fig. 7								
		V_{CC} = 2.0 V	-	33	100	-	125	-	150	ns
		V_{CC} = 4.5 V	-	12	20	-	25	-	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	10	17	-	21	-	26	ns
t_t	transition time	see Fig. 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	30	-	-	-	-	-	pF

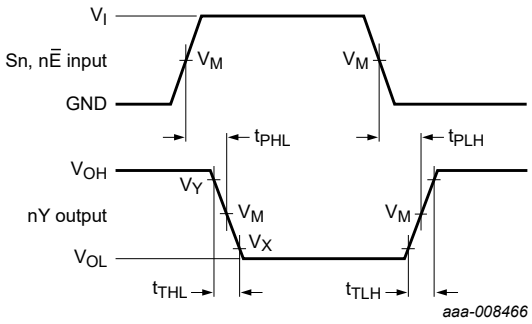
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT153										
t_{PHL}	HIGH to LOW propagation delay	1In to nY, 2In to nY; see Fig. 6 [1]								
		V_{CC} = 4.5 V	-	19	34	-	43	-	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
t_{PLH}	LOW to HIGH propagation delay	1In to nY, 2In to nY; see Fig. 6 [1]								
		V_{CC} = 4.5 V	-	13	24	-	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
t_{pd}	propagation delay	Sn to nY; see Fig. 7 [1]								
		V_{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		$n\overline{E}$ to nY; see Fig. 7 [1]								
		V_{CC} = 4.5 V	-	14	27	-	34	-	41	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
t_t	transition time	see Fig. 6 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} - 1.5 V [3]	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Waveforms showing the input (1In, 2In) to output (1Y, 2Y) propagation delays and output transition times



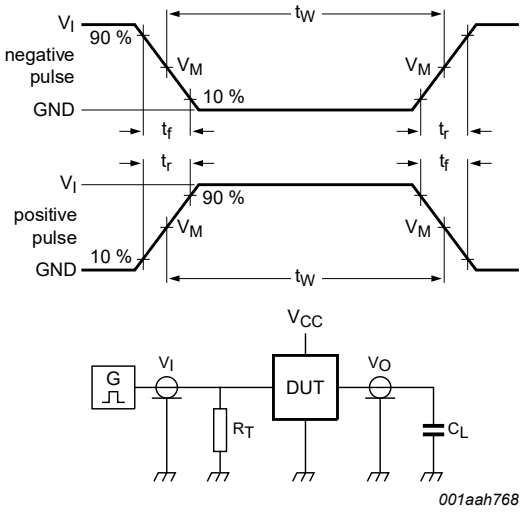
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the input (Sn, nĒ) to output (nY) propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC153	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT153	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

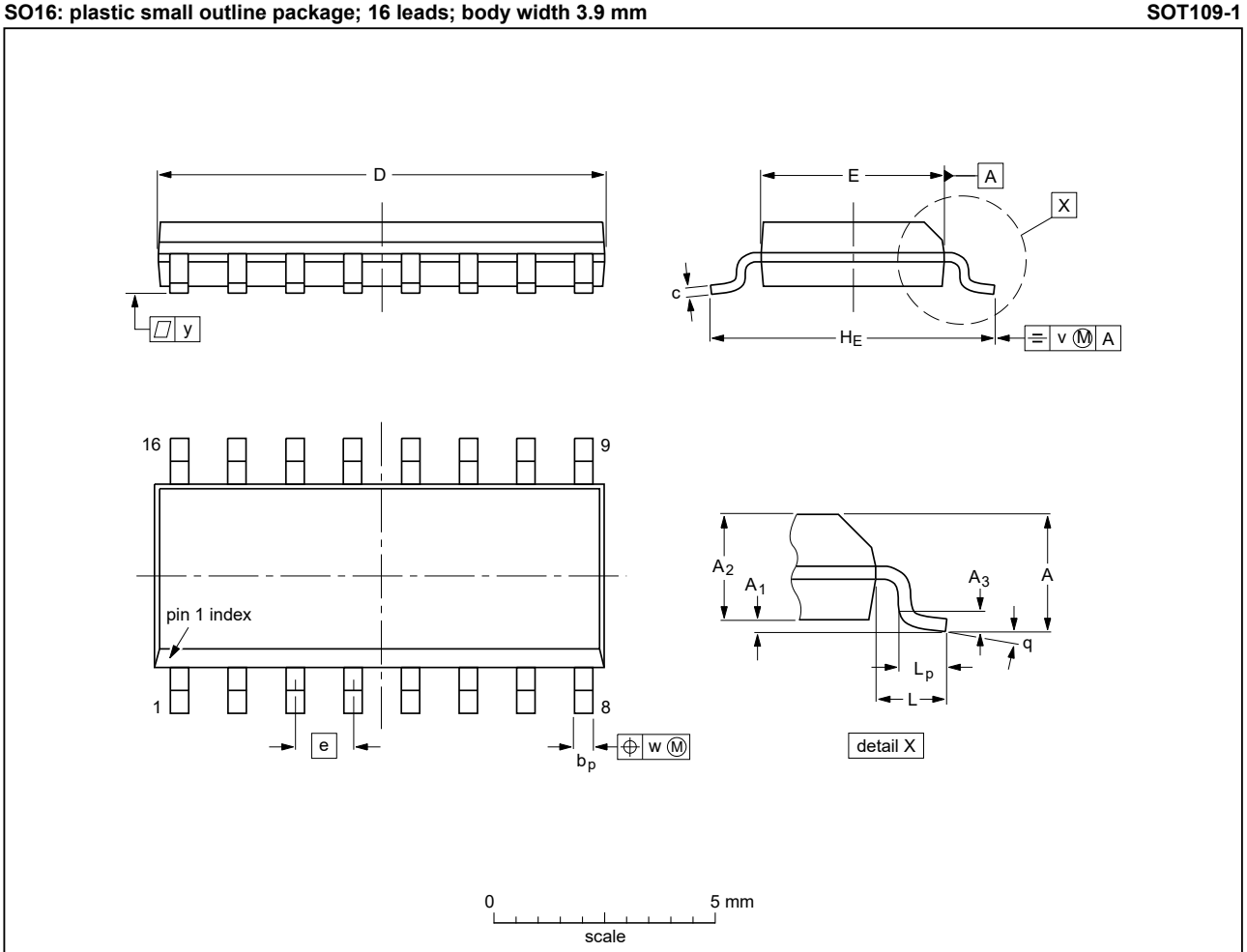
Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC153	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT153	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

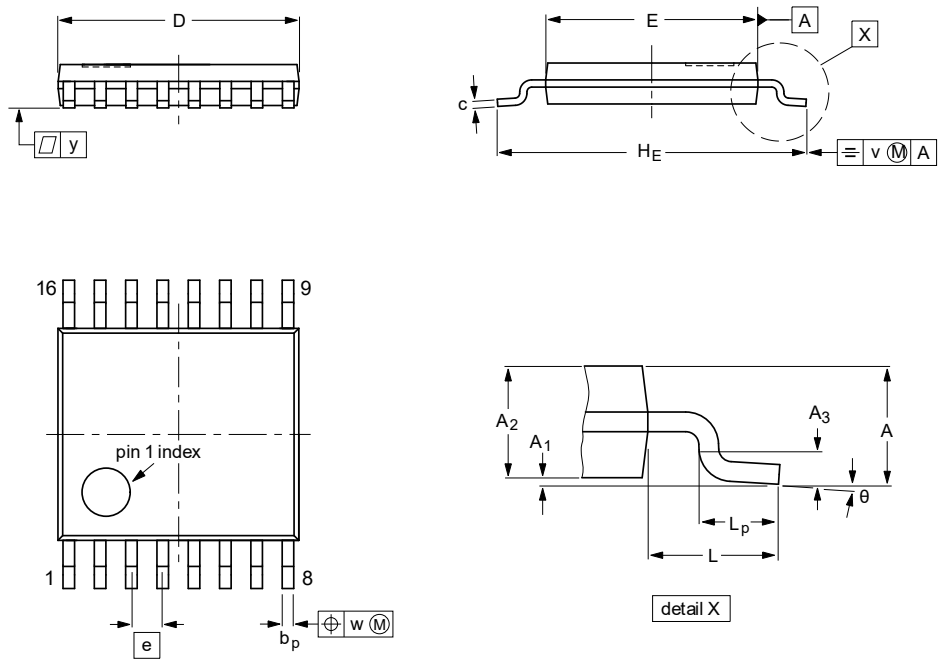
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

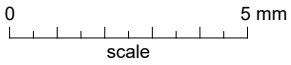
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm nom				0.25					0.65		1		0.2	0.1	0.1	
min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 10. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT153 v.11	20240311	Product data sheet	-	74HC_HCT153 v.10
Modifications:	• Fig. 9, Fig. 10: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT153 v.10	20210813	Product data sheet	-	74HC_HCT153 v.9
Modifications:	• Type number 74HC153DB (SOT338-1/SSOP16) removed. • Section 2 updated.			
74HC_HCT153 v.9	20210114	Product data sheet	-	74HC_HCT153 v.8
Modifications:	• Type number 74HCT153DB (SOT338-1/SSOP16) removed.			
74HC_HCT153 v.8	20190813	Product data sheet	-	74HC_HCT153 v.7
Modifications:	• Type numbers 74HC153DB and 74HCT153DB (SOT338-1/SSOP16) added. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT153 v.7	20181010	Product data sheet	-	74HC_HCT153 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC153DB and 74HCT153DB (SOT338-1/SSOP16) removed.			
74HC_HCT153 v.6	20160511	Product data sheet	-	74HC_HCT153 v.5
Modifications:	• Type numbers 74HC153N and 74HCT153N (SOT38-4) removed.			
74HC_HCT153 v.5	20140123	Product data sheet	-	74HC_HCT153 v.4
Modifications:	• Table 1 and Section 11: all references to 14 pin packages removed.			
74HC_HCT153 v.4	20131128	Product data sheet	-	74HC_HCT153 v.3
74HC_HCT153 v.3	20130722	Product data sheet	-	74HC_HCT153_CNV v.2
74HC_HCT153_CNV v.2	19970827	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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