SURYACHANDRA PRASAD PASUPULETI

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EDUCATION

Birla Institute of Science and Technology Pilani , Goa campus *Aug '14 - Aug '19*

Bachelor of Engineering (Hons.), Electrical and Electronics Engineering
Master of Science (Hons.), Chemistry (integrated dual degree)

TEST SCORES

GRE: 325 Quant:168 Verbal:158 AWA: 3.5
TOEFL: 100 R:27 L:30 S:22 W:21

RESEARCH EXPERIENCE

Research Intern,Computer Systems Group, IIIT Hyderabad *Aug '19 - Dec '19*
Advisor: Dr. Suresh Purini

Successfully integrated the verilog code generated by the Framework being developed in the lab into vivado flow and implemented an end to end real time image processing system on zynq SOCs(zedboard and zybo z-7010) and zynq Ultrascale (ZCU102) boards.

Undergrad Thesis,International Institute of Information Technology(IIIT),Hyderabad
Advisor: Dr. Suresh Purini
Title: Accelerating Image Processing Pipelines on FPGA Architectures *Aug '18 - Dec '18*

The project aims at designing the backend for the compiler being developed in the lab for image processing applications. Backend is written in Bluespec .
Ported the Bilateral Grid Algorithmn into the Framework by exploiting various levels of parallelism present in the Algorithmn.

INTERNSHIPS

Healthcare Technology Innovation Centre IIT Madras,Chennai
Title: FPGA Firmware Development for Endoscopy *Jan '19 - Jun '19*

Worked on analyzing the data processing of Endoscopy and ported them to FPGA hardware. **Rourkela Steel Plant**
Title: Level 1 to Level 2 Interfacing *May '16 - July '16*
Vocational training at the plant as part of University requirement.

MAJOR COURSE PROJECTS

Designed and Implemented various Image processing Algorithmns in vivado HLS
Designed filters like sobel , gaussian , canny edge filters in vivado HLS and tested them on zedboard and compared them with the results of the framework in the lab.Codes and related files are shared on github.

Implementation of single cycle and 4 stage pipelined processor in verilog
Implemented a single cycle and 4 stage pipelined processor with branching,forwarding etc in verilog as part of assignments.

Gateway design for IOT
Implemented a IOT gateway using the STM32F407 board as the gateway and using zigbees to send data to the microcontroller and the microcontroller sends the data to the mobile phone via bluetooth module. Completed the project as the part of the course Embedded System Design.

Normal Mode Analysis of Octa coordinated Boron(B9-)
Performed quantum chemistry calculations on octa co-ordianted boron molecule using cfour package developed at the university of Mainz and compared the results with a research paper to evaluate the performance of the package.

RELEVANT COURSES

Computer Architecture
Embedded Systems Design
Digital Design
Microprocessors and Interfacing
Micro Electronics
Control Systems
Signals and Systems
Electronic Deivices

SKILLS

Languages : Bluespec systemverilog,C,C++,verilog,matlab,python
Tools/Hardware: Xilinx Vivado,petalinux,FPGAs,Zynq SoCs,Zynq Ultrascale SoCs, Vivado HLS