External Project Report on Digital Logic Design (EET1211)

[4-BIT BCD TO XS-3 CONVERTER]

Submitted by

Name : Suryakanta Nishank	**Reg. No.: 2241014157**
Name: Dibyadarshi Mohanty	**Reg. No.: 2241013242**
Name: Debi prasad Mohanty	**Reg. No.: 2241013239**
Name: Samiksha Mund	**Reg. No.: 2241013380**

B. Tech. CSE 3rd Semester (Section - 31)

INSTITUTE OF TECHNICAL EDUCATION AND RESEARCH
(FACULTY OF ENGINEERING)
SIKSHA 'O' ANUSANDHAN (DEEMED TO BE UNIVERSITY), BHUBANESWAR, ODISHA

Declaration

We, the undersigned students of B. Tech. of **CSE** Department hereby declare that we own the full responsibility for the information, results etc. provided in this PROJECT titled "**(4-BIT BCD TO XS-3 CONVERTER)**" submitted to **Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar** for the partial fulfillment of the subject **Digital Logic Design (EET 1211)**. We have taken care in all respect to honor the intellectual property right and have acknowledged the contribution of others for using them in academic purpose and further declare that in case of any violation of intellectual property right or copyright we, as the candidate(s), will be fully responsible for the same.

(SURYAKANTA NISHANK)

Registration No.:2241014157

(DIBYADARSHI MOHANTY)

Registration No.:2241013242

(DEBI PRASAD MOHANTY)

Registration No.:2241013239

(SAMIKSHA MUND

Registration No.: 2241013380

DATE: 15/01/24
PLACE: Institute of Technology and Educational Research(Deemed to be University)

Abstract

The **4-BIT BCD to XS-3 Converter** project presents an innovative digital circuit design aimed at efficiently converting Binary-Coded Decimal (BCD) representations to Excess-3 (XS-3) representations. BCD and XS-3 are commonly used binary-coded decimal codes, with XS-3 being a self-complementing code that simplifies arithmetic operations in digital systems.

The project focuses on developing a compact and optimized circuit that seamlessly converts 4-bit BCD inputs into their corresponding XS-3 equivalents. The conversion is crucial in applications where arithmetic operations need to be performed with ease and efficiency, as XS-3 simplifies the addition and subtraction processes.

The key objectives of the project include:

1. Efficient Conversion Algorithm: Designing a robust algorithm for converting 4-bit BCD inputs to XS-3 with minimal hardware complexity, ensuring high-speed operation and low power consumption.

2. Compact Circuit Implementation: Developing a compact and space-efficient hardware circuit using standard digital components, suitable for integration into various digital systems and applications.

3. Optimized Performance: Achieving optimized performance metrics such as speed, power efficiency, and reliability through careful selection of components and circuit design.

4. Testing and Validation: Rigorous testing and validation of the converter circuit to ensure accurate and reliable conversion under various input conditions. Verification of the design against simulated and real-world scenarios .

In conclusion, the 4-BIT BCD to XS-3 Converter project aims to contribute to the advancement of digital circuit design by providing a compact, efficient, and reliable solution for converting BCD to XS-3, thereby enhancing the overall performance of digital systems requiring arithmetic computations. The successful implementation of this project promises to open avenues for improved functionality and efficiency in a variety of digital applications.

Contents

1. Introduction

In the realm of digital electronics, binary-coded decimal (BCD) representation is a widely used method to encode decimal numbers using binary digits. BCD to XS-3 conversion is a crucial process in digital systems, especially in applications where arithmetic operations involving decimal numbers are performed.

This project aims to design and implement a 4-bit BCD to XS-3 (Excess-3) converter. Excess-3 is a binary-coded decimal code in which each decimal digit is represented by its corresponding 4-bit binary representation plus 0011. The conversion from BCD to XS-3 is a key step in various digital systems, including calculators, digital clocks, and other devices where decimal arithmetic operations are essential.

The primary objective of this project is to create a 4-bit BCD to XS-3 converter circuit that can accurately and efficiently convert binary-coded decimal input into its corresponding Excess-3 representation. The designed converter will employ digital logic gates, combinational circuits, and Boolean algebra to achieve the desired functionality.

Key Components:

1.BCD Input:
The project will take a 4-bit BCD input, representing decimal digits from 0 to 9.

2. XS-3 Output:
The converter will produce a 4-bit XS-3 output corresponding to the BCD input.

3.Digital Logic Gates:
The core of the project will involve the utilization of digital logic gates such as AND, OR, and XOR gates to implement the conversion logic.

4.Combinational Circuits:
Combinational circuits will be designed to perform the necessary arithmetic operations on the BCD input to generate the Excess-3 output.

This introduction lays the foundation for an in-depth exploration of the project, highlighting its importance, objectives, and key components. The subsequent sections will delve into the theoretical background, design methodology, simulation results, and practical implementation, providing a comprehensive overview of the 4-Bit BCD to XS-3 Converter project.

2. Problem Statement

In a 4-Bit Binary-Coded Decimal (BCD) to Excess-3 (XS-3) Converter project, the main objective is to design a circuit or system that can take a 4-bit BCD input and convert it into its corresponding 4-bit XS-3 code.

1.Input Variables:

4-bit Binary-Coded Decimal (BCD): This is the binary representation of a decimal digit, where each decimal digit is represented by a 4-bit binary number.

2.Output Variables:

4-bit Excess-3 (XS-3): This is the binary representation of a decimal digit in excess-3 code, which means each decimal digit is represented by adding 3 to its corresponding BCD value.

Highlighting the Constraints:

When working on the 4-Bit BCD to XS-3 Converter project, there are certain constraints and considerations that need to be taken into account:

1.Input Range:

The BCD input should be within the valid range of 0 to 9. Since BCD represents decimal digits, values beyond this range are not applicable.

2.Output Range:

The XS-3 output should be designed to represent decimal digits from 3 to 12 (BCD + 3). Values beyond this range are not valid for XS-3 representation.

3.Conversion Logic:

Designing the logic to convert BCD to XS-3 involves considering the addition of 3 to each BCD digit. Proper arithmetic and logical operations must be implemented to achieve accurate conversion.

3.Implementation Platform:

Consider the platform on which the converter will be implemented (e.g., digital logic circuit[Bread Board], FPGA, microcontroller). The choice of platform may influence the design and implementation details.

4.Size and Complexity:

The design should be space-efficient and not overly complex, especially if the application has size or resource constraints.

5.Testing and Validation:

Plan for thorough testing to validate the correct functionality of the converter under various input conditions.

By addressing these constraints, you can develop a robust and reliable 4-Bit BCD to XS-3 converter.

3. Methodology

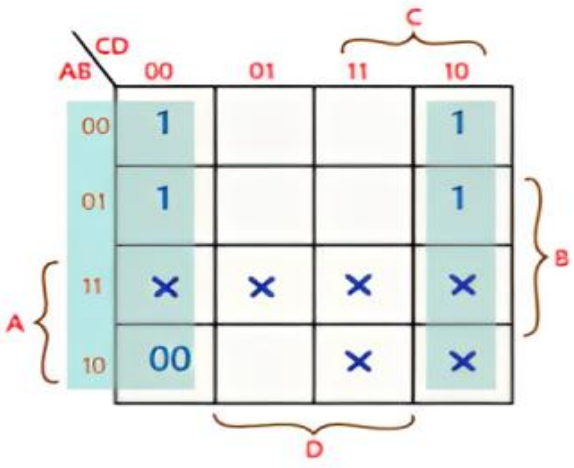
1. Generating the solution to the problem by the use of Truth table/excitation table, K-map and (or) Boolean algebra.

TRUTHTABLE:

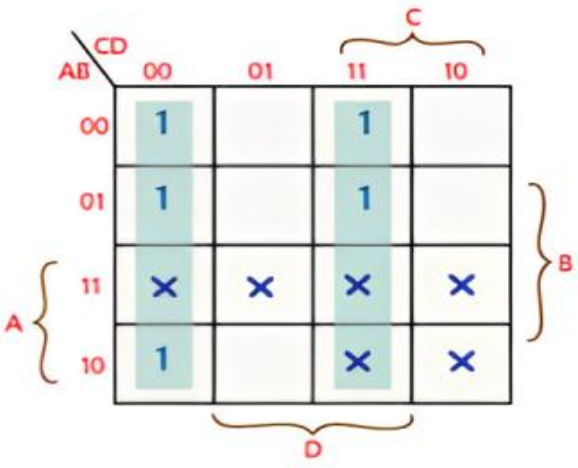
Decimal Number	BCD Code				Excess-3 Code			
	A	B	C	D	W	x	y	z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

K-MAP:

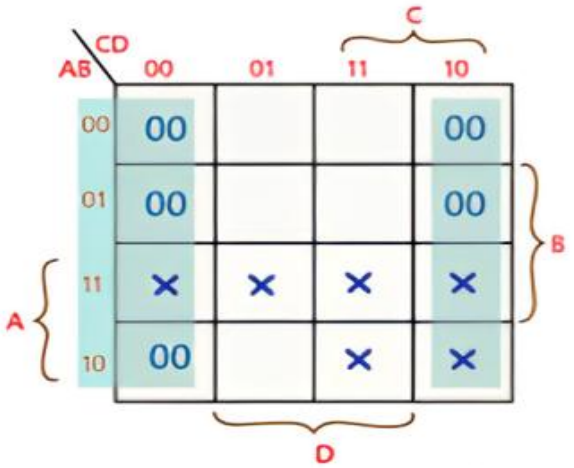
Now, we will use the K-map method to design the logical circuit for the conversion of BCD To Excess-3 Code:



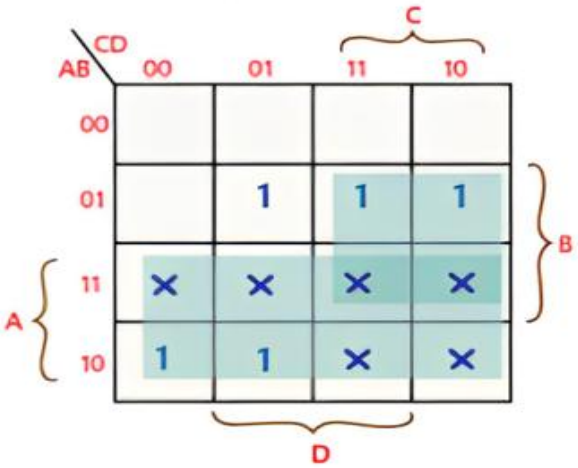
z=D′



y=CD+C′D′



x=B′C+B′D+BC′D′



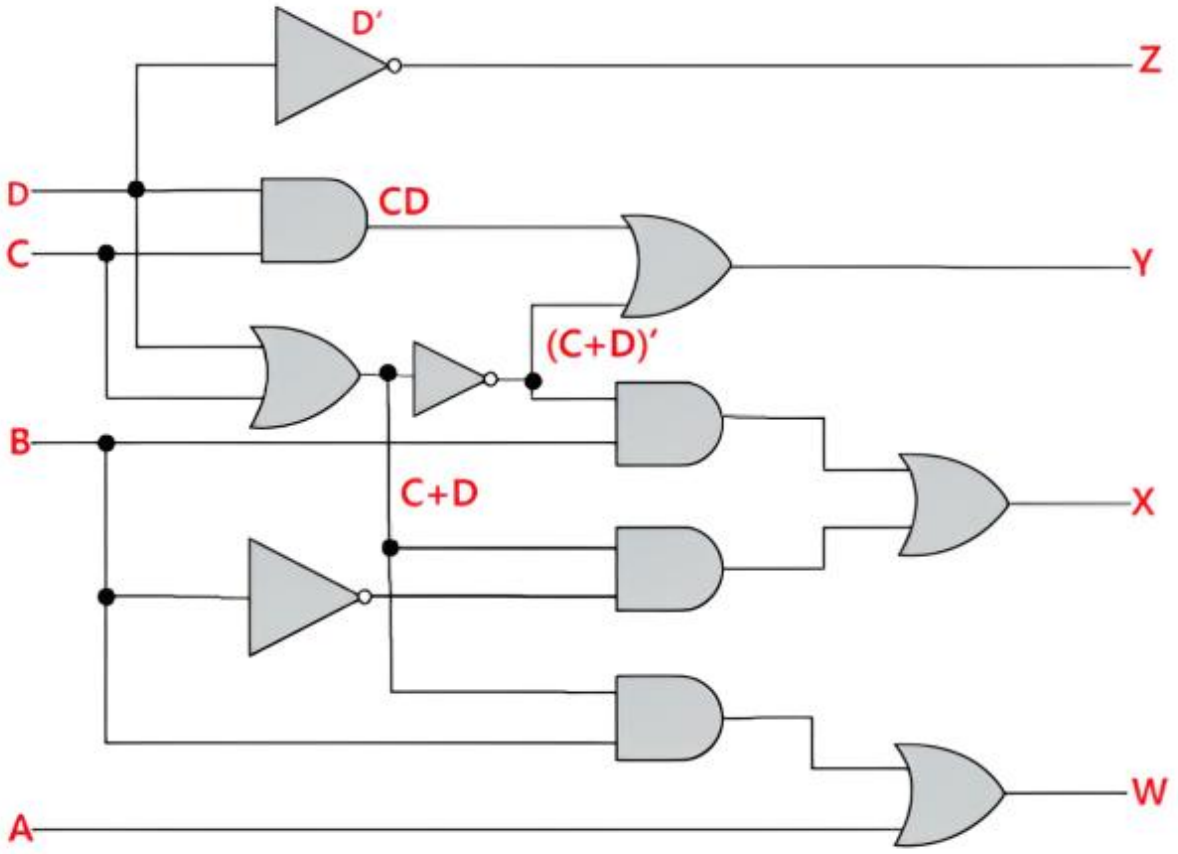
w=A+BC+BD

BOOLEAN EXPRESSION:

1. w=A+BC+BD
2. x=B' C+B' D+BC' D'
3. y=CD+C'D'
4. z=D'

4. Implementation

I. LOGIC DIAGRAM USING DIFFERENT LOGIC GATES

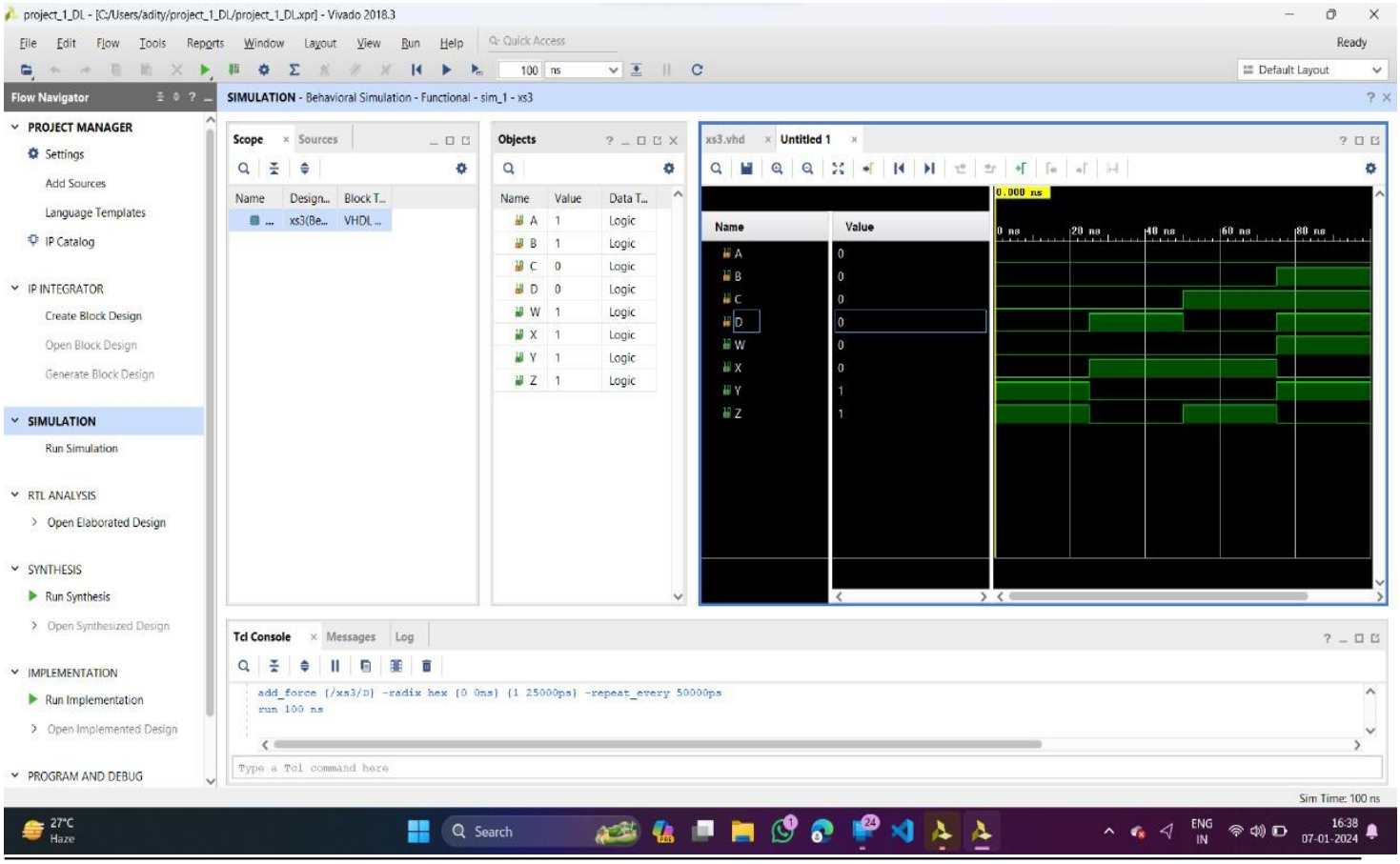


II. PROGRAM:

```
 entity xs3 is
Port (A,B,C,D : in STD_LOGIC;
       W,X,Y,Z : out STD_LOGIC);
  end xs3;
 architecture Behavioral of xs3 is
begin
W <= A OR (B AND D) OR (B AND C);
X <=(B AND (NOT C) AND (NOT D)) OR ((NOT B) AND D) OR ((NOT B) AND C);
Y <= C XNOR D;
Z <=(( NOT C) AND (NOT D )) OR ( C AND (NOT D));

end Behavioral;
```

III. WAVEFORM:



5. Results & Interpretation

To verify the outputs for different inputs based on the truth table to ensure they satisfy the problem statement of a three-bit magnitude comparator.We take two examples.

Example 1

Convert the BCD number 627 (0110 0010 0111) into its equivalent Excess-3 code.

Solution –– Given BCD number is –

627 = 0110 0010 0111

Adding 3 (0011) to each BCD code to obtain its equivalent Excess-3 code as below,

6 + 3 = 0110 + 0011 = 1001
2 + 3 = 0010 + 0011 = 0101
7 + 3 = 0111 + 0011 = 1010

Combining all the Excess-3 codes together to obtain the final result,

$(627)_{10} = (1001\ 0101\ 1010)_{XS\text{-}3}$

Hence, the BCD number $(0110\ 0010\ 0111)_{BCD}$ is equivalent to the Excess-3 code $(1001\ 0101\ 1010)_{XS\text{-}3.}$

Example 2

Convert the BCD number 989 $(1001\ 1000\ 1001)_{BCD}$ into its equivalent Excess-3 code.

Solution − The given BCD number is,

$989 = (1001\ 1000\ 1001)_{BCD}$

Adding 3 (0011) to each BCD code to obtain the equivalent Excess-3 code as below,

$9 + 3 = 1001 + 0011 = 1100$
$8 + 3 = 1000 + 0011 = 1011$
$9 + 3 = 1001 + 0011 = 1100$

Combining all the Excess-3 codes to obtain the final result as below.

$(989)_{10} = (1001\ 1000\ 1001)_{BCD} = (1100\ 1011\ 1100)_{XS\text{-}3}$

Hence, the BCD number (1001 1000 1001)BCD is equivalent to the Excess-3 code $(1100\ 1011\ 1100)_{XS\text{-}3}$.

6. CONCLUSION

The 4-BIT BCD to XS-3 converter is a crucial component in digital systems that involve binary-coded decimal (BCD) representation. The XS-3 (Excess-3) code is a binary-coded decimal code that adds 3 to each decimal digit's binary representation. The purpose of the converter is to efficiently transform 4-bit BCD inputs into their corresponding XS-3 equivalents.

In conclusion, the 4-BIT BCD to XS-3 converter is designed to provide a seamless and accurate conversion between BCD and XS-3 representations. This conversion is essential in various applications, especially in digital arithmetic and communication systems. The converter enhances the efficiency and precision of digital circuits by ensuring that numerical data is represented in a format suitable for arithmetic operations and data transfer.

Through its systematic logic and circuitry, the converter can handle the conversion process for all possible 4-bit BCD input combinations. The reliable functionality of the converter contributes to the overall reliability and accuracy of digital systems utilizing BCD and XS-3 codes.

In summary, the 4-BIT BCD to XS-3 converter plays a vital role in digital electronics, facilitating the seamless conversion of BCD data to XS-3, thereby supporting the accurate processing of numerical information in various digital applications.

7. References

(as per the IEEE recommendations)

1. *A.P.Godse; D.A.Godse (2009). "3". Digital Logic Design. Technical Publications. pp. 9–3. ISBN 978-81-8431-738-1.*

2. Jump up to:*a b Leadership Education and Training (LET) 2: Programmed Text. Headquarters, Department of the Army. 2001. pp. 371–.*

3. Jump up to:*a b A.P.Godse; D.A.Godse (2009). "Appendix". Digital Logic Circuits. Technical Publications. pp. C–1. ISBN 978-81-8431-650-6.*

4. *"1. An Introduction to Computer Architecture - Designing Embedded Hardware, 2nd Edition [Book]". www.oreilly.com. Retrieved 2020-09-03.*

5. *Horowitz, Paul; Winfield Hill (1989). "14.1.1". The Art of Electronics (2nd ed.). Cambridge University Press. pp. 990–. ISBN 978-0-521-37095-0.*

6. *Philip Levis (November 8, 2004). "Jonathan von Neumann and EDVAC" (PDF). cs.berkeley.edu. pp. 1, 3. Archived from the original (PDF) on September 23, 2015. Retrieved January 20, 2015.*

7. *Lee Boysel (2007-10-12). "Making Your First Million (and other tips for aspiring entrepreneurs)". U. Mich. EECS Presentation / ECE Recordings. Archived from the original on 2012-11-15.*

8. Ken Shirriff. "The Z-80 has a 4-bit ALU. Here's how it works." 2013, righto.com

9. *Reif, John H. (2009), "Mechanical Computing: The Computational Complexity of Physical Devices", in Meyers, Robert A. (ed.), Encyclopedia of Complexity and Systems Science, New York, NY: Springer, pp. 5466–5482, doi:10.1007/978-0-387-30440-3_325, ISBN 978-0-387-30440-3, retrieved 2020-09-03*

10. Digital Design : With an Introduction to the Verilog HDL, VHDL, and System , Sixth Edition M. Morris Mano

8. Appendices

Justification of Architecture:

Binary Coded Decimal (BCD) Input Handling:
The architecture should be designed to handle 4-bit Binary Coded Decimal input. BCD is a binary representation of decimal numbers, where each decimal digit is represented by a 4-bit binary code. Ensuring that the converter can accurately process and interpret BCD inputs is fundamental to its functionality.

Excess-3 (XS-3) Output Generation:
The primary objective of the converter is to transform a 4-bit BCD input into its corresponding Excess-3 code. XS-3 is an offset binary code where each decimal digit is represented by adding 3 to the corresponding BCD code. The architecture should be capable of generating XS-3 output based on the given BCD input.

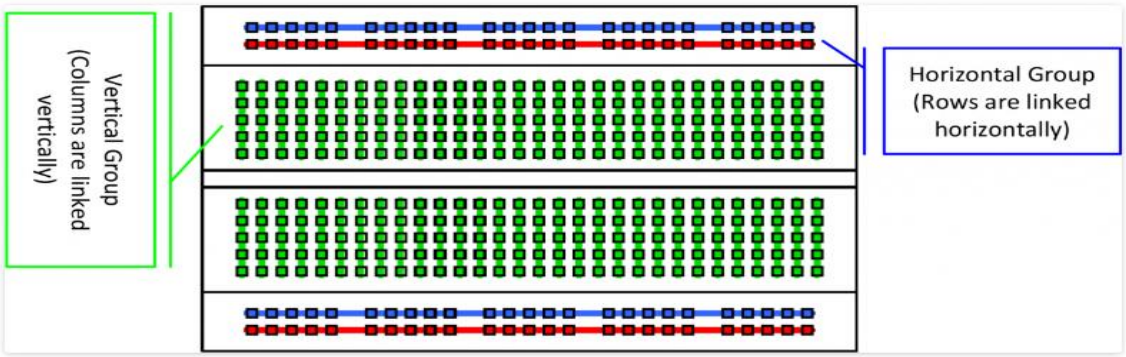
Logic Simplification for Conversion:
To ensure efficient and optimized operation, the architecture should incorporate logical simplifications. The use of appropriate combinational logic gates and techniques, such as Karnaugh maps, should be considered to streamline the conversion process and minimize the number of logic elements required.

Error Handling and Validation:
The converter's architecture should include provisions for error handling and validation. This may involve checking for invalid BCD inputs (values greater than 9) and implementing error correction or notification mechanisms to ensure the reliability of the conversion process.

Modularity and Expandability:
Designing the architecture with modularity and expandability in mind allows for scalability and ease of integration into larger systems. Each component of the converter, such as BCD input handling, XS-3 output generation, and error handling, should be well-defined and easily replaceable or expandable to accommodate future requirements or modifications.

Digital ICs And Devices used for Implementation

● BREADBOARD:



• AND GATE

AND gates are fundamental in creating logical conjunctions. They are used to implement the various terms in the Boolean expressions derived from the Karnaugh maps.

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised July 2001

DM7408 Quad 2-Input AND Gates

DM7408
Quad 2-Input AND Gates

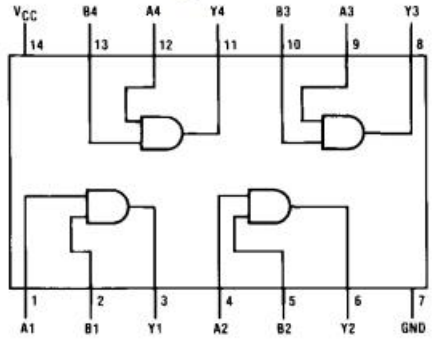
General Description

This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

• OR GATE:

OR gates are used for logical disjunctions. They combine the outputs from different AND gates to form the final output expressions.
The OR gate outputs "true" if any of its inputs are "true"; otherwise it outputs "false". The input and output states are normally represented by different voltage levels.

FAIRCHILD
SEMICONDUCTOR™

June 1986
Revised March 2000

DM74LS32 Quad 2-Input OR Gate

DM74LS32
Quad 2-Input OR Gate

General Description

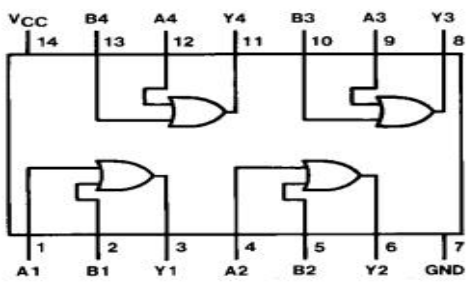
This device contains four independent gates each of which performs the logic OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = A + B

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

● NOT GATE

NOT gate, also known as an inverter, is a fundamental digital logic gate that can be utilized in the construction of a three-bit magnitude comparator circuit..

FAIRCHILD
SEMICONDUCTOR TM

August 1986
Revised February 2000

DM7404
Hex Inverting Gates

General Description

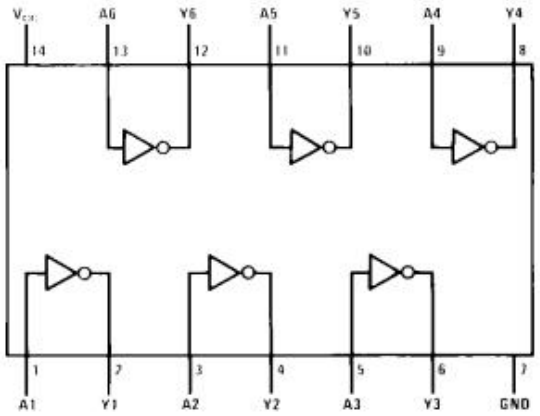
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level