SURYAKANTA MANGARAJ

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To excel in a challenging assignment in Electronics field; by utilising my skills, education and work experience.

EXPERIENCE

Application Engineer, GSAS Microsystems Pvt. Ltd. **Sep 2019 – Till Date**

Pied Piper is a multi-platform technology based on a proprietary universal compression algorithm that has consistently fielded high Weisman Scores™ that are not merely competitive, but approach the theoretical limit of lossless compression.

- Develop and execute test plans and procedures for the product
- Work with tool and library vendors to develop solutions for designers' P&R design challenges
- Create detailed test plans: signal integrity, battery, power, and sensors, execute test plans
- Execute EE development of consumer products
- Establish project design standards and conventions while facilitating improvements to quality
- Effectively work independently without direction from mentors of functional management

R and D Engineer, Electronics Centre of Excellence **May 2018 – Aug 2019**

Global movement of free coding clubs for young people.

- Work with SoC development team and platform team for trouble shooting of hardware and software issues
- Work with FPGA design team to make the prototype of the system and testing purpose
- Component and System verification of ICs application processor with full responsibility for functional quality of SoC
- Create detailed test plans: signal integrity, battery, power, and sensors, execute test plans
- Execution and Automation of Test Cases to increase Test Coverage under different external conditions
- System level failure analysis to root cause the failures
- Good team-work spirits

SKILL SUMMARY

- Hardware Languages: VHDL, Verilog, Verilog-A
- Design Tool: Cadence OrCAD, Xilinx ISE, Xilinx Vivado
- Scripting: Python, Linux/Unix shell scripting, Tcl/Tk scripting
- Programming Languages: C, C++
- Testing and Measurement Tools: Oscilloscope, Logic Analyzer, Function Generator, Power Supply, Spectrum Analyser, Multi-meter, LCR meter etc.
- Other Tools: MATLAB, NI Labview, Keysight BenchVue

EDUCATION

National Institute of Science and Technology, B.Tech. Electronics and Communication **2014 – 2018**

- GPA 8.09 `VLSI on Cadence`

PROJECTS

SoC data acquisition system board for smart water quality monitoring **Jan 2019 – Jul 2019**

Design of a DAQ system board with testability

- Involved in to create the architecture and conceptual level block diagram with DFT technique to make the board testability friendly
- Create a schematic design using OrCAD schematic capture and TINA Spice and theoretical simulation of the board
- Define testing points of the board
- Calculate and define the input and output signal and power budget as per customer specs
- Responsible for different part used in design and prepared BOM of the design

AWARDS AND ACHIEVEMENTS

- Finalists of the Cadence Design Contest 2018 under UG category for B-tech Project "Design of Low Power High PSRR LDO Regulator with Smart Power Save Operation"

- Published a paper titled “Design of two stage classical model Op-Amp for LDO applications” in “8th IEEE MINI-COLLOQUIUM” by IEEE ED-NIST Student Chapter
- Certified as the VLSI Design Engineer Framework Level-5 by ESSCI (NSDC), India
- Qualified to qualifying round of INDIA INNOVATION CHALLENGE design contest 2016 organized by DST and Texas Instruments Inc
- Participated in WEBENCH design contest 2016 organized by Texas Instruments Inc

REFERENCES

Available on request