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Report on

'Analysis of Power Optimization Technique of Level Shifter for Multi Supply Voltage Design'

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Table of contents

LIST OF FIGURES

1. Introduction and Block Diagram

In digital electronics, a **level shifter**, also called **level converter** or **logic level shifter**, or **voltage level translator**, is a circuit used to translate signals from one logic level or voltage domain to another, allowing compatibility between integrated circuits with different voltage requirements, such as TTL and CMOS. Modern systems use level shifters to bridge domains between processors, logic, sensors, and other circuits. In recent years, the three most common logic levels have been 1.8V, 3.3V, and 5V, though levels above and below these voltages are also used.

Since level shifters are used to resolve the voltage incompatibility between various parts of a system, they have a wide range of applications as well. Level shifters are widely used in interfacing legacy devices and also in SD cards, SIM cards, CF cards, audio codecs and UARTs.

Level shifters are also widely used in gate driver circuits used in power management ICs. In these applications, **level shifter translates the control logic signal to high voltages used in driving power MOSFETs.**

Hence, Voltage level shifter is a device which converts one voltage level to another. Voltage level shifters are used to interface various circuit blocks operating at different supply voltages.

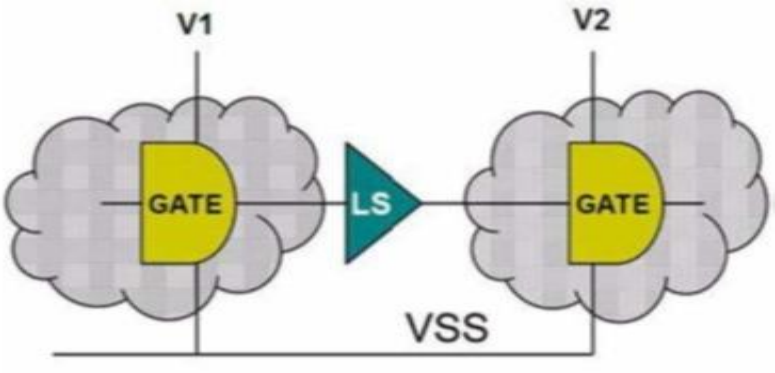

Figure 1: Example of a Level Shifter

As the demand of battery-operated devices like cell phones, laptops, tablets etc. is increasing, low power consumption has become major concern for circuit design . Low power application devices operate efficiently in sub threshold region . There are two types of power consumption: static and dynamic power consumption. Dynamic power dissipation is mainly due to the charging and discharging of the load capacitor. Power consumption can be reduced by reducing the supply voltage since we know the relation between dynamic power and voltage and that voltage has a quadratic effect on the power

$$\boldsymbol{P = \alpha C V^2 f}$$

Multi-supply voltage domain technique is effective method to reduce power dissipation. In this technique, the design is partitioned into separate voltage domains, where each domain is operating at distinct power supply levels.

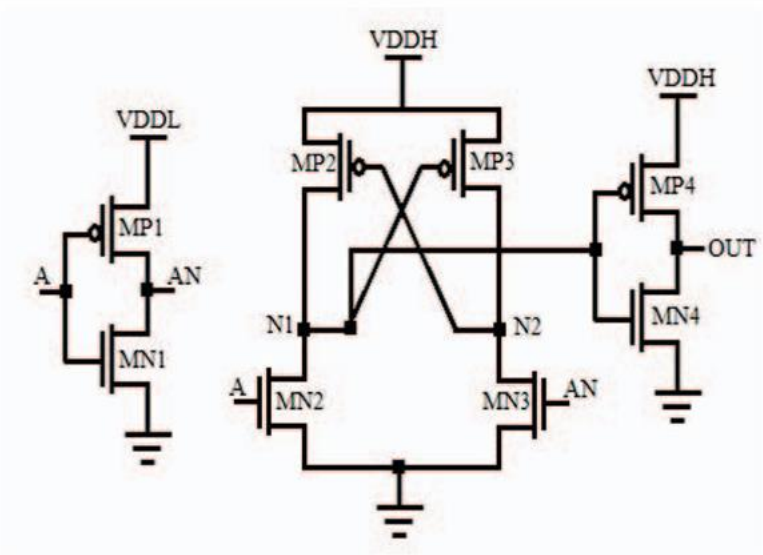

Figure 2: Conventional Level Shifter

The conventional voltage level shifter is depicted in Fig. 2. It consists of input inverter operating at VDDL and the cross coupled PMOS half latch operating at VDDH.

Let us now look into how this Conventional Level Shifter Works:

- When input A is high
- MN2 and MP3 turns on and,
- Rises voltage at node N1 is pulled to ground and N2 is pulled down to Vdd.
- Also, this turns on MP4 and OUT rises to VDDH.

So, basically here our Input is given in a Low Voltage Domain and Output is obtained in a high voltage domain. This is what exactly level shifter does.

Voltage level shifter is a circuit which converts the signal from one voltage level to another. To interface various domains in multi-supply voltage design, voltage level shifter is used.

But there is contention at node N1 and N2 between pull-down devices operating at VDDL and pull-up devices operating at VDDH. **Thus, conventional level shifter cannot operate correctly when difference between values of VDDH and VDDL is large.**

So, the problem statement becomes "*Analysis of power optimization technique of level shifter for multi supply voltage design"*

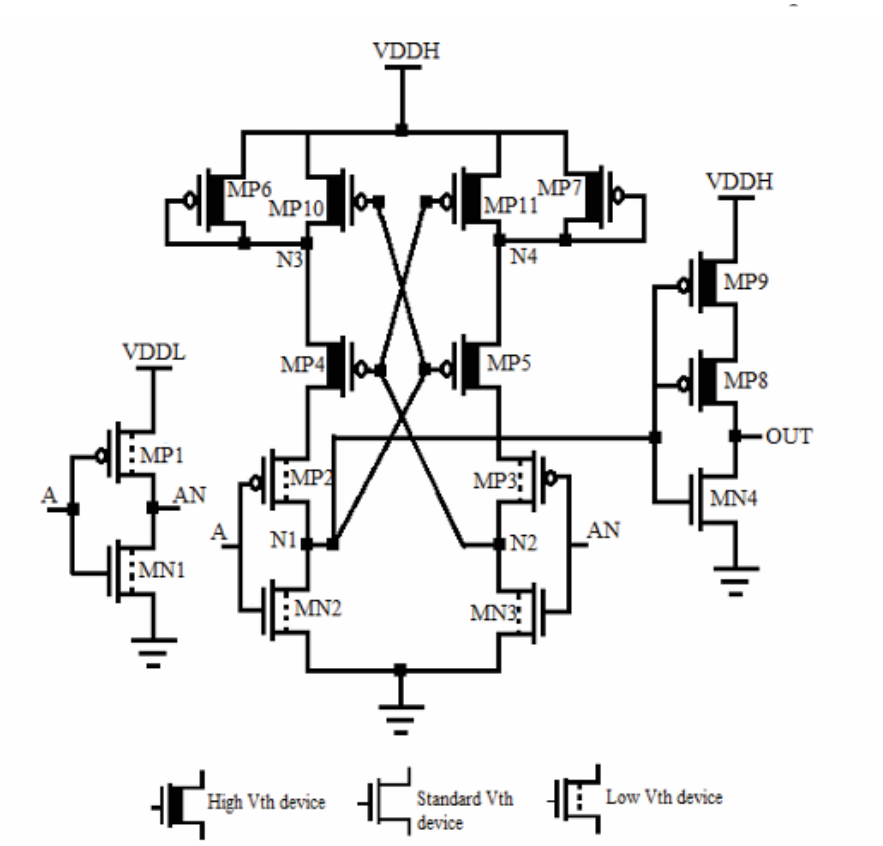

Figure 3: Proposed Level Shifter

The schematic of proposed voltage level shifter is shown in Fig. 3. It uses multi-threshold voltage CMOS technique.

Transistors MN1, MN2, MN3, MP1, MP2 and MP3 are low threshold voltage transistors (LVT). Transistors MP4 to MP11 are high threshold transistors (HVT) and MN4 is standard threshold voltage transistor (SVT).

The design operates with two supply voltages VDDL and VDDH. HVTs MP4 and MP5 are used to reduce leakage current flowing through pull-up network, when MP4 and MP5 are off. Since HVTs reduces transition at the nodes, the parallel connected transistors MP6 MP10 and MP7-MP11 are used to reduce switching delay at nodes N1 and N2.

Transistors MP10 and MP11 are sized to reduce leakage current flowing through node N1 and N2. The current at node N1 is significantly reduced by serially connected HVTs MP8, MP9 and SVT MN4.

WORKING OF THE PROPOSED LEVEL SHIFTER:

When the input signal A is low and AN is high, the voltage level at node N1 is high and at N2 it is low. Transistors MP5 and MP10 are turned off, thus voltage at node N3 is lower than VDDH by saturation voltage of MP6, since it is a diode connected transistor.

Also MP4 and MP11 are turned on and voltage at node N4 is equal to VDDH. As node N1 is high, it will turn on MN4 due to which output node is connected to ground. When input A rises from low to

high, node N1 discharges while node N2 starts to charge by voltage at node N4.Transistor MP4 turns off and thus discharging of node N1 accelerates further. Transistor MP5 turns on after complete discharge of node N1. Thus, voltage at node N3 is VDDH after transition at input A and at N4 voltage level is lower than VDDH by saturation voltage of MP7. Since, N1 is pulled down to ground; it will turn on transistor MP8 and MP9, thus node OUT raises to VDDH.

TRANSISTOR SIZES

Transistor	Value (W/L)	Transistor	Value (W/L)
MN1	0.3 µm/0.1 µm	MP5	0.18 µm/0.2 µm
MN2	1.5 µm/0.2 µm	MP6	0.3 µm/0.2 µm
MN3	0.5 µm/0.2 µm	MP7	0.18 µm/0.2 µm
MN4	0.36 µm/0.2 µm	MP8	0.6 µm/0.2 µm
MP1	0.45 µm/0.1 µm	MP9	0.6 µm/0.2 µm
MP2	0.3 µm/0.2 µm	MP10	0.12 µm/0.2 µm
MP3	0.18 µm/0.2 µm	MP11	0.12 µm/0.2 µm
MP4	0.3 µm/0.2 µm		

Figure 4: Transistor Sizes

2. Schematic and Simulation Results

⇨ **SIMULATION:**

Conventional Level Shifter Schematic:

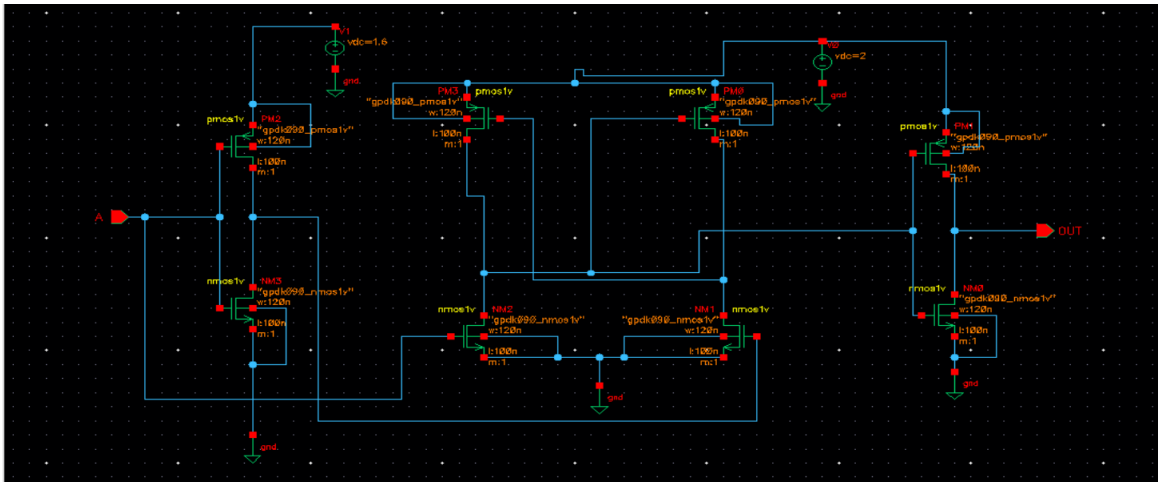

Figure 5: Conventional Level Shifter Schematic

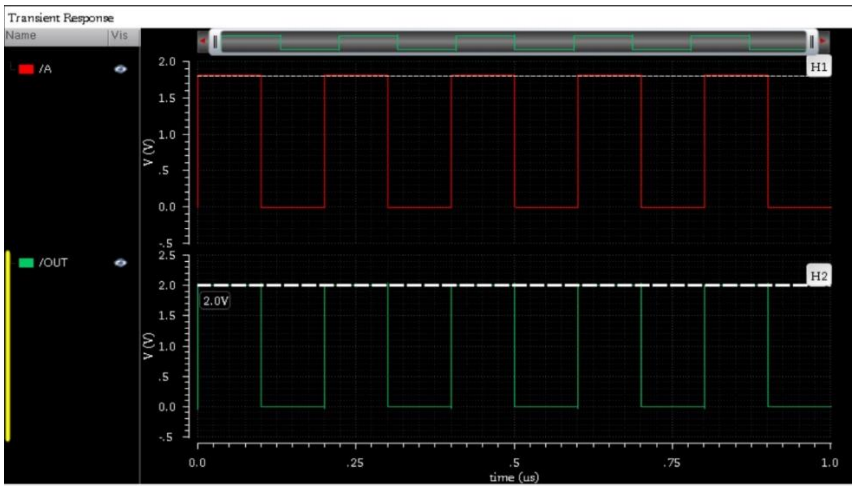

Figure 6: Output of the Conventional Level Shifter

Average Power (obtained from the CADENCE tool) : 1.61246 uW

Proposed Level Shifter Schematic:

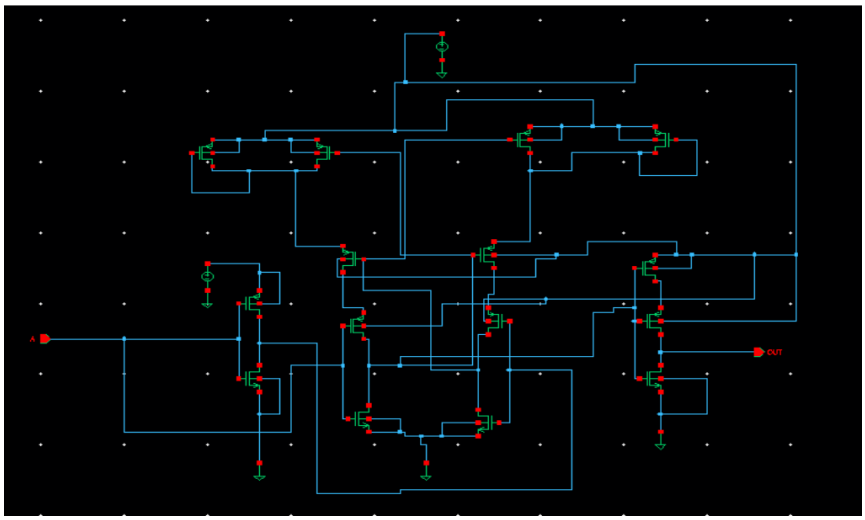

Figure 7: Proposed Level Shifter Schematic

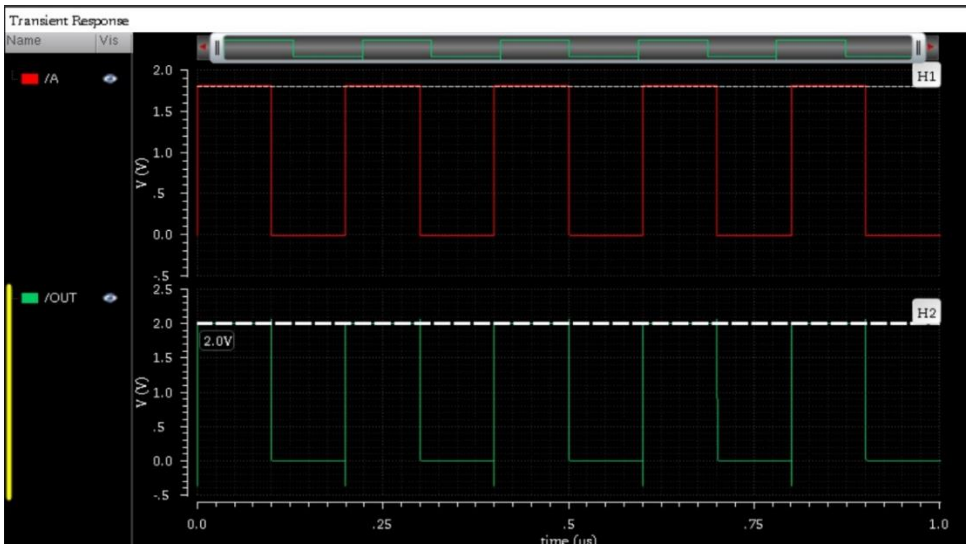

Figure 8: Output of the Proposed Level Shifter Schematic

Average power (obtained from CADENCE tool) : 942.698 nW
As we can observe, we can see that with the use of Multi Vt cells and Multi Vdd cells there is an optimization in power which was calculated up to 41.6% from the conventional circuit.

3. Conclusion

INFERENCE:

- Because of the weak pull-up pmos network(MP6 and MP7), nodes N3 and N4 will always be at VDDH. So, When A is high N1 is pulled to ground and N2 is pulled to VDDH, which would be ready for the next transistion to happen.
- During the transition this node would help in controlling VDDH getting shorted with ground which reduces total avg.power
- Since using HVT cells, which contributes to decrease in leakage current , hence dissipates less leakage power, hence overall avg, power is decreased as shown in the simulation results.

APPLICATIONS:

- Voltage level shifters are used to interface various circuit blocks operating at different supply voltages, particularly at the boundaries of different voltage islands on a system-on-chip (SoC).
- Additionally, voltage level shifters are used in applications such as 2:1 multiplexers and static random access memory (SRAM) cells to enable the storage and transfer of data between circuits operating at different supply voltages.

CONCLUSION:

- We have successfully analyzed the power optimization technique of Level Shifter for multi supply voltage design using cadence virtuoso.
- We have successfully learnt the role of Multi Vth and Multi Vdd cells in designs for enhanced power optimization .
- Also learnt how Aspect Ratio played a key role in altering the threshold voltage of CMOS transistors.

4. References

[1] P. Gosatwar and U. Ghodeswar, "Design of voltage level shifter for multi-supply voltage design," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, 2016, pp. 0853-0857, doi: 10.1109/ICCSP.2016.7754267.