Indian Institute of Technology Kharagpur

AUTUMN Semester, 2021
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Laboratory Test–2 (Version–2 [for even roll numbers])

Full Marks: 20

Time allowed: 2 hours

INSTRUCTIONS: Every student should make one submission in the form of a single zipped folder containing his/her Verilog source code files(s) and Verilog testbench. Name your submitted zipped folder as `CT_Ver_2_<Roll_no>.zip`. Inside each submitted source and testbench file, there should be a clear header describing the name and roll number of the submitting student. Liberally comment your code to improve its comprehensibility.

1. [**Unsigned Binary Fraction Multiplier**] Consider the iterative multiplication of two n-bit unsigned fractions, $X = 0.x_1x_2x_3\cdots x_{n-1}$ and $Y = 0.y_1y_2y_3\cdots y_{n-1}$, with numerical values $X = \sum_{j=1}^{n-1} x_j 2^{-j}$ and $Y = \sum_{j=1}^{n-1} y_j 2^{-j}$ (e.g. 0.111 in binary has the numerical value $0.5+0.25+0.125 = 0.875$), to form the $(2n-1)$-bit product $P = 0.p_1p_2p_3\cdots p_{2n-2} = X \cdot Y$. An iterative scheme for this multiplication proceeds, in the i-th iteration, as:

$$P_i = P_i + Y x_{n-1-i} \quad \text{and} \quad P_{i+1} = 2^{-1}P_i \tag{1}$$

with $P_0 = 0$ and $P_{n-1} = P$. Design (using Verilog) and simulate an **7-bit (i.e. $n = 7$) binary sequential unsigned fraction multiplier** following the scheme of Eqn. (1). Include a proper Verilog testbench to simulate it. The interface of your design should be:

```
module bin_frac_seq_mult (input clk, input start, input [6:0] a, input [6:0] b, output
done, output [11:0] product);
```

Note that you need not consider the leading "0" in the input operands or the product. Your input operand/output product bus-widths will change accordingly. Both variants (if correct) are acceptable.

It is suggested that you modularize your design, to clearly differentiate between the data path and the control path. (20 marks)