COAA Lab Assignment - 1

Group Members

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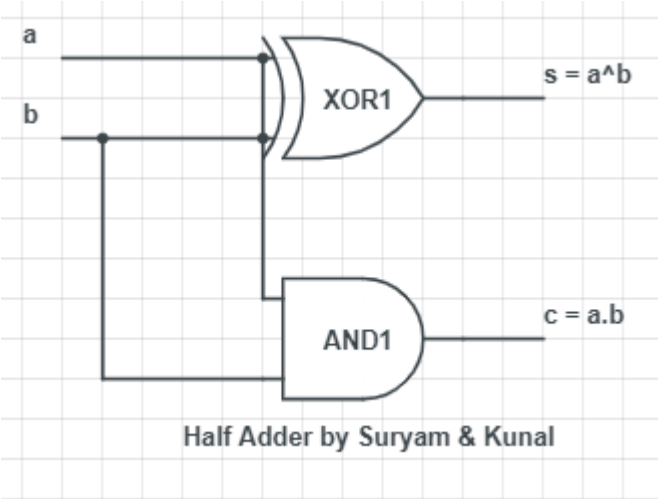
Half Adder

Truth Table

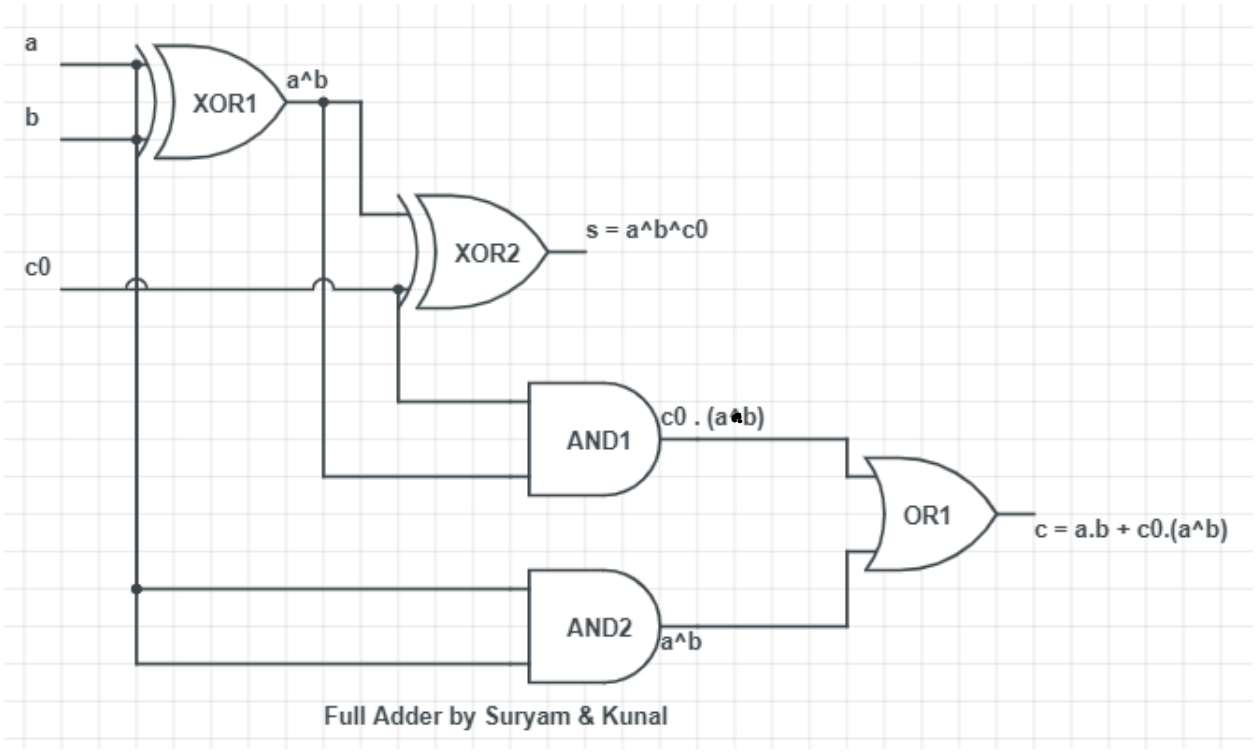
a	b	s	c
0	0	0	0
0	1	1	0
1	1	0	1
1	0	1	0

Circuit Diagram



Full Adder

Circuit Diagram

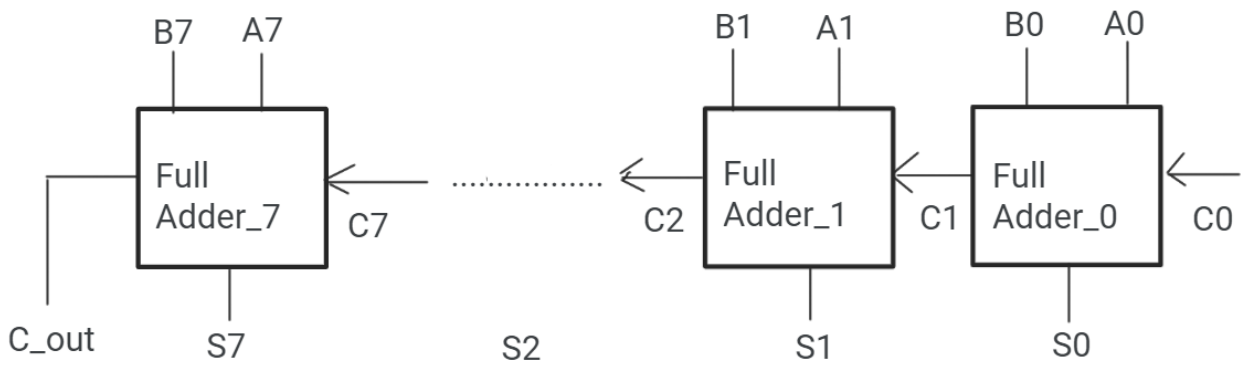


Truth Table

a	b	c0	s	c
0	0	0	0	0
0	1	0	1	0
1	1	0	0	1
1	0	0	1	0
0	0	1	1	0
0	1	1	0	1
1	1	1	1	1
1	0	1	0	1

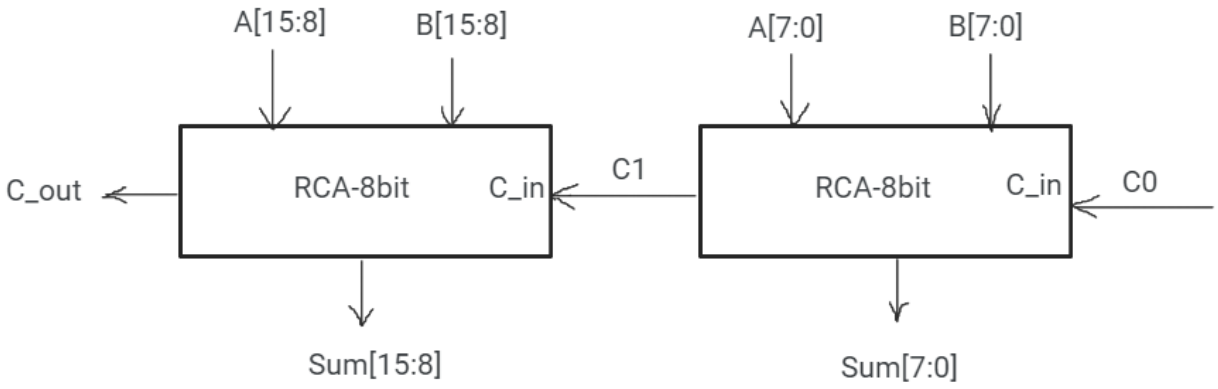
Longest Delays in Circuits

1) The longest delay in 8-bit RCA was **6.088 ns** with the path going from B_in[0] to sum[7]



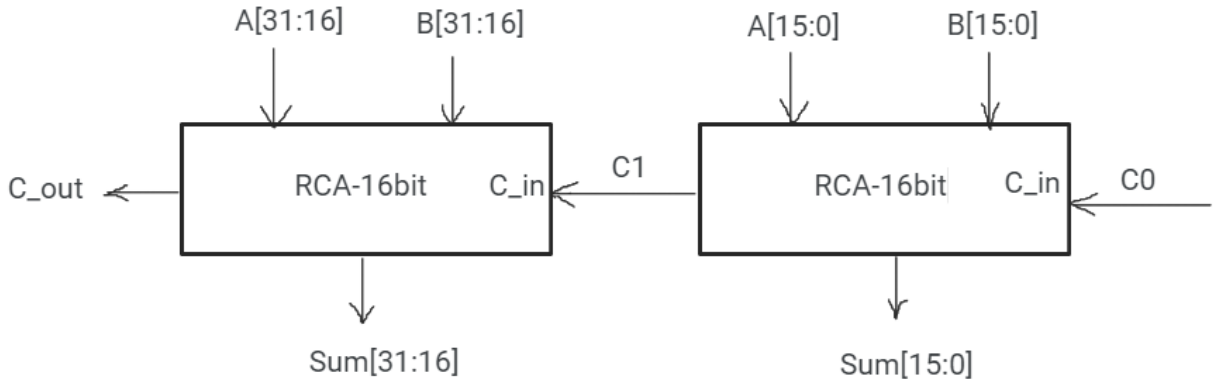
RCA-8bit

2) The longest delay in 16-bit RCA was **11.416 ns** with the path going from B_in[0] to sum[15]



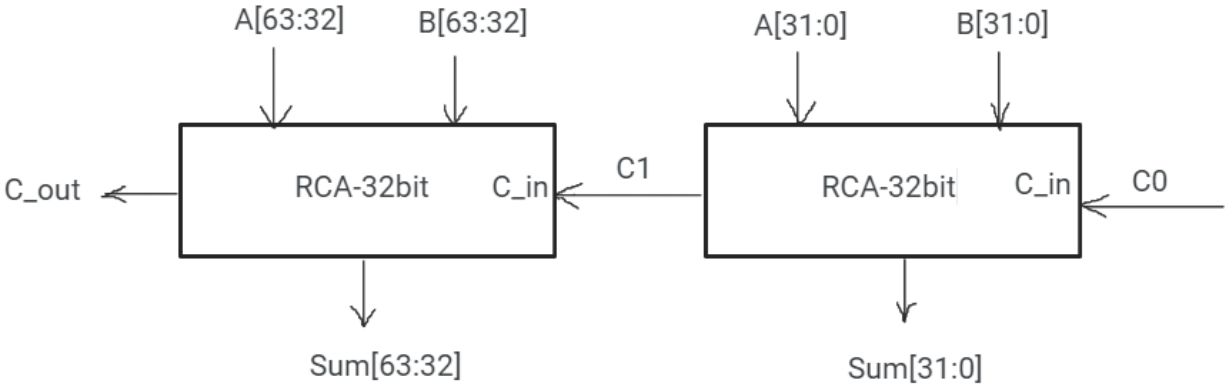
RCA-16bit

3) The longest delay in 32-bit RCA was **22.072 ns** with the path going from B_in[0] to sum[31]



RCA-32bit

4) The longest delay in 64-bit RCA was **43.384 ns** with the path going from B_in[0] to sum[63]



RCA-64bit

The reason for such long delays is the fact that the carry is rippled into the next adder due to which the next adder has to wait for the computation of carry from the previous adder.

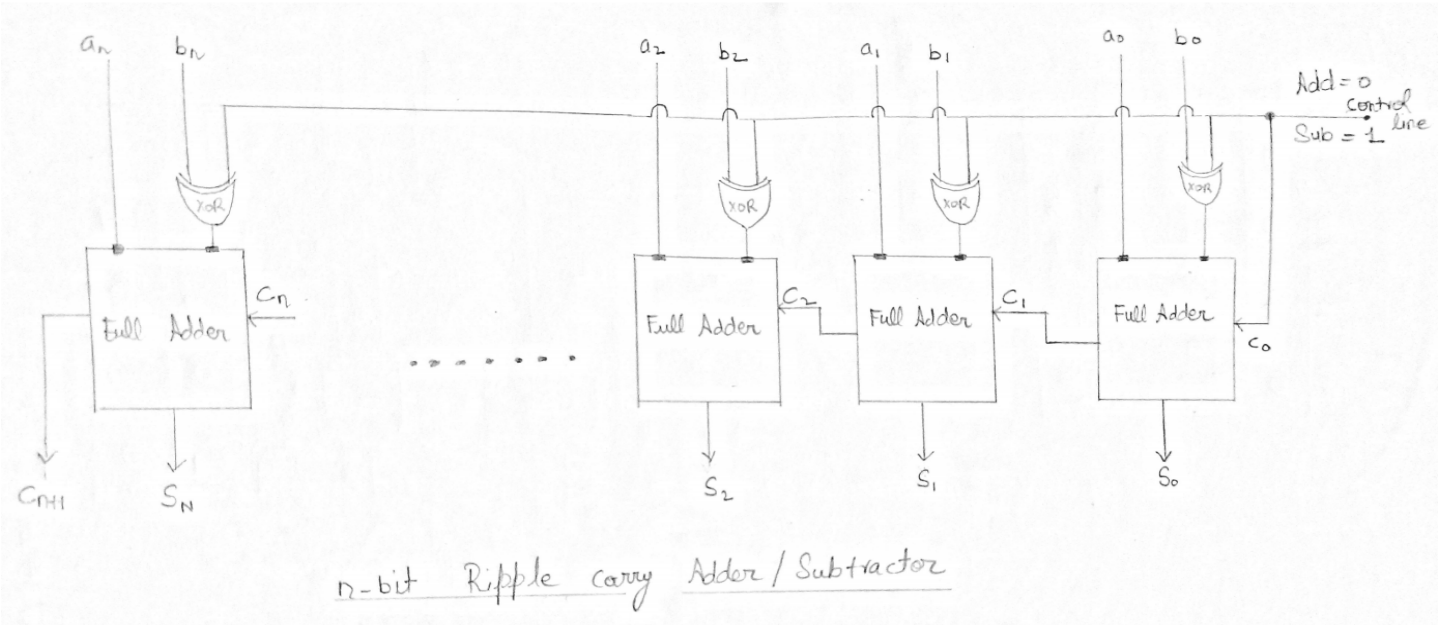
Difference between two n-bit numbers

When we need to compute a-b , then this is equivalent to a + (-b).
We can obtain (-b) in the 2's complement representation = 1's complement of b + 1

So, we can keep a control line which represents Addition as 0 and Subtraction as 1.
To flip the bits we can use an XOR gate for each bit since x^0 = x and x^1 = complement of x.

The same control line can be passed to the carry-in bit as well since for subtraction we need to add an extra 1.
Therefore, we can keep an xor gate for each bit of the input b and keep the control line as the second input to the xor gate.

The circuit is attached below for more reference.



Equations for CLA 4-bit

1) The equations for the propagate signals P are as shown below:

P0 = A[0] xor B[0]
P1 = A[1] xor B[1]
P2 = A[2] xor B[2]
P3 = A[3] xor B[3]

2) The equations for the generate signals G are as shown below:

G0 = A[0] & B[0]
G1 = A[1] & B[1]

G2 = A[2] & B[2]
G3 = A[3] & B[3]

3) The equations for the carry signals C are as shown below:

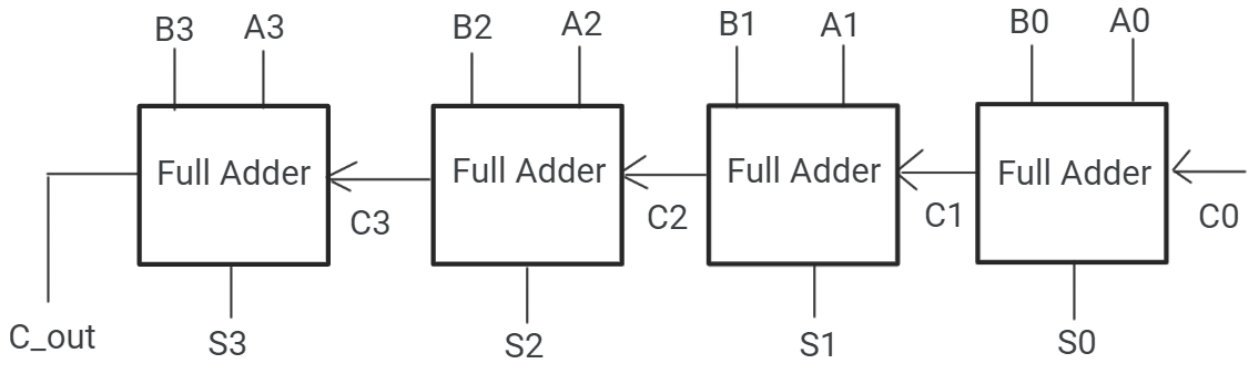
C1 = G0 + P0C0
C2 = G1 + P1G0 + P1P0C0
C3 = G2 + P2G1 + P2P1G0 + P2P1P0C0
C4 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C0

4) The equations for the sum signals S are as shown below:

Sum[0] = P0 xor C0
Sum[1] = P1 xor C1
Sum[2] = P2 xor C2
Sum[3] = P3 xor C3

Synthesis Report of 4-bit CLA and 4-bit RCA and their speed comparison

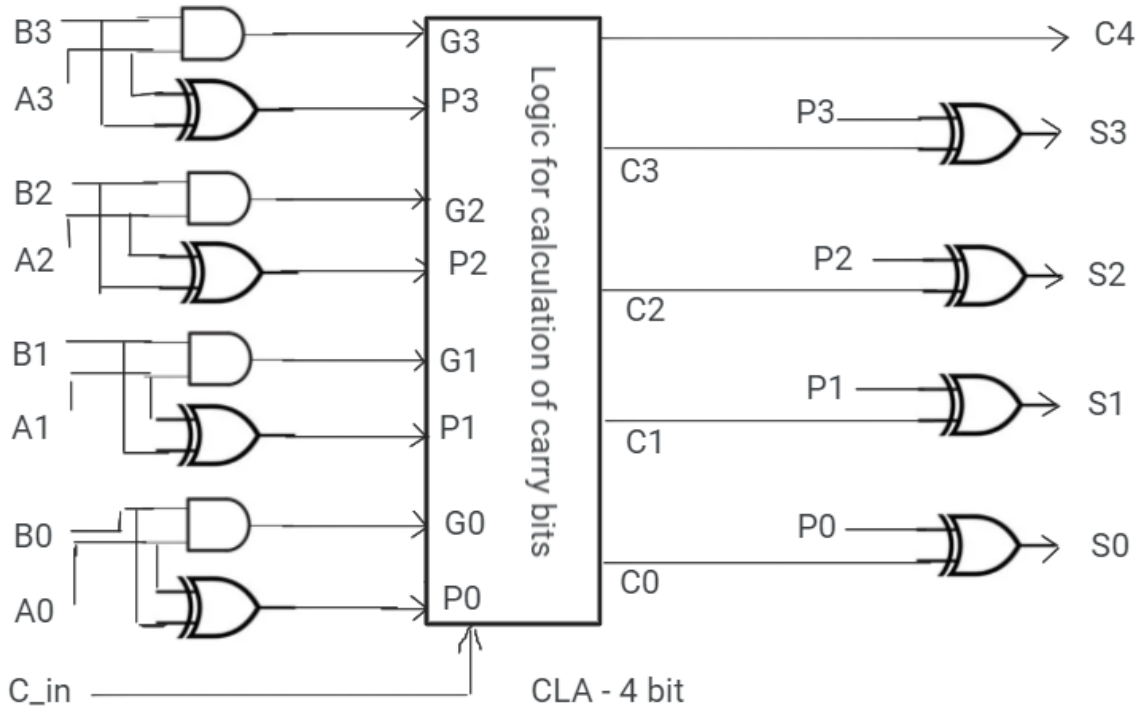
1) The RCA 4-bit takes **3.424 ns** as the maximum combinational path delay with the path going from B_in[0] to sum[3]



RCA-4bit

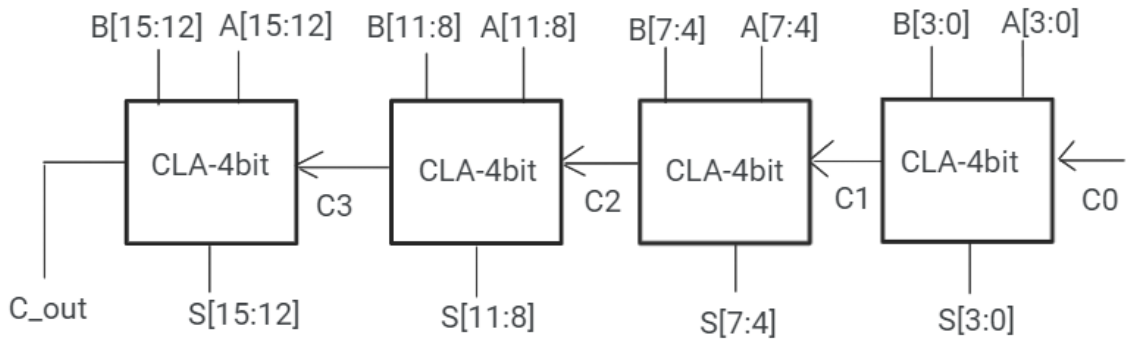
2) The CLA 4-bit without P and G as output takes **2.123 ns** as the maximum combinational path delay with the path going from A[1] to sum[3]

3) The CLA 4-bit with P and G as output takes **2.363 ns** as the maximum combinational path delay with the path going from B[1] to P



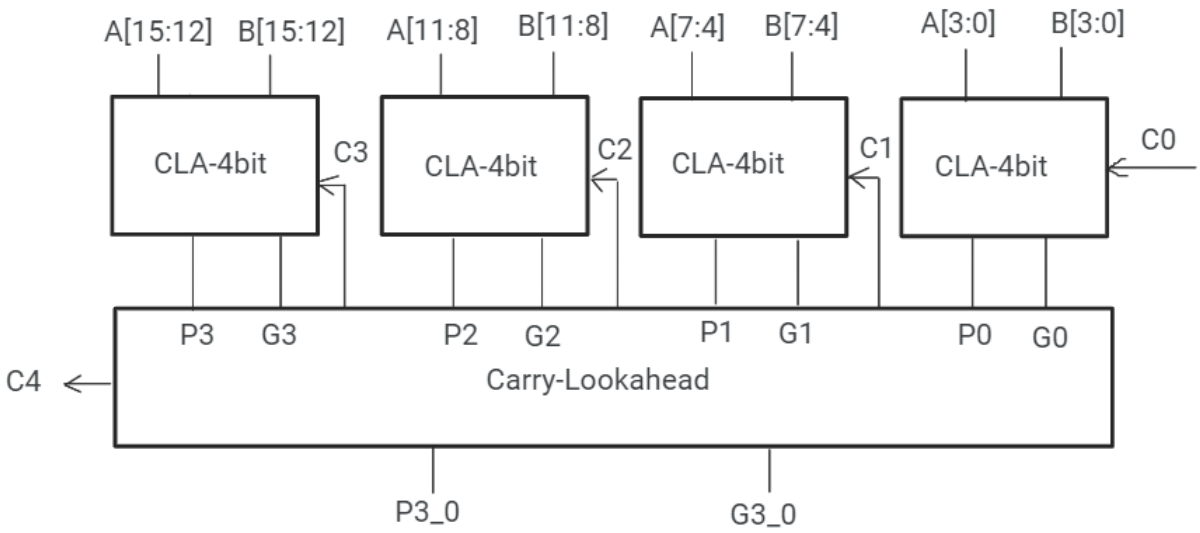
Delays for obtaining sum and carry-out bits for 16-bit CLA

1) When the carry is rippled in the maximum combinational path delay is **6.167 ns** with the path going from A_in[1] to sum[15]



CLA-16bit with ripple carry

2) When the carry is calculated using another lookahead carry unit the maximum combinational path delay is **5.229 ns** with the path going from B_in[1] to sum[15]



CLA-16bit with lookahead unit for carry calculation

Comparison of 16-bit CLA with a 16-bit RCA

We can see that the maximum time delay for the 16-bit RCA is 11.416 ns because the 16-bit RCA uses two 8-bit RCA which further use 8-FullAdder Cascaded in Series in which the next FullAdder has to wait for the carry from the previous FullAdder. Due to this rippling of the carry bit this circuit takes a lot of time.

For the CLA-16 bit as well, we can observe that the CLA in which the carry is rippled in is slower than the CLA in which the carry is calculated using another lookahead carry unit due to the same reason as the next CLA-4 bit needs to wait for the carry from the previous CLA-4 bit in the CLA-16 bit adder in which the carry is rippled in.

The speed comparison of the adders is given below:

CLA-16 bit with lookahead carry unit < CLA-16 bit with carry rippled in < RCA-16 bit

The total LUT units for the CLA 16-bit with lookahead carry unit is 44 with the following break-up:
LUT2 = 2 , LUT3 = 10, LUT4 = 9, LUT5 = 21 , LUT6 = 2.

The total I/O buffers for the CLA 16-bit with lookahead carry unit is 52 with the following break-up:
IBUF = 33, OBUF = 19

The total LUT units for the CLA 16-bit with carry rippled in is 24 with the following break-up:
LUT3 = 8, LUT5 = 16.

The total I/O buffers for the CLA 16-bit with carry rippled in is 50 with the following break-up:
IBUF = 33, OBUF = 17

The total LUT units for the RCA 16-bit is 32 with the following break-up:
LUT3 = 42

The total I/O buffers for the RCA 16-bit is 50 with the following break-up:
IBUF = 33, OBUF = 17

So, the LUT cost follows the order:
CLA 16-bit with carry rippled in < RCA 16-bit < CLA 16-bit with lookahead carry unit