

# DIGITAL LOGIC DESIGN LAB (EET1211)

## **LAB IV: Introduction to VHDL and Design of combinational circuits using VHDL**

Siksha 'O' Anusandhan (Deemed to be University), Bhubaneswar

Branch: CSE	Section: 2341211	Subgroup No.: 07
Name	Registration No.	Signature
Suryamadhab Moharana	2341013398	Suryamadhab Moharana

Marks: \_\_\_/10

Remarks:

Teacher's Signature

## I. OBJECTIVE:

1. Design, construct and test Half-Adder and Half-Subtractor circuit.
2. Design, construct and test a Full-Adder circuit.
3. Design, construct and test a 2-bit Parallel Adder circuit.

## II. PRE-LAB:

Objective-1 :

- a) Obtain the truth table.
- b) Derive the minimized Boolean expression for each output of the circuit.
- c) Draw the logic diagram of the circuit.
- d) Write VHDL code.

Ans a) Half-Adder:

a	b	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

### Half-subtractor:

a	b	diff	borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

### b) Half-Adder:

$$\begin{aligned} \text{sum} &= \sum m(1, 2) \\ &= \bar{A}B + A\bar{B} \\ &= A \oplus B = A \text{ xor } B \end{aligned}$$

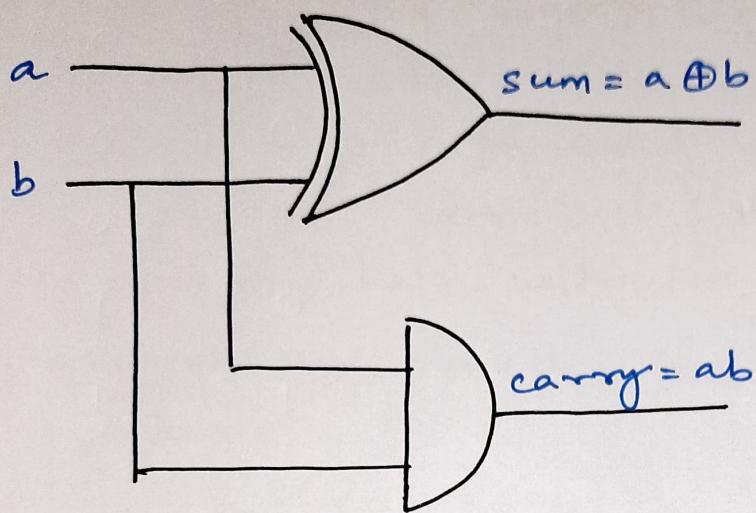
$$\begin{aligned} \text{carry} &= \sum m(3) \\ &= AB = A \text{ and } B \end{aligned}$$

### for Half-subtractor:

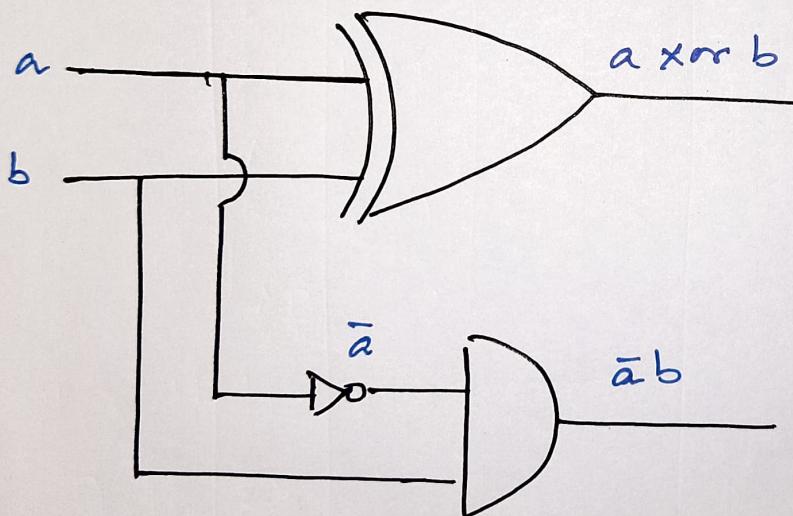
$$\begin{aligned} \text{diff} &= \sum m(1, 2) \\ &= \bar{A}B + A\bar{B} \\ &= A \oplus B = A \text{ xor } B \end{aligned}$$

$$\begin{aligned} \text{borrow} &= \sum m(1) \\ &= \bar{A}B = (\text{not } A) \text{ and } B. \end{aligned}$$

c) For Half-Adder:



For half-subtractor:



d)

```
entity half_subtractor is
    Port ( a : in STD_Logic;
            b : in STD_Logic;
            diff : out STD_Logic;
            borrow : out STD_Logic );
```

```
end half_subtractor;
```

```
architecture dataflow of half_subtractor is
```

```
begin
```

```
    diff <= a xor b;
```

```
    borrow <= (not a) and b;
```

```
end dataflow;
```

### Objective-2 :

- Obtain truth table.
- Derive the minimized Boolean expression for each output of the circuit.
- Draw the logic diagram for the circuit.
- Write VHDL code.

Ans. a)

a	b	c	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

b)  $S = \sum_m (1, 2, 4, 7)$ .

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A(B \odot C)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$= A \oplus B \oplus C.$$

Carry =  $\sum_m (3, 5, 6, 7)$

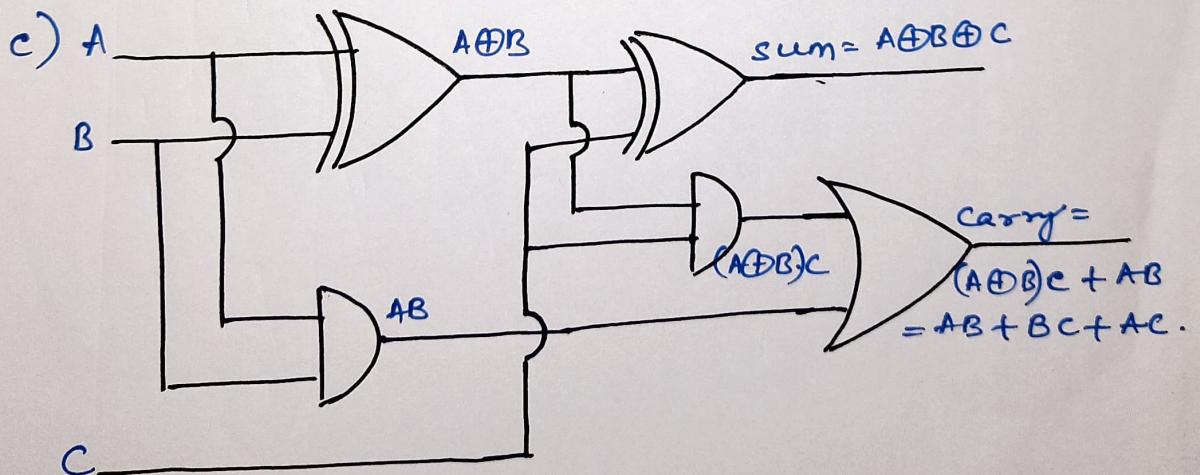
$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + ABC + A\bar{B}C + AB\bar{C}$$

$$= BC(\bar{A} + A) + A\bar{B}C + AB\bar{C}$$

$$= BC + AB + AC$$

$$= AB + BC + AC.$$



d)

```
entity full-adder is
Port ( a : in STD-Logic ;
       b : in STD-Logic;
       c : in STD-Logic;
       sum: out STD-Logic;
       carry: out STD-Logic);
end full-adder;
```

architecture of full-adder is

begin

sum <= a xor b xor c;

carry <= (a and b) or (b and c) or (a and c);

end dataflow

Objective-3.

- Obtain the truth table.
- Derive the minimized Boolean expression for each output of the circuit.
- Draw the logic diagram for the circuit.
- Write VHDL code.

Ans.

a)

$a_1$	$a_0$	$b_1$	$b_0$	$C_a$	$S_1$	$S_0$
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

$$b) S_1 = \sum m(2, 3, 5, 6, 8, 9, 12, 15).$$

$a_1, a_0$	$b_1 b_0$	$\bar{b}_1 \bar{b}_0$	$\bar{b}_1 b_0$	$b_1, b_0$	$b_1 \bar{b}_0$
$\bar{a}_1, \bar{a}_0$		0	1	3	2
$\bar{a}_1, a_0$		4	5	7	6
$a_1, \bar{a}_0$		12	13	15	14
$a_1, a_0$		8	9	11	10

$$S_1 = a_1 \oplus b_1 \cdot \bar{a}_1 \quad \text{--- } ①$$

$$S_0 = \sum m(1, 3, 4, 6, 9, 11, 12, 14).$$

$a_1, a_0$	$b_1 b_0$	$\bar{b}_1 \bar{b}_0$	$\bar{b}_1 b_0$	$b_1, b_0$	$b_1 \bar{b}_0$
$\bar{a}_1, \bar{a}_0$		0	1	3	2
$\bar{a}_1, a_0$		4	5	7	6
$a_1, \bar{a}_0$		12	13	15	14
$a_1, a_0$		8	9	11	10

$$\therefore S_0 = a_1 \oplus a_0 \oplus b_0$$

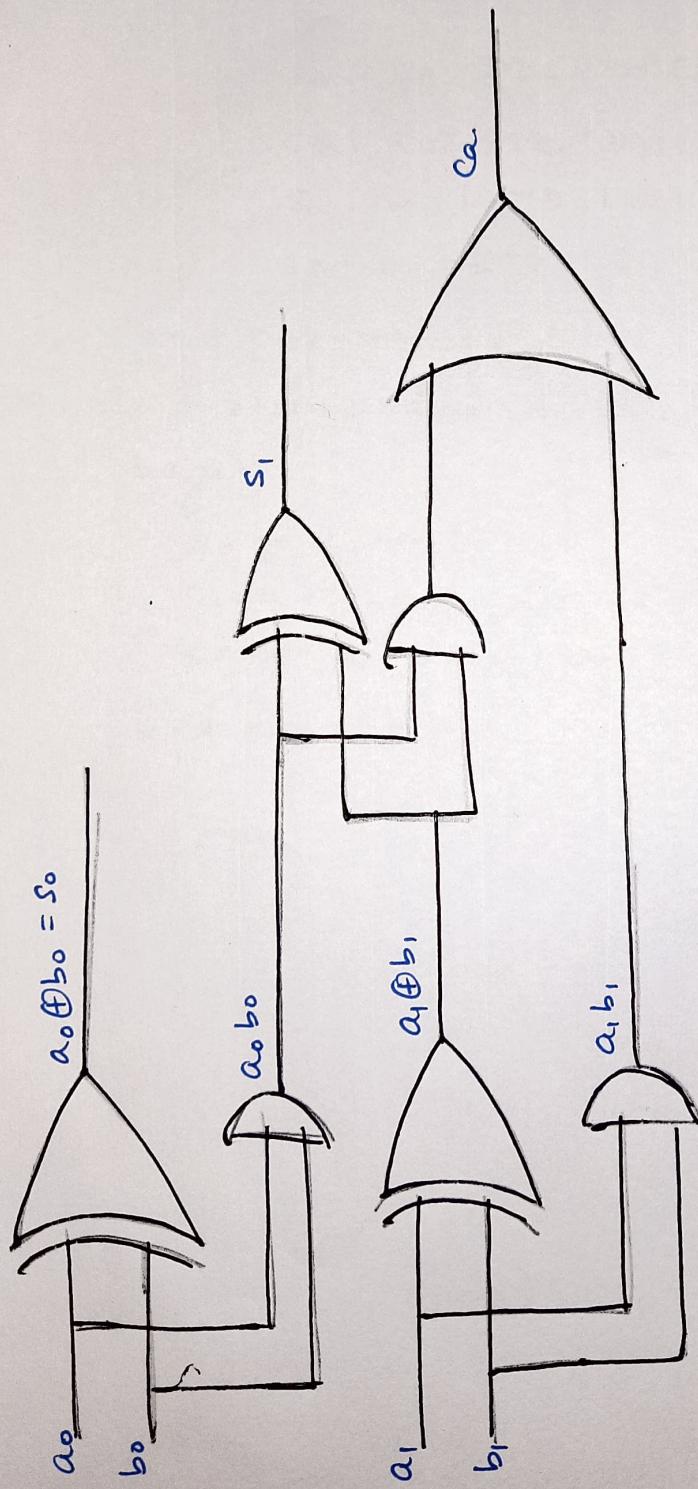
$$ca = \sum_m (7, 10, 11, 13, 14, 15)$$

$a_1 a_0$	$b_1 b_0$	$\bar{b}_1 b_0$	$b_1 \bar{b}_0$	$\bar{b}_1 \bar{b}_0$	
$\bar{a}_1 \bar{a}_0$	•	1	3	2	
$\bar{a}_1 a_0$	4	5	7	6	
$a_1 a_0$	12	13	15	14	
$a_1 \bar{a}_0$	8	9	11	10	

$$\therefore ca = a_1 b_1 + b_1 c_0 + a_0 c_0.$$

$$ca = (a_1 b_0) \oplus a_0 b_0 + a_1 b_1$$

c)



d)

entity parallel-adder is

```
Port (a1: in STD-LOGIC;  
      a0: in STD-LOGIC;  
      b1: in STD-LOGIC;  
      b0: in STD-LOGIC;  
      ca: out STD-LOGIC;  
      s1: out STD-LOGIC;  
      s0: out STD-LOGIC);
```

end parallel-adder;

architecture dataflow of parallelAdder is

begin

$s_0 \leftarrow a_0 \text{ xor } b_0;$

$s_1 \leftarrow a_1 \text{ xor } b_1 \text{ xor } a_0 b_0;$

$ca \leftarrow ((a_0 \text{ and } b_0) \text{ and } (a_1 \text{ xor } b_1)) \text{ or } (a_1 \text{ and } b_1);$

end dataflow;

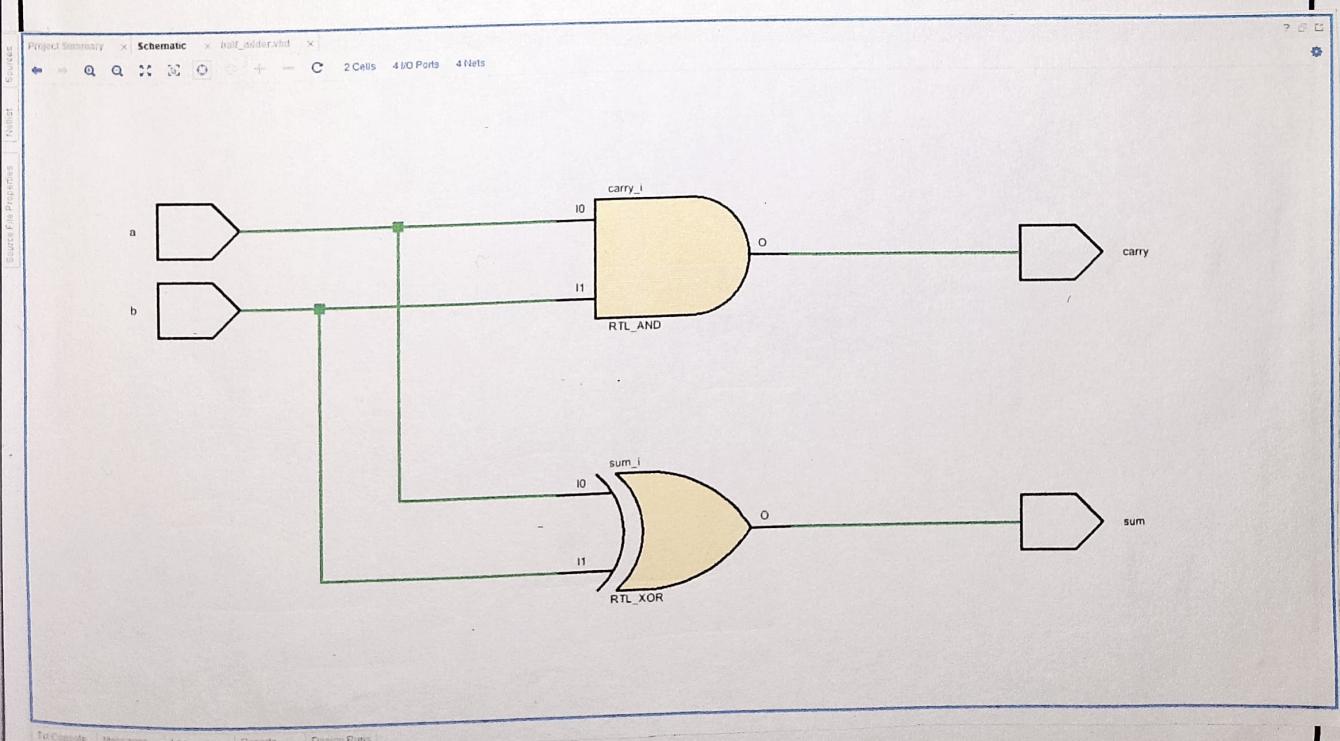
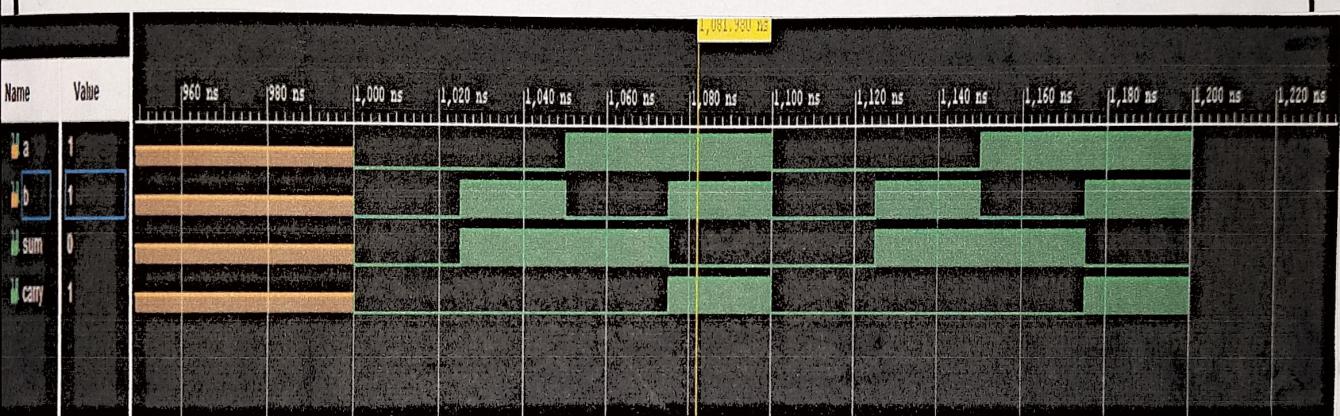
### III. LAB :

Software required : VHDL.

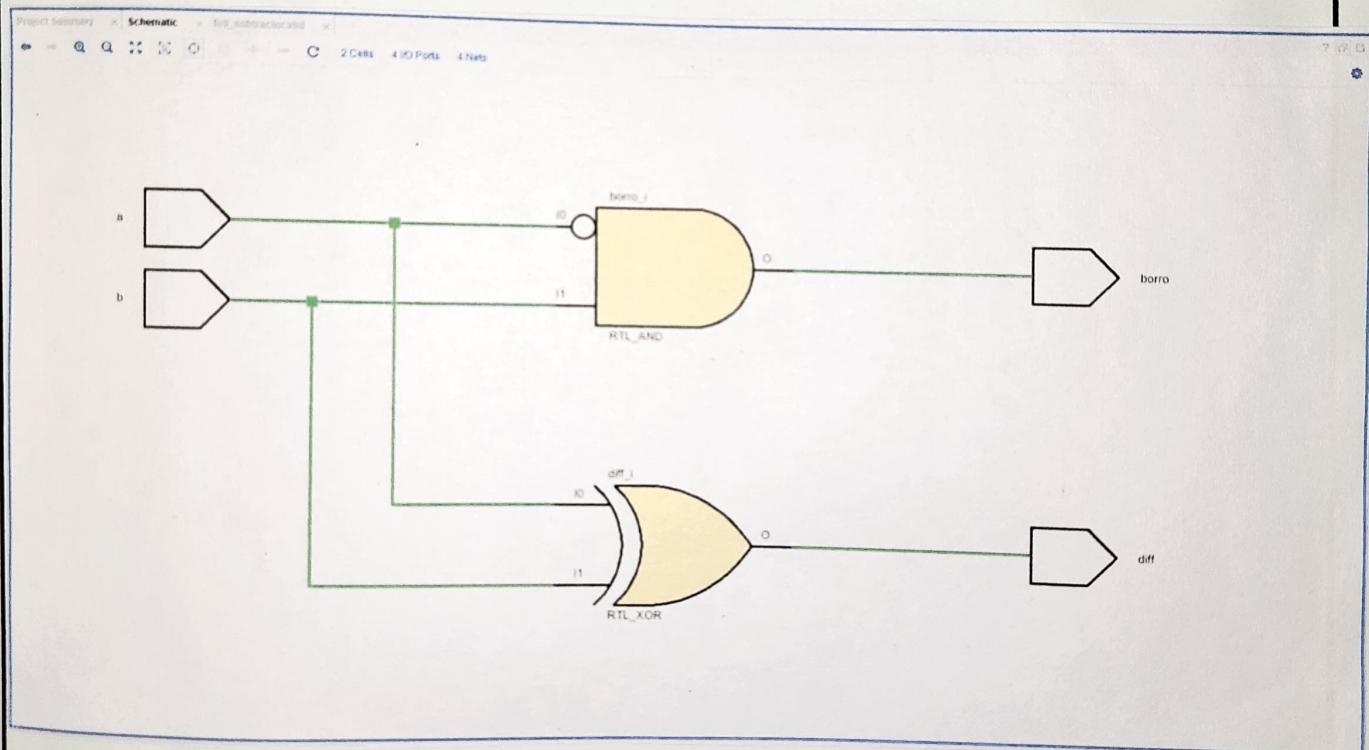
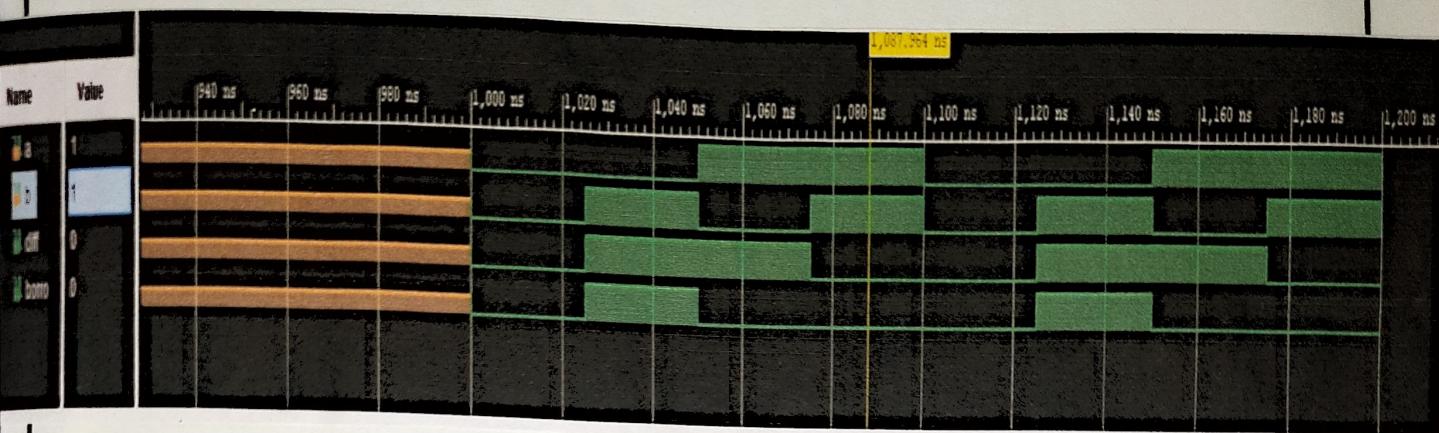
Observation:

Objective -1:

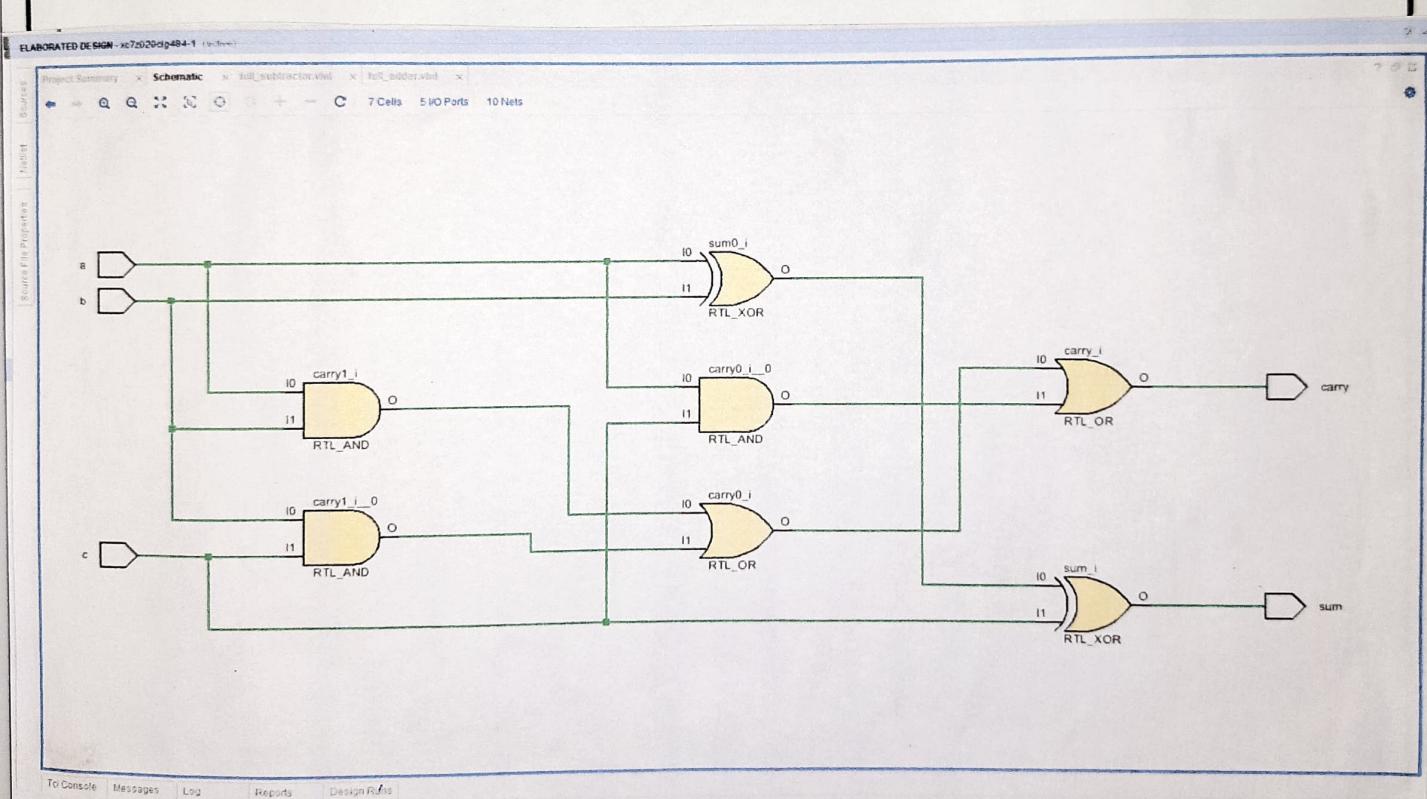
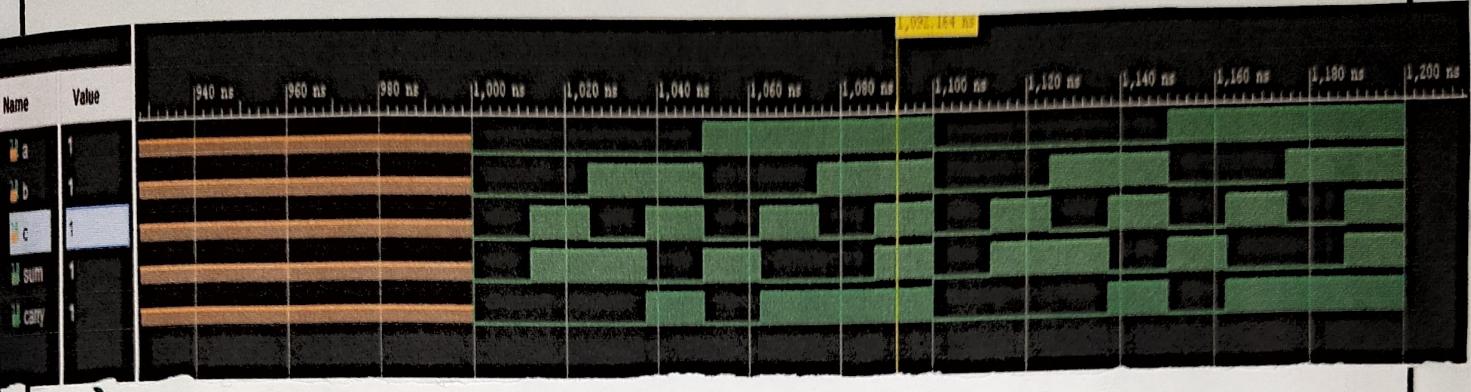
Half-Adder:



## Half-Subtractor:



## Objective-2 :

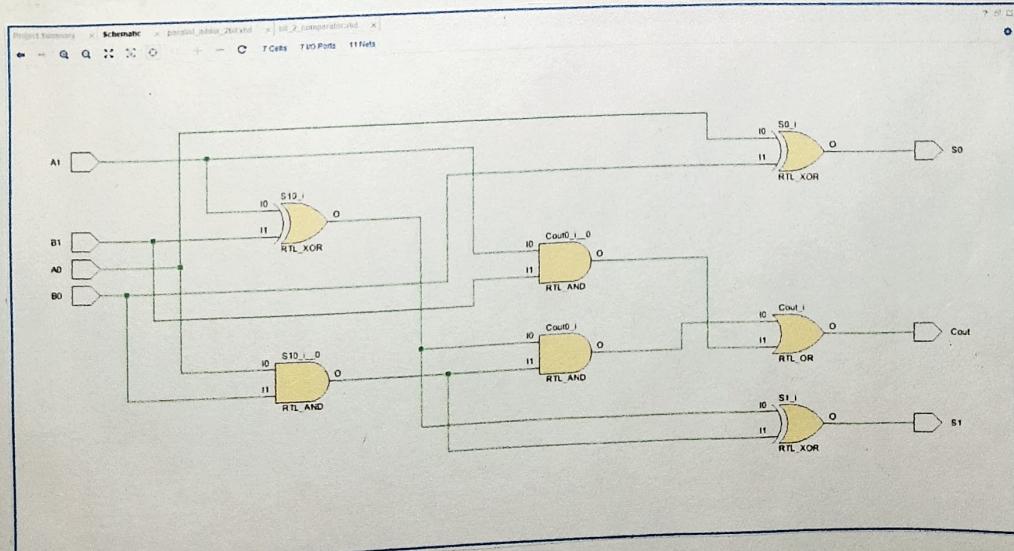


## Objective-3 :

```

parallel_adder_2bit.vhd
library IEEE;
use IEEE.STD.TEXTIO.TEXT.all;
-- Uncomment the following library declaration if using
-- arithmetic functions with signed or unsigned values
--use IEEE.STD.TEXTIO.TEXT.all;
-- Uncomment the following library declaration if instantiating
-- anyひたしの標準関数在此處
library STD;
use STD.TEXTIO.TEXTCOMPONENTS.all;
entity parallel_adder_2bit is
    Port (A1 : in STD.TEXTIO.TEXT;
          A0 : in STD.TEXTIO.TEXT;
          B1 : in STD.TEXTIO.TEXT;
          B0 : in STD.TEXTIO.TEXT;
          S0 : out STD.TEXTIO.TEXT;
          Cout : out STD.TEXTIO.TEXT);
end parallel_adder_2bit;
architecture dataflow of parallel_adder_2bit is
begin
    S0 := A0 AND B0;
    S1 := A1 XOR B1 XOR (B0 AND B1);
    Cout := (A1 AND B1) AND (A0 AND B0) OR (A1 AND B1);
end dataflow;

```



## IV. CONCLUSION:

We have successfully designed, constructed and tested the half adder, full adder, half subtractor and 2-bit parallel adder circuits. The circuits were tested and implemented through VHDL to conform its accuracy and performance.

## V. POST LAB:

1. A Half-adder is characterized by:

Ans. Two inputs and Two-outputs.

2. 4-bit parallel adder can add

Ans. Two 4-bit binary number.

3. Two four bit numbers can be added using two full adder. Yes or No? Justify your answer.

Ans. No.

To add two 4-bit numbers, a total of four full adders are required. Each full adder handles one bit of two no.s and the carry from prev. bit addition. Using two full adder would not be sufficient to handle the add of four bits.