

I. OBJECTIVE :

1. Design of multiplexer of 2×1 that will select the binary function information from one of the two input lines and direct it to single output line based on the value of selection line.
2. Design 3 to 8-line decoder with active low enabled input using NAND gates only.
3. Design a full adder using 3 to 8 line decoder and external OR gate.
4. Design a 4-bit priority encoder with inputs D_3 (MSB), D_2 , D_1 , D_0 (LSB) and output X , Y , and V . The priority assigned to inputs D_3 , D_2 , D_1 , D_0 . The output V shows a value 1 when one or more inputs are equal to 1. If all inputs are 0, V is equal to 0. When $V=0$, the other two outputs are not specified as don't care condition.

I. PRE-LAB :

Objective 1:

- Obtain truth table.
- Derive the Boolean expression for each output of the circuit.
- Draw the logic diagram for the circuit.
- Write VHDL code.

Ans.

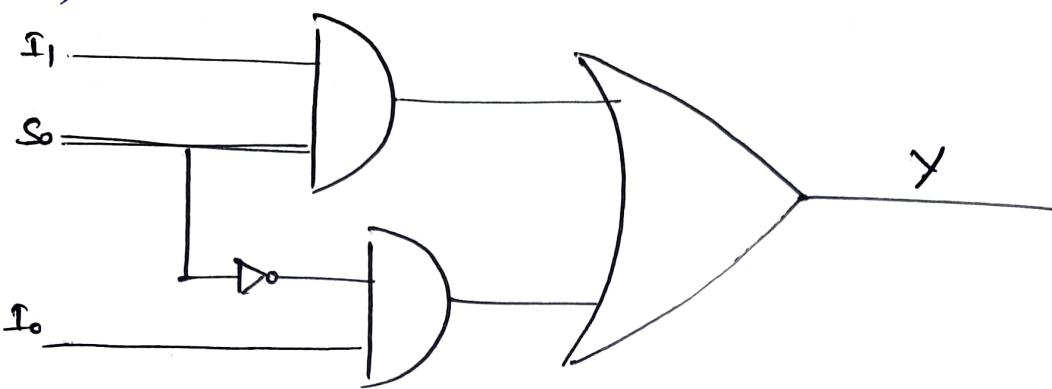
	S_0	I_0	I_1	Y
a)	0	0	0	0
	0	0	1	1
	1	1	0	1
	1	1	1	1

b) $Y = \sum m(1, 2, 3)$

$\bar{S}_0 \bar{I}_0 \bar{I}_1$	$\bar{I}_0 \bar{I}_1$	$\bar{I}_0 I_1$	$I_0 \bar{I}_1$	$I_0 I_1$
0		1	3	2
1		5	7	6
S_0				

$$Y = \bar{S}_0 I_0 + S_0 I_1$$

c)



d) entity MUX-2-X-1 is

```
Port ( S0 : in STD_LOGIC;  
      I0 : in STD_LOGIC;  
      I1 : in STD_LOGIC;  
      Y : out STD_LOGIC);
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end MUX-2-X-1;
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~~architecture dataflow of MUX-2-X-1 is~~

~~begin~~

~~Y <= ((NOT S0) AND I0) OR (S0 AND I1);~~

~~end dataflow;~~

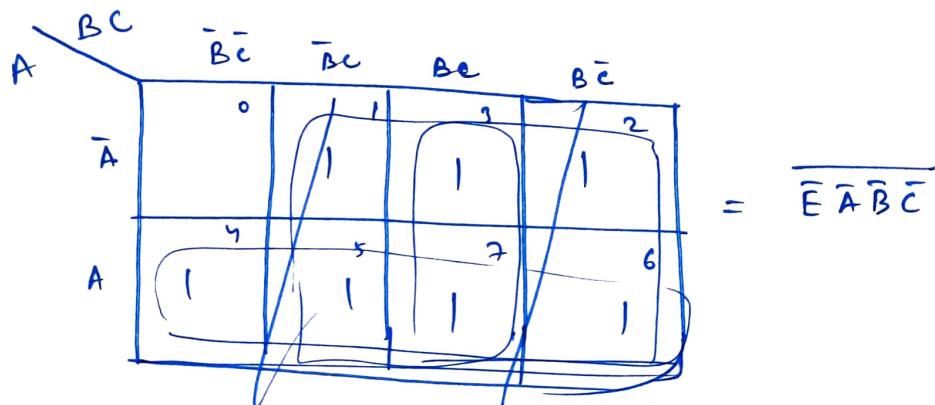
Objective-2:

- Obtain truth table.
- Derive the Boolean expression for each output of the circuit.
- Write the logic diagram for circuit.
- Write VHDL code.

Ans.

E	A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
1	X	X	X	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0

b) $D_0 = \sum_m(1, 2, 3, 4, 5, 6, 7)$



$$D_1 = \overline{E} \overline{A} \overline{B} C$$

$$D_2 = \overline{E} \overline{A} B \overline{C}$$

$$D_3 = \overline{E} \overline{A} \overline{B} \overline{C}$$

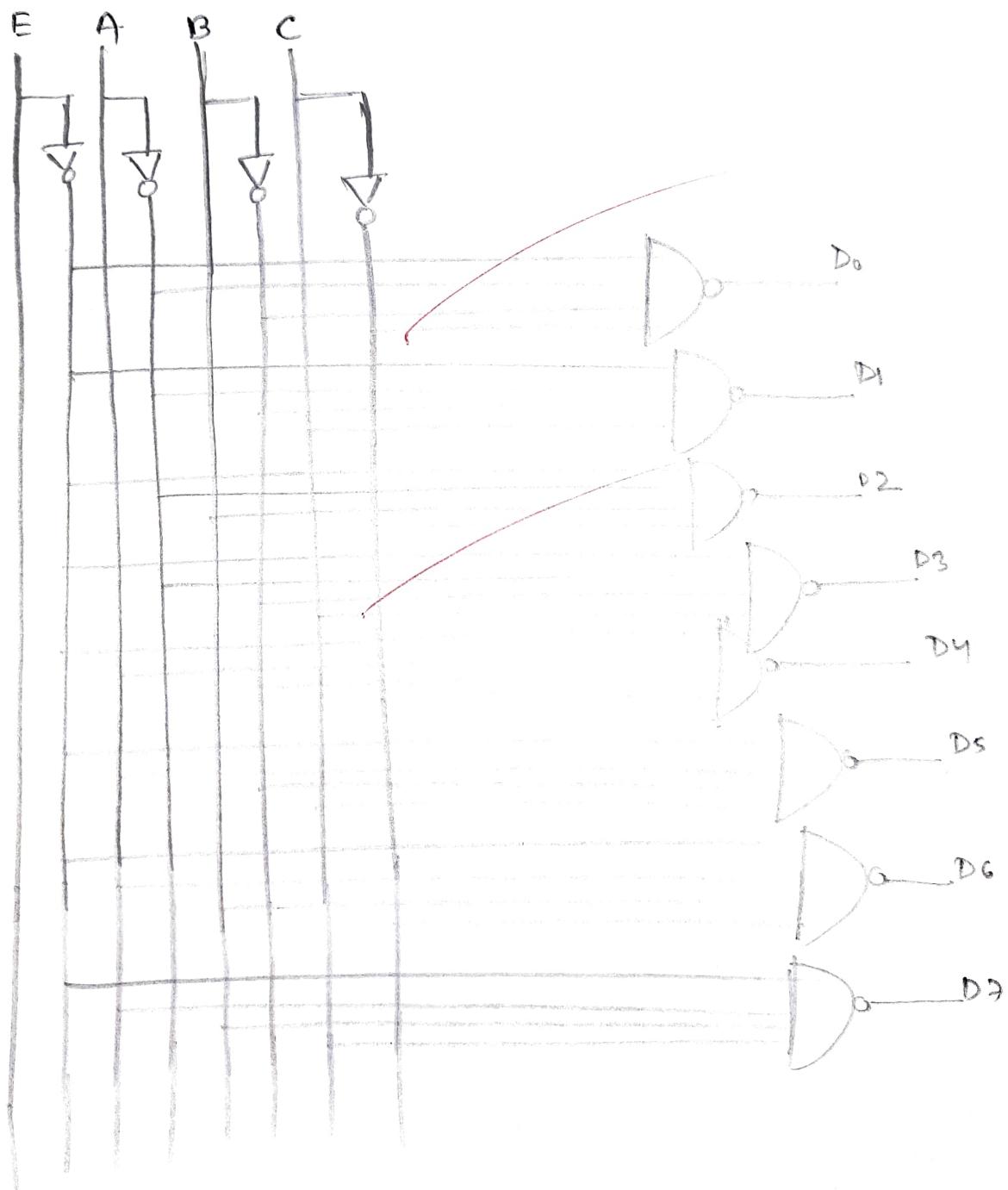
$$D_4 = \overline{E} A \overline{B} \overline{C}$$

$$D_5 = \overline{E} A \overline{B} C$$

$$D_6 = \overline{E} A B \overline{C}$$

$$D_7 = \overline{E} A B C$$

c)



d) entity LINE_3_TO_8_LINE_DECODER IS

Port (A: in STD_LOGIC;
B: in STD_LOGIC;
C: in STD_LOGIC;
E: in STD_LOGIC;
D0: out STD_LOGIC;
D1: out STD_LOGIC;
D2: out STD_LOGIC;
D3: out STD_LOGIC;
D4: out STD_LOGIC;
D5: out STD_LOGIC;
D6: out STD_LOGIC;
D7: out STD_LOGIC);

end LINE_3_TO_8_LINE_DECODER;

architecture dataflow LINE_3_TO_8_LINE_DECODER IS

begin

D0<=NOT((NOT E) AND (NOT A) AND (NOT B) AND (NOT C));
D1<=NOT((NOT E) AND (NOT A) AND (NOT B) AND (C));
D2<=NOT((NOT E) AND (NOT A) AND (B) AND (NOT C));
D3<=NOT((NOT E) AND (NOT A) AND (B) AND (C));
D4<=NOT((NOT E) AND (A) AND (NOT B) AND (NOT C));
D5<=NOT((NOT E) AND (A) AND (NOT B) AND (C));
D6<=NOT((NOT E) AND (A) AND (B) AND (NOT C));
D7<=NOT((NOT E) AND (A) AND (B) AND (C));

end dataflow;

Objective-3

- Obtain truth table.
- Derive Boolean expression for each output of the circuit.
- Draw the logic diagram for circuit.
- Write VHDL code.

Ans.

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

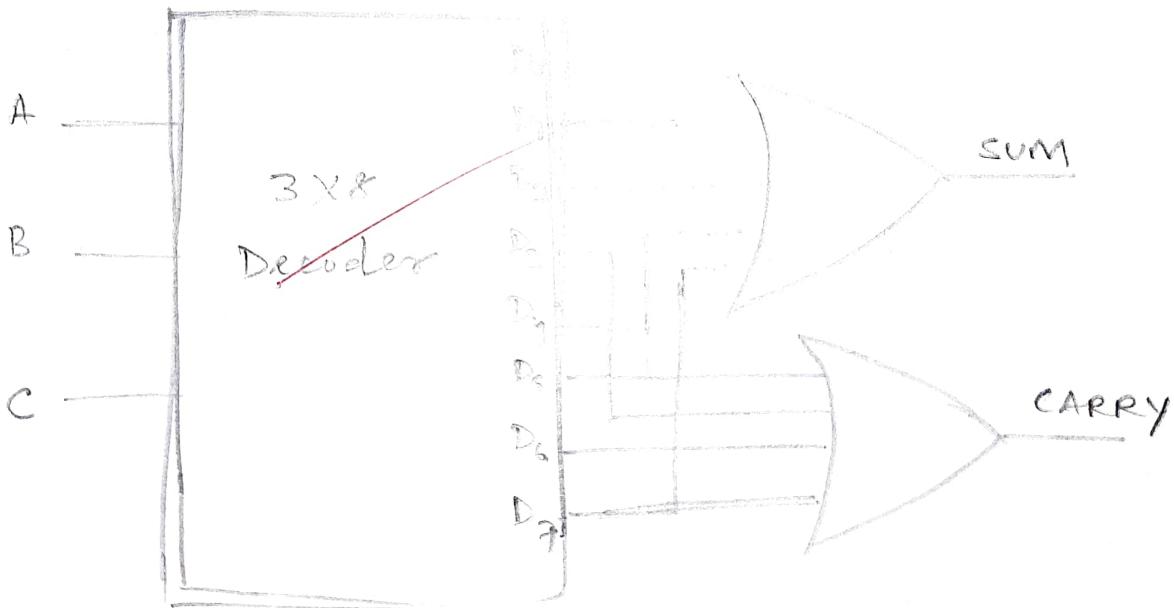
b) $SUM = \sum m = (1, 2, 4, 7)$

\bar{A}	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	1	3	2
A	1	5	7	6

$$\begin{aligned}
 \text{SUM} &= A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + A\bar{B}\bar{C} \\
 &= A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB \\
 &= \bar{B}(A\bar{C} + \bar{A}C) + AB \\
 &= \bar{B}(A \oplus C) + AB \\
 &= A \oplus B \oplus C
 \end{aligned}$$

$$\begin{aligned}
 \text{CARRY} &= \Sigma_m(3, 5, 6, 7) \\
 &= \bar{A}BC + A\bar{B}C + A\bar{B}\bar{C} + ABC \\
 &= \cancel{C}(\bar{A}B + A\bar{B}) + AB \\
 &= \cancel{C}(A \oplus B) + AB \\
 &= AB + BC + AC.
 \end{aligned}$$

c)



d)

entity FA_3_TO_8_DECODER is
Port(A : in STD_LOGIC;
B : in STD_LOGIC;
C : in STD_LOGIC;
SUM: out STD_LOGIC;
CARRY: out STD_LOGIC;
D0: inout STD_LOGIC;
D1: inout STD_LOGIC;
D2: inout STD_LOGIC;
D3: inout STD_LOGIC;
D4: inout STD_LOGIC;
D5: inout STD_LOGIC;
D6: inout STD_LOGIC;
D7: inout STD_LOGIC);
end FA_3_TO_8_DECODER;

architecture dataflow FA_3_TO_8_DECODER is

begin
 $D0 \leftarrow (\text{NOT } A) \text{ AND } (\text{NOT } B) \text{ AND } (\text{NOT } C);$
 $D1 \leftarrow (\text{NOT } A) \text{ AND } (\text{NOT } B) \text{ AND } C;$
 $D2 \leftarrow (\text{NOT } A) \text{ AND } (B) \text{ AND } (\text{NOT } C);$
 $D3 \leftarrow (\text{NOT } A) \text{ AND } (B) \text{ AND } (C);$
 $D4 \leftarrow (A) \text{ AND } (\text{NOT } B) \text{ AND } (\text{NOT } C);$
 $D5 \leftarrow (A) \text{ AND } (\text{NOT } B) \text{ AND } (C);$
 $D6 \leftarrow (A) \text{ AND } (B) \text{ AND } (\text{NOT } C);$
 $D7 \leftarrow (A) \text{ AND } (B) \text{ AND } (C);$
 $SUM \leftarrow D1 \text{ OR } D2 \text{ OR } D4 \text{ OR } D7;$
 $CARRY \leftarrow D3 \text{ OR } D5 \text{ OR } D6 \text{ OR } D7;$

end dataflow;

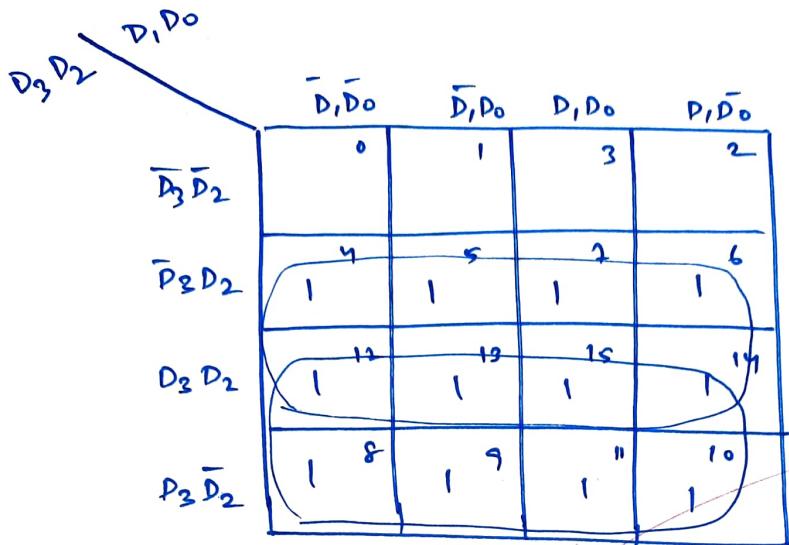
Q4 Objective 4:

- Obtain truth table.
- Derive Boolean expression for each output of the circuit.
- Draw the logic gates for the circuits
- Write VHDL code.

Ans.

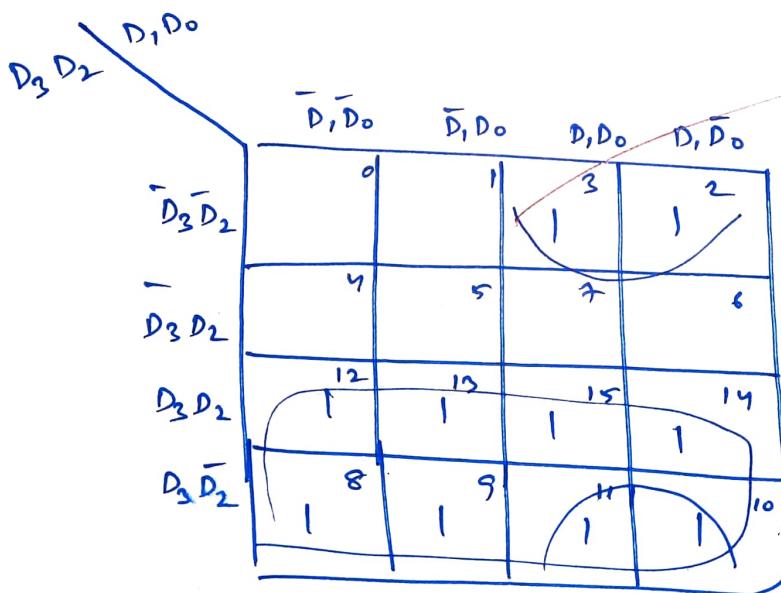
D_3	D_2	D_1	D_0	X	Y	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	0	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$$b) X = \sum m(4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$$



$$X = D_2 + D_3$$

$$Y = \sum m(2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$$



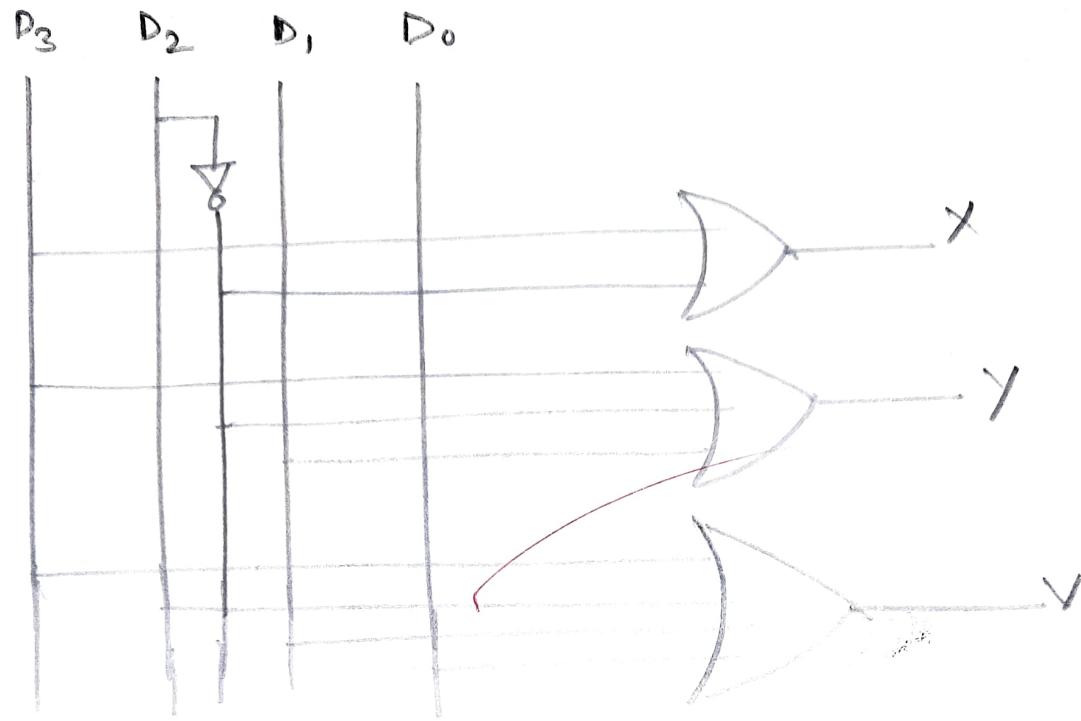
$$Y = D_3 + \bar{D}_2 D_1$$

$$V = \sum m(1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14)$$

$\bar{D}_3 D_2$	$\bar{D}_3 \bar{D}_2$	$D_3 \bar{D}_2$	$D_3 D_2$	$\bar{D}_1 D_0$	$\bar{D}_1 \bar{D}_0$	$D_1 D_0$	$D_1 \bar{D}_0$	\bar{D}_0
				0	1	3	2	
				1	1	1	1	
				4	5	6	7	
				12	13	15	17	
				1	1	1	1	
				8	9	11	10	

$$V = D_3 + D_2 + D_1 + D_0.$$

(d) c)



d) entity HIGH-P-ENCODER is
Port (D_3 : in STD-LOGIC;
 D_2 : in STD-LOGIC;
 D_1 : in STD-LOGIC;
 D_0 : in STD-LOGIC;
 X : out STD-LOGIC;
 Y : out STD-LOGIC;
 V : out STD-LOGIC);

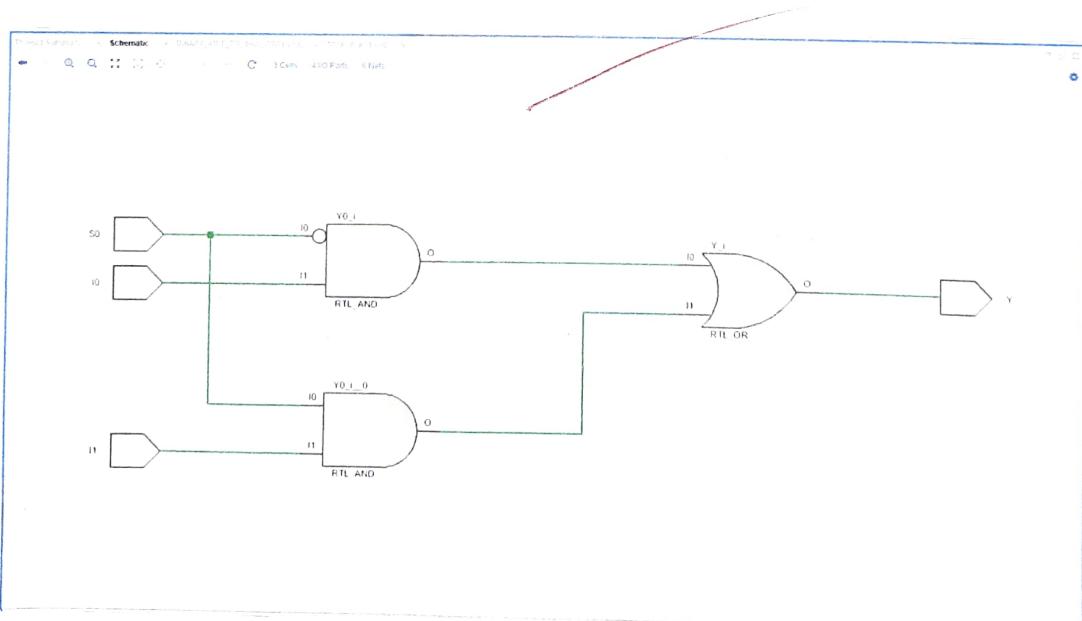
end HIGH-P-ENCODER;

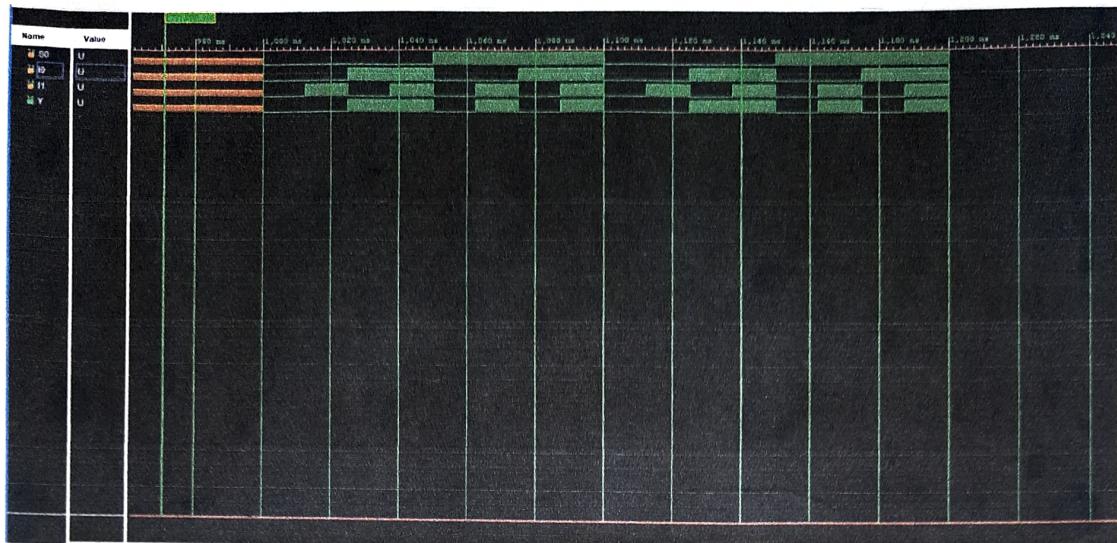
architecture dataflow HIGH-P-ENCODER is
begin

III. LAB

Software required: VHDL.

Objective 1:

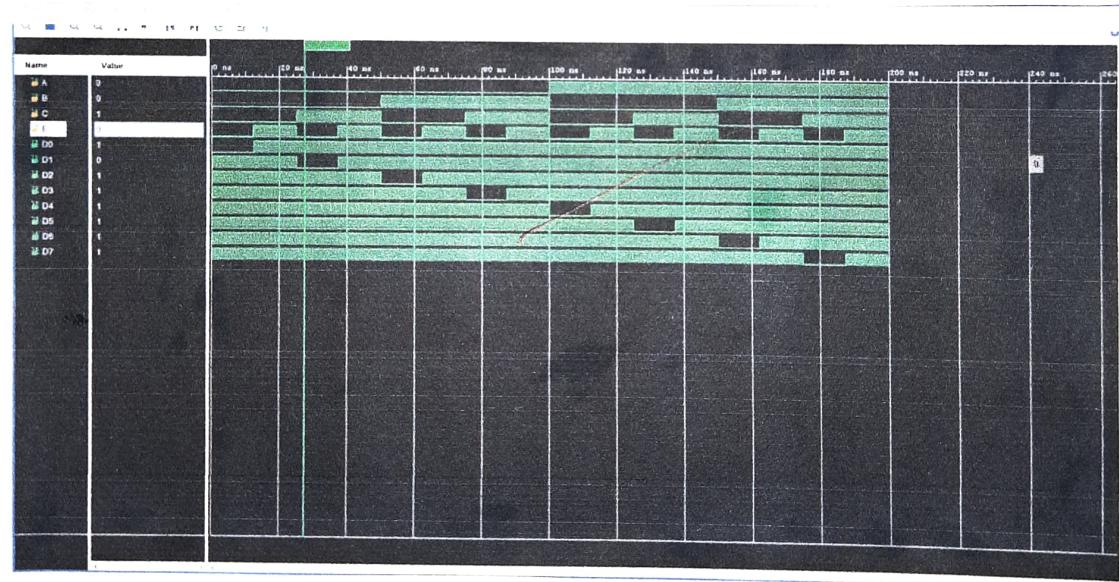
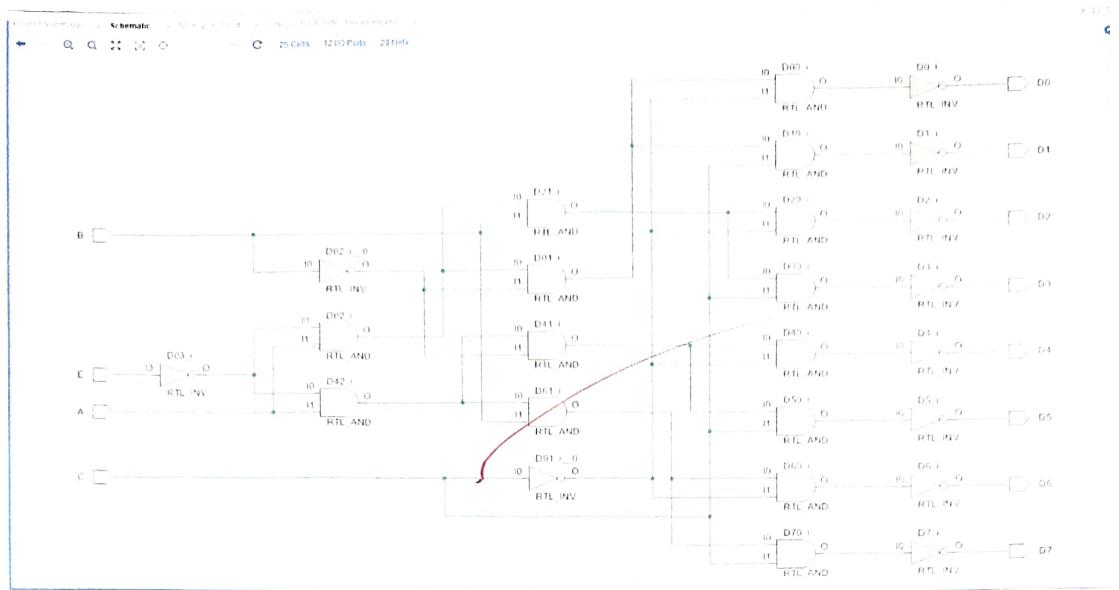


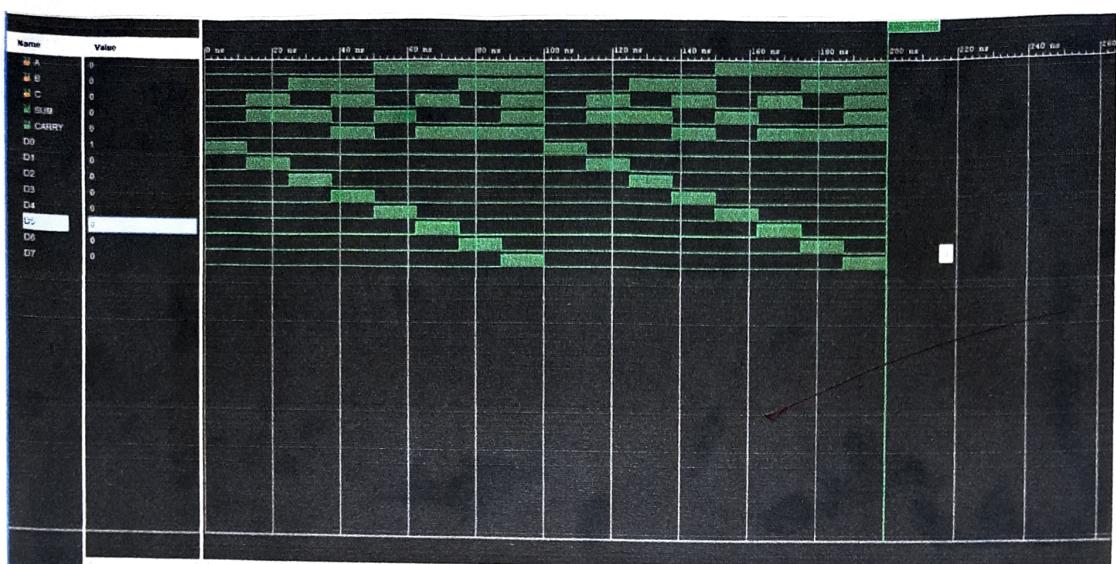


Objective-2 :

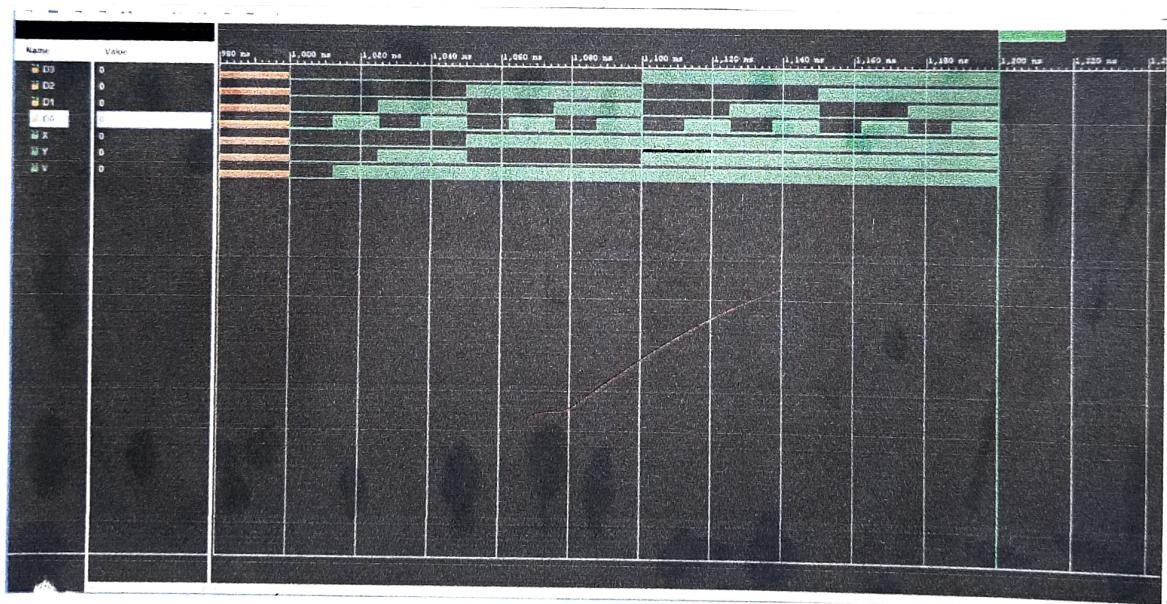
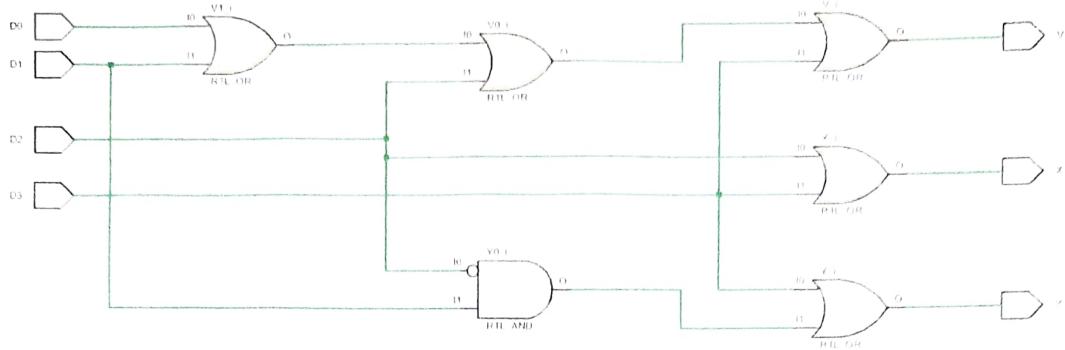
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Created STUDENT DEFINED LOGIC FUNCTIONS (INSTANCES) TRAVERSE_1 TO 8, ONE DECODED AS  
SEARCH X F1 F2 F3 F4 F5 F6 F7 F8  
LIBRARY IEEE;  
USE STD.TEXTIO;  
  
ENTITY LUT IS  
PORT (A,B,C,D : STD_LOGIC;  
      E,F,G,H : STD_LOGIC;  
      I,J,K,L : STD_LOGIC;  
      M,N,O,P : STD_LOGIC;  
      Q,R,S,T : STD_LOGIC;  
      U,V,W,X : STD_LOGIC;  
      Y,Z,U1,U2,U3,U4,U5,U6,U7,U8 : STD_LOGIC);  
END;  
  
ARCHITECTURE behave OF LUT IS  
BEGIN  
  PROCESS(A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P,Q,R,S,T,U,V,W,X,Y,Z,U1,U2,U3,U4,U5,U6,U7,U8)  
    VARIABLE T : STD.TEXTFILE;  
    BEGIN  
      IF (A=1 AND B=1 AND C=1 AND D=1) THEN  
        IF (E=1 AND F=1 AND G=1 AND H=1) THEN  
          IF (I=1 AND J=1 AND K=1 AND L=1) THEN  
            IF (M=1 AND N=1 AND O=1 AND P=1) THEN  
              IF (Q=1 AND R=1 AND S=1 AND T=1) THEN  
                IF (U=1 AND V=1 AND W=1 AND X=1) THEN  
                  IF (Y=1 AND Z=1 AND U1=1 AND U2=1 AND U3=1 AND U4=1 AND U5=1 AND U6=1 AND U7=1 AND U8=1) THEN  
                    OPEN TEXTFILE T;  
                    WRITELINE(T,"1");  
                    CLOSE(T);  
                  ELSE  
                    OPEN TEXTFILE T;  
                    WRITELINE(T,"0");  
                    CLOSE(T);  
                  END IF;  
                ELSE  
                  OPEN TEXTFILE T;  
                  WRITELINE(T,"0");  
                  CLOSE(T);  
                END IF;  
              ELSE  
                OPEN TEXTFILE T;  
                WRITELINE(T,"0");  
                CLOSE(T);  
              END IF;  
            ELSE  
              OPEN TEXTFILE T;  
              WRITELINE(T,"0");  
              CLOSE(T);  
            END IF;  
          ELSE  
            OPEN TEXTFILE T;  
            WRITELINE(T,"0");  
            CLOSE(T);  
          END IF;  
        ELSE  
          OPEN TEXTFILE T;  
          WRITELINE(T,"0");  
          CLOSE(T);  
        END IF;  
      ELSE  
        OPEN TEXTFILE T;  
        WRITELINE(T,"0");  
        CLOSE(T);  
      END IF;  
    END IF;  
  END PROCESS;  
END;
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Digital Logic Design (EET1211)
 Faculty of Engineering & Technology (ITER)





Objective-4 :



CONCLUSION :

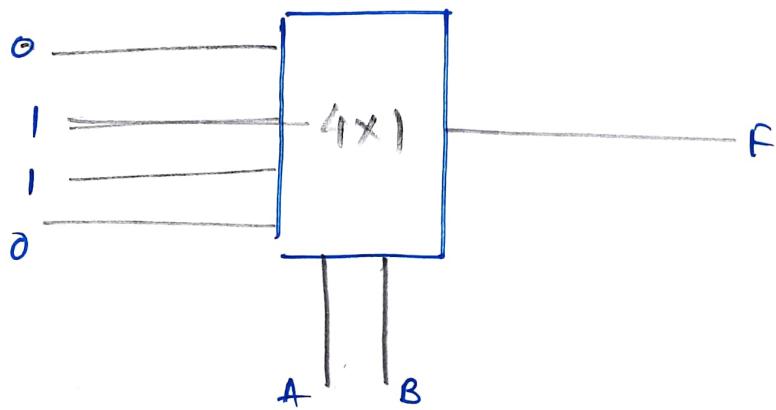
We have successfully designed, constructed
2x1 MUX, 3 to 8 Line Decoder, Full Adder using
3 to 8 Line Decoder and High Priority Encoder.
Each circuit's truth table, Boolean expression and
circuit diagrams were verified through
VHDL simulations.

Q. POST-LAB :

1. Design a 2 input XOR gate using 4x1 MUX.

Ans.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



2. Design a 8x1 MUX using 4x1 MUX.

