DIGITAL LOGIC DESIGN LAB (EET1211)

LAB V: Design of combinational circuits using VHDL

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: ____/10

Remarks:

Teacher's Signature

I. Objective:

1. Design a 2 bit Comparator circuit.
2. Design a combinational circuit with four inputs and four outputs that converts a 4bit binary number into the equivalent 4bit Gray code
3. Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.

II. Pre-lab:

Obj. 1:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 2:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 3:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

III. LAB:

Software Required:

Observation:

(Attach screenshot of Source code, Test bench, Schematic diagram and waveform)

IV. CONCLUSION:

V. POST LAB:

1. Design a 3 bit majority circuit.

2. What is the advantage of Gray code?

3. Draw the logic circuit that converts a 4 bit Gray code to binary code.