DIGITAL LOGIC DESIGN LAB (EET1211)

LAB IV: Introduction to VHDL and Design of combinational circuits using VHDL

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: ____/10

Remarks:

Teacher's Signature

I. Objective:

1. Design, construct, and test a Half_Adder and Half_Subtractor circuit
2. Design, construct and test a Full Adder circuit.
3. Design, construct, and test a 2 bit Parallel Adder circuit.

II. Pre-lab:

Obj. 1:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 2:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 3:

a) Obtain the truth table.
b) Derive the Minimized Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

III. LAB:

Software Required:

Observation:

(Attach screenshot of Source code, Test bench, Schematic diagram and waveform)

IV. CONCLUSION:

V. POST LAB:

1. A Half-adder is characterized by

a. Two inputs and two outputs b. Three inputs and two outputs
c. Two inputs and three outputs d. Two inputs and one outputs

2. A 4-bit parallel adder can add

a. Two 4-bit binary numbers b. Two 2-bit binary number
c. Four bits at a time d. Four bits at a time

3. Two four bit numbers can be added using two full adders. Yes or No? Justify answer.