

## OBJECTIVE -

1. Design and test of D flip-flop with negative edge-triggering.
2. Design and test of JK flip-flop active ~~low~~ low asynchronous reset and negative positive edge-triggering.
3. Design and test of flip-flop with active low synchronous reset and positive edge-triggering.

## II. PRE-LAB :

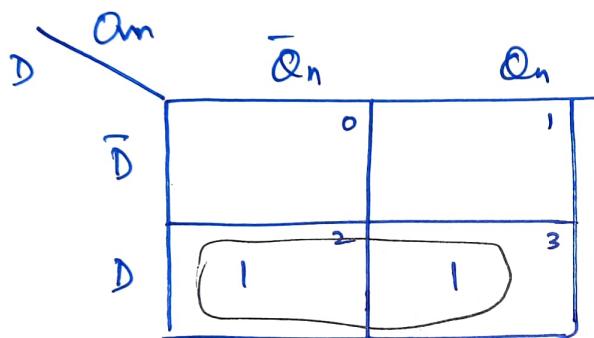
### Objective 1 :

- a) Obtain the characteristics table.
- b) Design Derive the characteristic eqn of D-flip flop.
- c) Draw the circuit diagram of circuit.
- d) Write VHDL code.

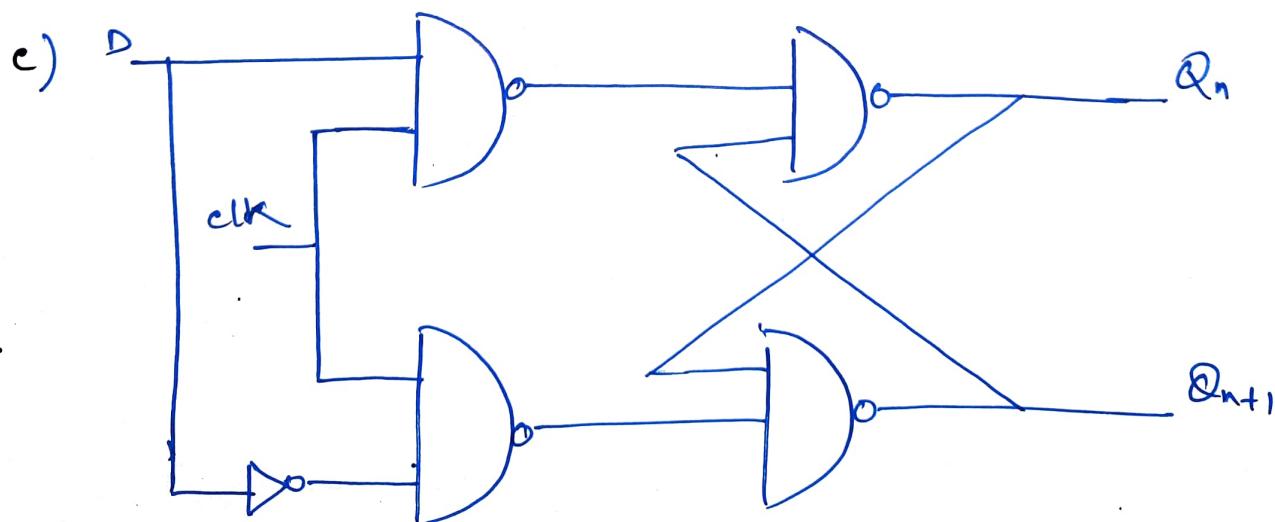
Ans.

a)	D	$Q_n$	$Q_{n+1}$
	0	0	0
	0	1	0
	1	0	1
	1	1	1

b) Derive the characteristics eqn of D-flip flop



$$Q_{n+1} = D$$



d) entity DFF-PE is  
Port ( D: in STD-LOGIC;  
CLK: in STD-LOGIC;  
Q: in STD-LOGIC;  
QB: in STD-LOGIC);  
end DFF-PE;

architecture Behavioral of DFF-PE is

begin

Process (D, CLK)

begin

if (CLK'EVENT AND CLK = '0') then

    Q <= D;  
    QB <= NOT D;

  end if;

end process;

end Behavioral;

### Objective-2 :

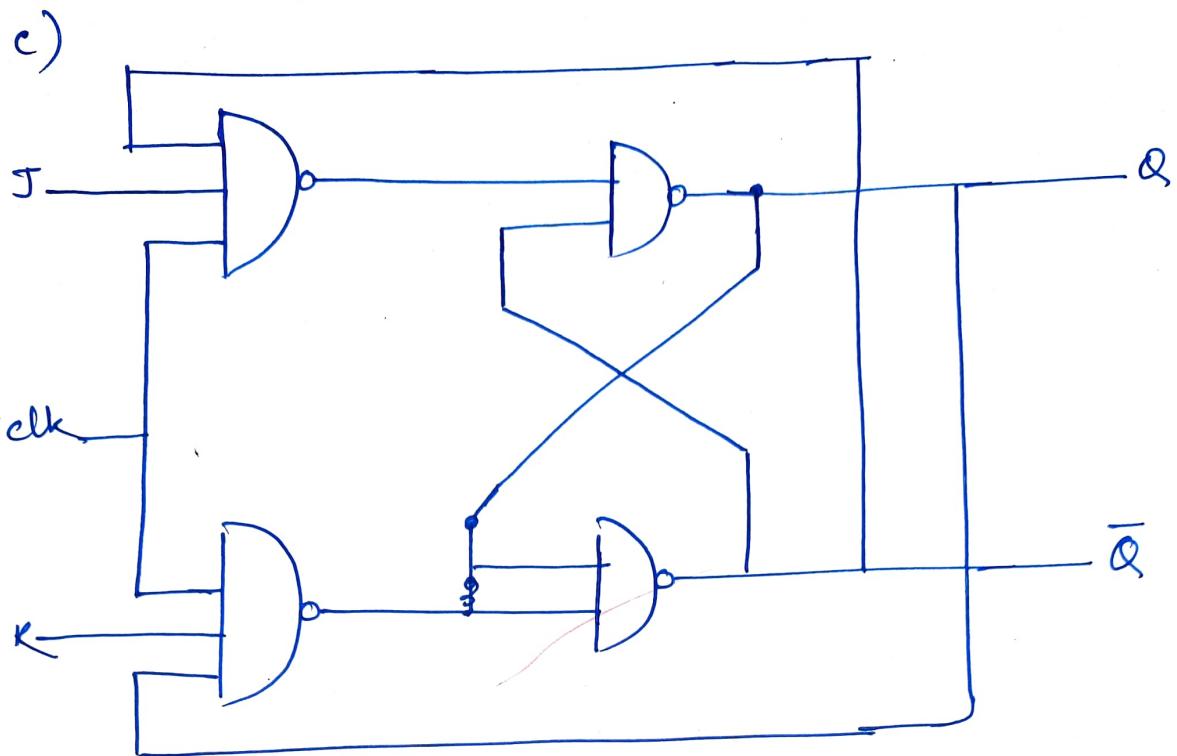
- Obtain the characteristics table.
- Derive the characteristics eqn for JK flipflop.
- Draw the circuit diagram.
- Write VHDL code.

Ans.

J	K	$Q_n$	$Q_{n+1}$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

	$\bar{K}Q_n$	$\bar{K}Q_n$	$\bar{K}Q_n$	$\bar{K}Q_n$
$\bar{J}$	0	1	3	2
J	1	1	1	1

$$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$



d) entity JK-FF is

Port (RST: in STD-LOGIC)

CLK: in STD-LOGIC

J : in STD-LOGIC

K: in STD-LOGIC;

Q: out STD-LOGIC;

Qbar: out STD-LOGIC;

and JK-FF;

Architecture Behavioral of TK-FF is

signal  $q_n$ : STD\_LOGIC;

begin

process(clk, RST, J, K)

begin

```
if (R&T = '0') then  
    qn <= 0;  
elsif (CLK'event and CLK='1') then  
    if (J = '0' and K = '0') then  
        qn <= qn;  
    elsif (J = '0' and K = '1') then  
        qn <= '0';  
    elsif (J = '1' and K = '0') then  
        qn <= '1';  
    elsif (J = '1' and K = '1') then  
        qn <= not qn;  
    end if;  
    Q <= qn;  
    Qbar <= not qn;  
end process;  
end Behavioral;
```

Objective-3 :

- Obtain the characteristics table.
- Derive the characteristics eqn of T-flip flop.
- Draw the circuit diagram for circuit.
- Write VHDL code.

Aus.

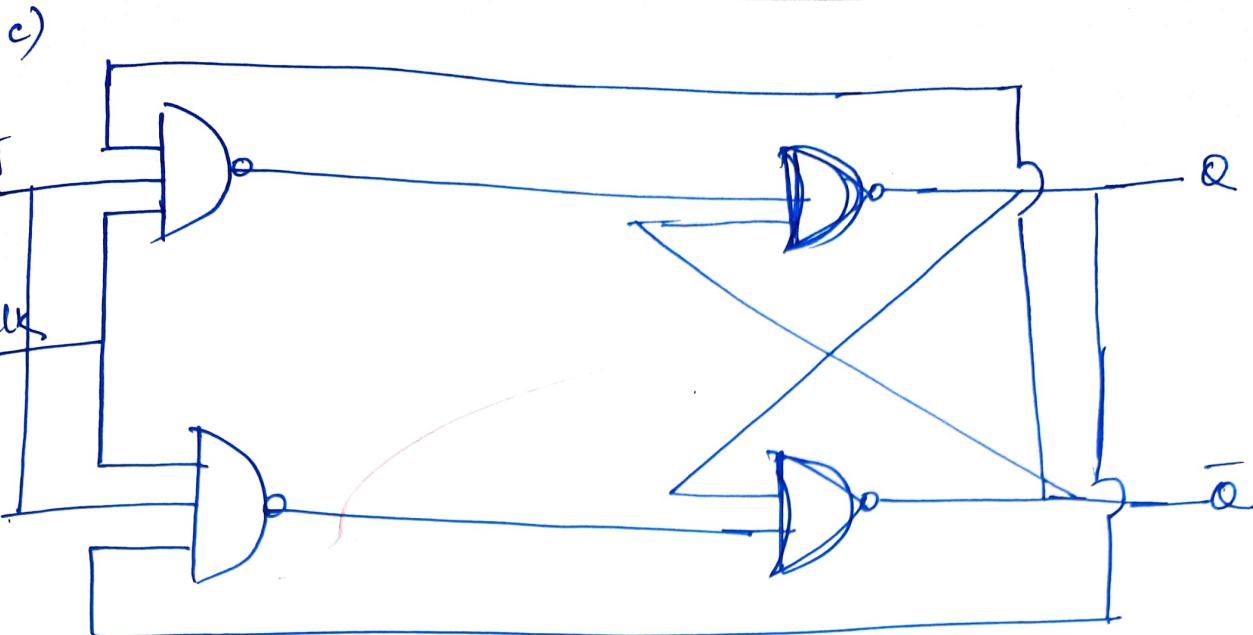
a)

T	$\bar{Q}_n$	$\bar{Q}_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

b)

T	$\bar{Q}_n$	$\bar{Q}_n$	$\bar{Q}_n$
$\bar{T}$	0	(1)	1
T	(1)	2	3

$$Q_{n+1} = \bar{Q}_n T + \bar{T} Q_n = Q_n \oplus T$$



d) entity TFF is  
Port(RES, CLK, T : in STD-LOGIC;  
Q, QNOT, I Buffer STD-LOGIC);  
end TFF;

architecture Behavioral of TFF is

begin

~~QNOT <= NOT Q;~~

process (T, CLK, RES)

BEGIN

if (RES = '0') THEN

~~Q <= '0';~~

elsif (rising-edge(CLK)) then

if (~~T~~ = '1') then

~~Q <= NOT Q;~~

end if;

end process;

end Behavioral;

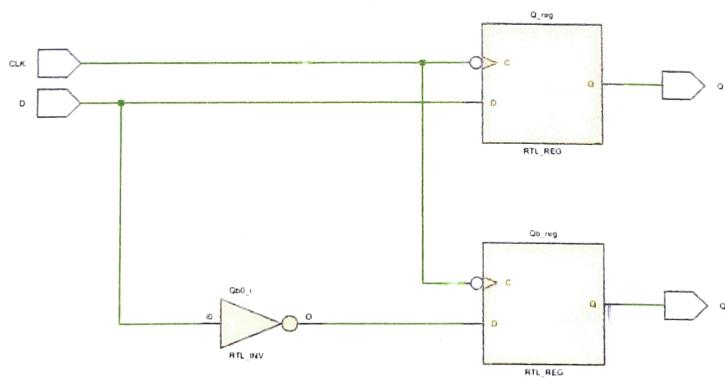
## III. OBSERVATION :

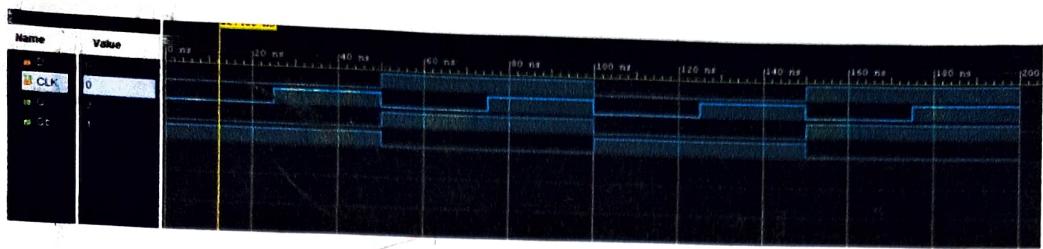
Software required : VHDL

Objective-1 :

```
entity TFF_PE is
    Port ( RES,CLK,T : in STD_LOGIC;
           Q,Qb : buffer STD_LOGIC);
end TFF_PE;

architecture Behavioral of TFF_PE is
begin
    Qb <= NOT Q;
    process(CLK,RES)
    begin
        if(RES = '0')then
            Q <= '0';
        elsif(rising_edge(CLK))then
            if(T = '1')then
                Q <= not Q;
            end if;
        end if;
    end process;
end Behavioral;
```

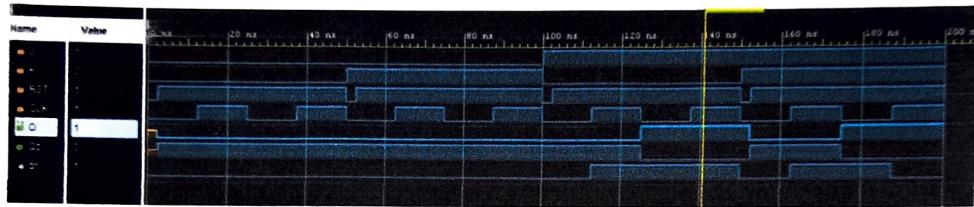
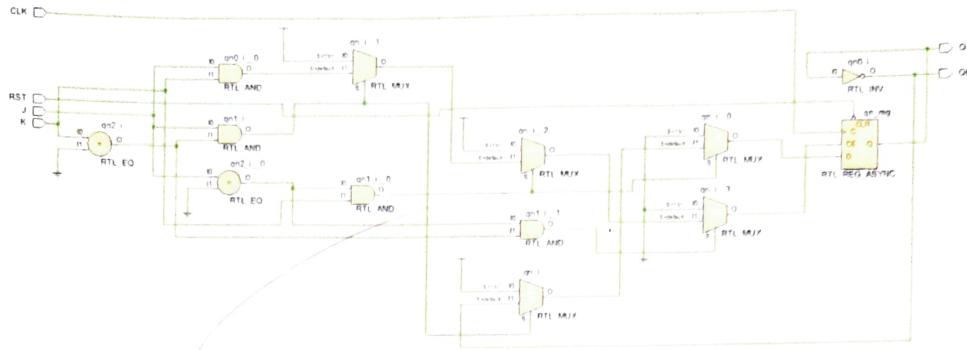




Objective-2:

```
entity JKFF_PE is
  Port ( J,K,RST,CLK : in STD_LOGIC;
         Q,Qb : out STD_LOGIC);
end JKFF_PE;

architecture Behavioral of JKFF_PE is
  signal qn : STD_LOGIC;
begin
  process(RST,CLK,J,K)
  begin
    if(RST='0')then
      qn='0';
    elsif(CLK'EVENT AND CLK='1')then
      if(J='0' AND K='0')then
        qn <= qn;
      elsif(J='0' AND K='1')then
        qn <= '0';
      elsif(J='1' AND K='0')then
        qn <= '1';
      elsif(J='1' AND K='1')then
        qn <= not qn;
      end if;
    end if;
    Q <= qn;
    Qb <= not qn;
  end process;
end Behavioral;
```



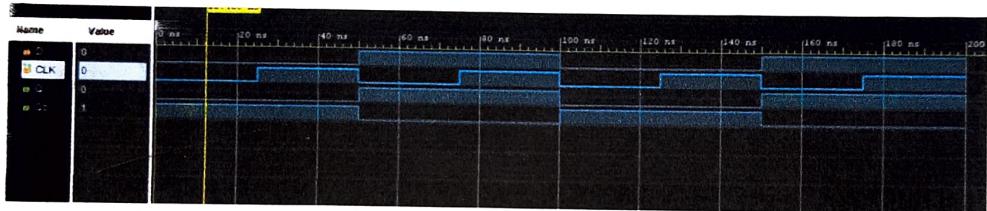
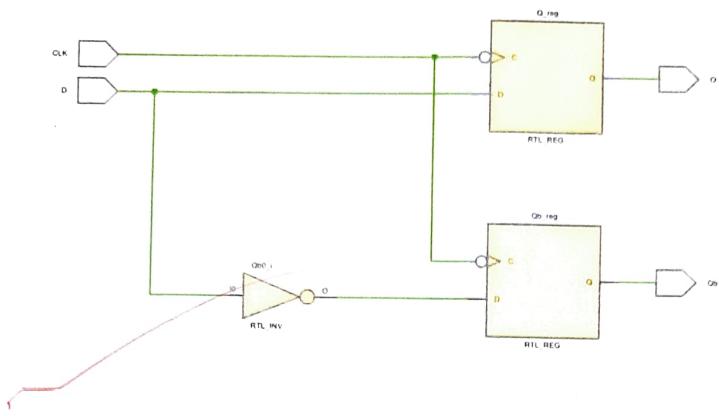
Objective - 3 :

```

entity TFF_PE is
    Port ( RES,CLK,T : in STD_LOGIC;
           Q,Qb : buffer STD_LOGIC);
end TFF_PE;

architecture Behavioral of TFF_PE is
begin
    Qb <- NOT Q;
    process (T,CLK,RES)
    begin
        if(RES = '0')then
            Q <- '0';
        elsif(rising_edge(CLK))then
            if(T = '1')then
                Q <- not Q;
            end if;
        end if;
    end process;
end Behavioral;

```



## IV. CONCLUSION:

We have successfully designed, constructed D-flip flop, JK flip flop and T flip flop. Each circuit's truth table, Boolean expression and circuit diagram were verified through VHDL simulations.

## V. POST-LAB:

### 1. Difference between Latch and flip flop

#### Ans. Latch

- i) Latch does not require clock symbol.
- ii) A latch is a level sensitive device (level triggered involved).
- iii) The operation of a latch is faster as they do not have to wait for any clock signal.
- iv) The power required for latch is less.
- v) It works based on enable signals.

#### Flip-flop

- i) Flip-flop have clock signal.
- ii) A flip-flop is an edge sensitive device. (Edge triggering involved)
- iii) Flip-flops are comparatively slower than latch due to clock signal.
- iv) Power required is more.
- v) It work based on clock signals.

2) If both inputs of SR NOR latch are low, what will happen to output?

Ans. the output will not be changed.

3) If both inputs of SR NAND are low, what will happen to the output?

Ans. the output will toggle.

4) Which of the following describes the operations of a positive edge-triggered D-flip-flop?

Ans. The output will follow the input of on the leading edge of the clock.