

DIGITAL LOGIC DESIGN LAB (EET1211)

LAB V: Design of combinational circuits using VHDL

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Marks: ___/10

Remarks:

Teacher's Signature

I. OBJECTIVE :

1. Design a 2-bit comparator circuit.
2. Design a combinational circuit with 4 inputs and 4-outputs that converts a 4-bit Binary no. to its equivalent 4-bit Gray code.
3. Design a combinational circuit with four input lines that represent a decimal digit in BCD and 4-input output lines that generate the 9's complement of the input digit.

II. PRE-LAB :

Objective 1:

- a) Obtain the truth table.
- b) Derive the minimized Boolean expression for each output of the circuit.
- c) Draw the logic diagram for the circuit.
- d) Write the VHDL code.

Ans

a)

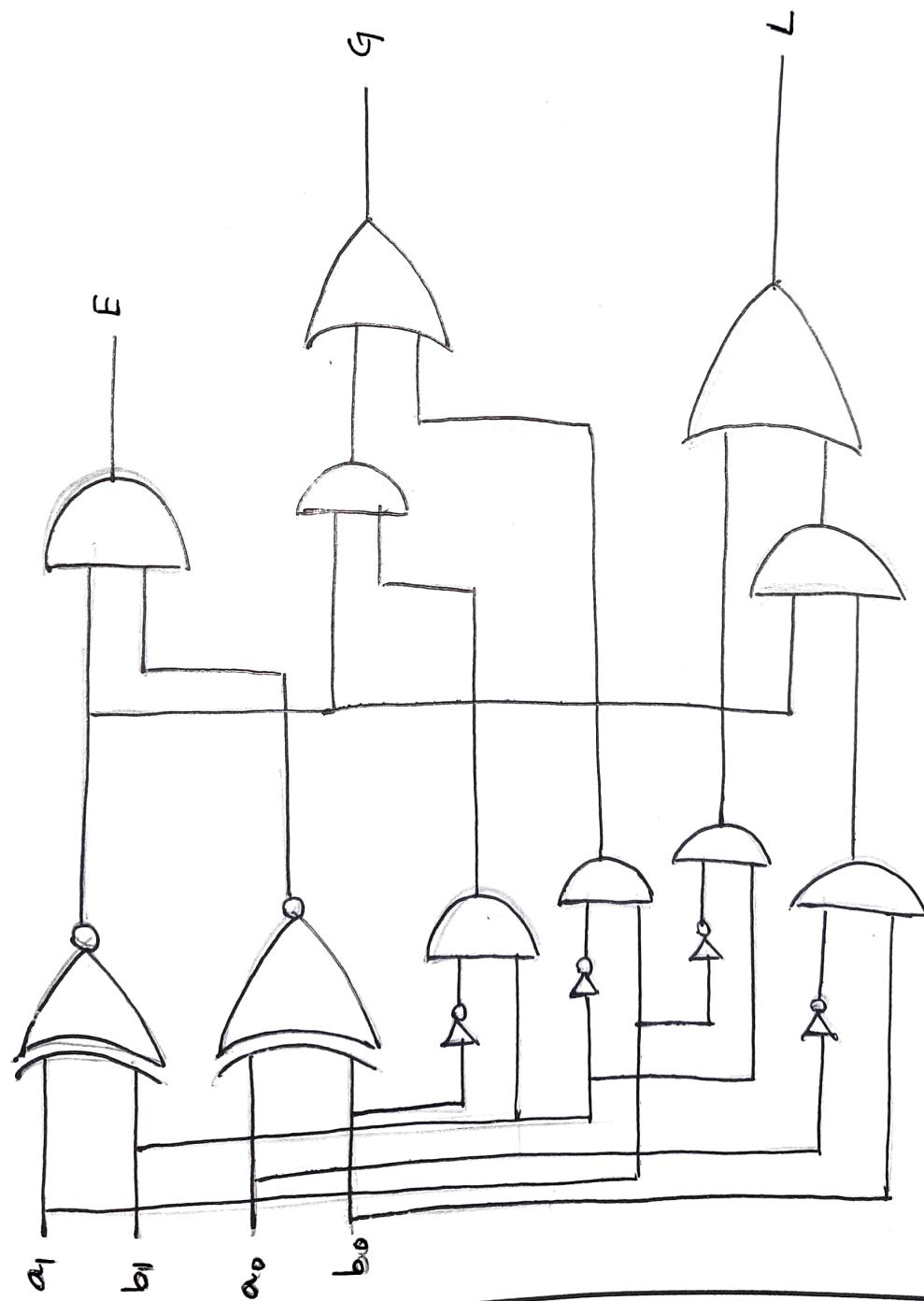
A1	A0	B1	B0	G	L	E
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

$$b) A \otimes B = A_1 \bar{B}_1 + (A_1 \odot B_1) A_0 \bar{B}_0$$

$$A \triangle B = \bar{A}_1 B_1 + (A_1 \odot B_1) \bar{A}_0 B_0$$

$$A \oplus B = (A_1 \odot B_1) (A_0 \odot B_0).$$

c)



d)

entity magnitude-comparator is

```
Port( A1: in STD-LOGIC;
      A0: in STD-LOGIC;
      B1: in STD-LOGIC;
      B0: in STD-LOGIC;
      G: out STD-LOGIC;
      E: out STD-LOGIC;
      L: out STD-LOGIC);
```

end magnitude-comparator;

architecture dataflow of magnitude-comparator is

begin

$$\begin{aligned} G &\leftarrow (A1 \text{and} (\text{not } B1)) \text{or} ((A1 \text{xnor } B1) \text{ and } (A0 \text{and} \\ &\quad \text{not } B)); \\ E &\leftarrow (A1 \text{xnor } B1) \text{ and } (A0 \text{xnor } B0); \\ L &\leftarrow ((\text{not } A1) \text{ and } B1) \text{ or} ((A1 \text{xnor } B1) \text{ and } ((\text{not } A0) \text{ and } B0)); \end{aligned}$$

end dataflow;

Objective-2 :

- Obtain the truth table.
- Derive the minimized Boolean expression for each output of the circuit.
- Draw the logic diagram for the circuit.
- Write VHDL code.

Ans.

a)

B_3	B_2	B_1	B_0	G_{13}	G_{12}	G_{11}	G_{10}
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

b)

$$G_3 := \sum m(8, 9, 10, 11, 12, 13, 14, 15)$$

$B_3 B_2$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$\bar{B}_1 B_0$	0	1	3	2
$\bar{B}_1 \bar{B}_0$	4	5	7	6
$B_1 B_0$	12	13	15	14
$B_1 \bar{B}_0$	1	1	1	1
$\bar{B}_1 \bar{B}_0$	8	9	11	10
$B_3 \bar{B}_2$	1	1	1	1

$$\therefore G_3 = B_3.$$

$$G_2 := \sum m(4, 5, 6, 7, 8, 9, 10, 11)$$

$B_3 B_2$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$\bar{B}_1 B_0$	0	1	3	2
$\bar{B}_1 \bar{B}_0$	4	5	7	6
$B_1 B_0$	12	13	15	14
$B_1 \bar{B}_0$	1	1	1	1
$\bar{B}_1 \bar{B}_0$	8	9	11	10
$B_3 \bar{B}_2$	1	1	1	1

$$G_2 = \bar{B}_3 B_2 + B_3 \bar{B}_2 = B_3 \oplus B_2$$

$$G_1 = \sum m (2, 3, 4, 5, 10, 11, 12, 13)$$

$B_3 B_2$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 \bar{B}_0$	$B_1 B_0$
0		1		3	2
$\bar{B}_3 B_2$	1	1	5	7	6
$B_3 B_2$	12	13		15	14
$\bar{B}_3 \bar{B}_2$	8	9	11	1	10

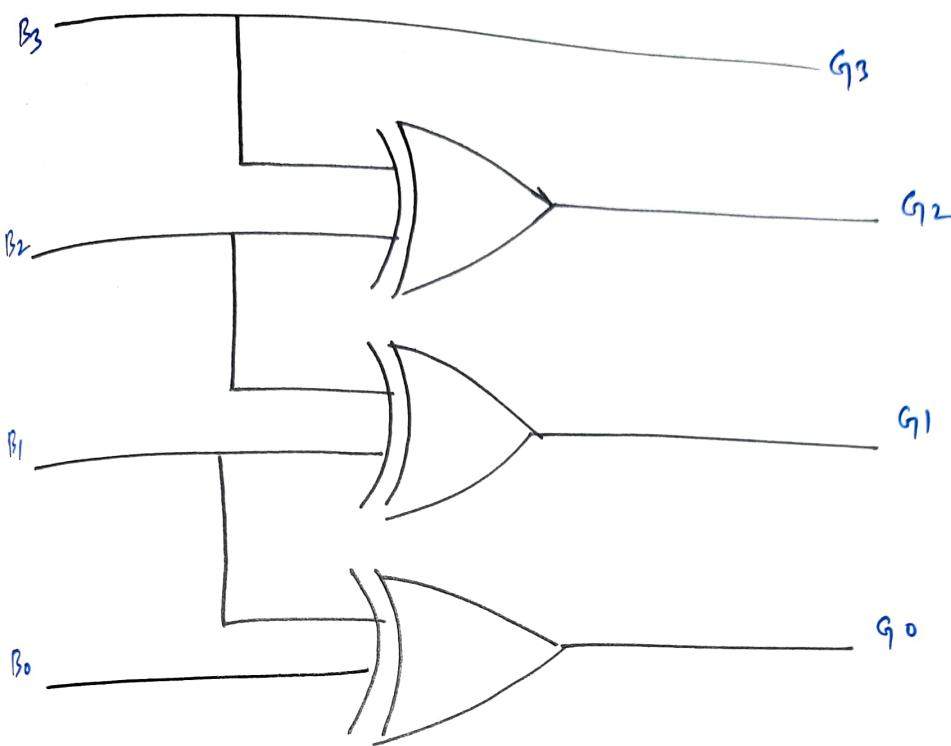
$$G_1 = B_2 \bar{B}_1 + \bar{B}_2 B_1 = B_2 \oplus B_1$$

$$G_0 = \sum m (1, 2, 5, 6, 9, 10, 13, 14).$$

$B_3 B_2$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_1 \bar{B}_0$	$\bar{B}_1 B_0$	$B_1 \bar{B}_0$	$B_1 B_0$
0		1		3	2
$\bar{B}_3 B_2$	1	5		7	6
$B_3 B_2$	4	13		15	14
$\bar{B}_3 \bar{B}_2$	12	1	11	1	10
$B_3 \bar{B}_2$	8	9			

$$G_0 = \bar{B}_1 B_0 + B_1 \bar{B}_0 = B_1 \oplus B_0$$

1)



) entity binary-to-gray is

Port (B3: in STD-LOGIC;
B2: in STD-LOGIC;
B1: in STD-LOGIC;
B0: in STD-LOGIC;
G3: out STD-LOGIC;
G2: out STD-LOGIC;
G1: out STD-LOGIC;
G0: out STD-LOGIC);

end binary-to-gray;

architecture dataflow of binary-to-gray is

begin

$G_3 \leftarrow B_3;$

$G_2 \leftarrow B_3 \text{ xor } B_2;$

$G_1 \leftarrow B_2 \text{ xor } B_1;$

$G_0 \leftarrow B_1 \text{ xor } B_0;$

end dataflow;

Objective-3 :

- Obtain the truth table.
- Derive the minimized Boolean expression.
- Draw the logic diagram for the circuit.
- Write VHDL code.

Ans.

a)

A	B	C	D	P	Q	R	S
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0

1 0 1 0

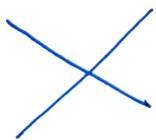
1 0 1 1

1 1 0 0

1 1 0 1

1 1 1 0

1 1 1 1



b)

$$P = \sum_m (0, 1) + d (10, 11, 12, 13, 14, 15)$$

A Karnaugh map for four variables (A, B, C, D). The columns are labeled $\bar{C}\bar{D}$, $\bar{C}D$, CD , and $C\bar{D}$. The rows are labeled $\bar{A}\bar{B}$, $\bar{A}B$, AB , and $A\bar{B}$. The map shows the following values:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$	
$\bar{A}\bar{B}$	1	1		3	2
$\bar{A}B$		4	5	7	6
AB	X	X	X	X	14
$A\bar{B}$	8	9	X	X	10

Minterms 0 and 1 are circled in the first two columns. Minterms 10, 11, 12, 13, 14, and 15 are marked with X's.

$= \bar{A}\bar{B}\bar{C}$

$$Q = \sum_m (2, 3, 4, 5) + d (10, 11, 13, 14, 15)$$

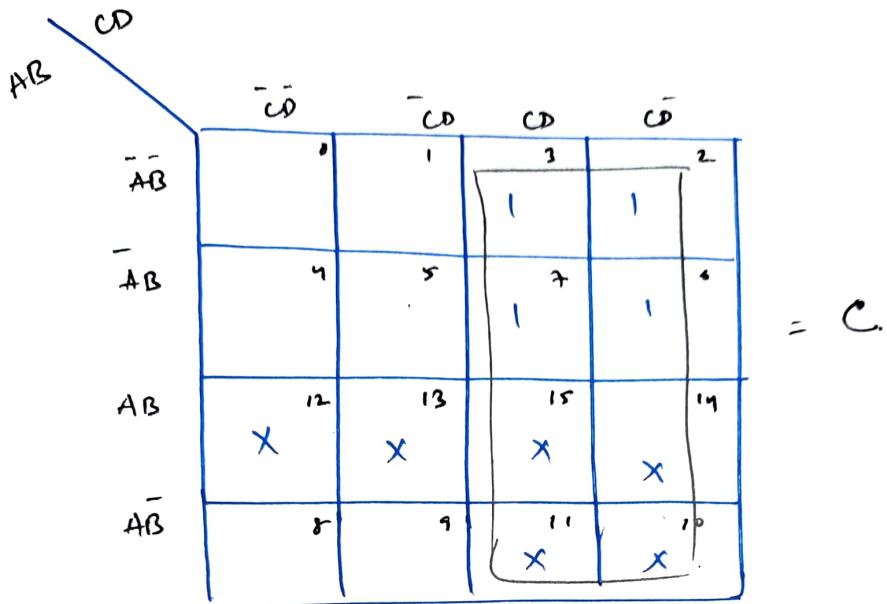
A Karnaugh map for four variables (A, B, C, D). The columns are labeled $\bar{C}\bar{D}$, $\bar{C}D$, CD , and $C\bar{D}$. The rows are labeled $\bar{A}\bar{B}$, $\bar{A}B$, AB , and $A\bar{B}$. The map shows the following values:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$	
$\bar{A}\bar{B}$			2	1	
$\bar{A}B$	4	5			6
AB	1	1			
$A\bar{B}$	X	X	X	X	14
	8	9	X	X	10

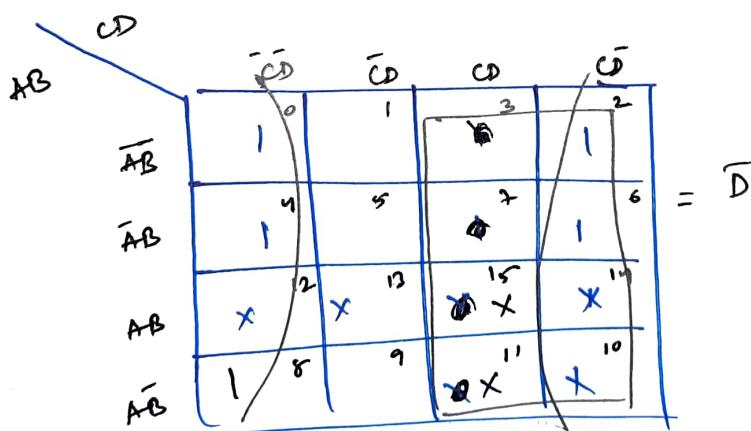
Minterms 2, 3, 4, and 5 are circled in the first three columns. Minterms 10, 11, 13, 14, and 15 are marked with X's.

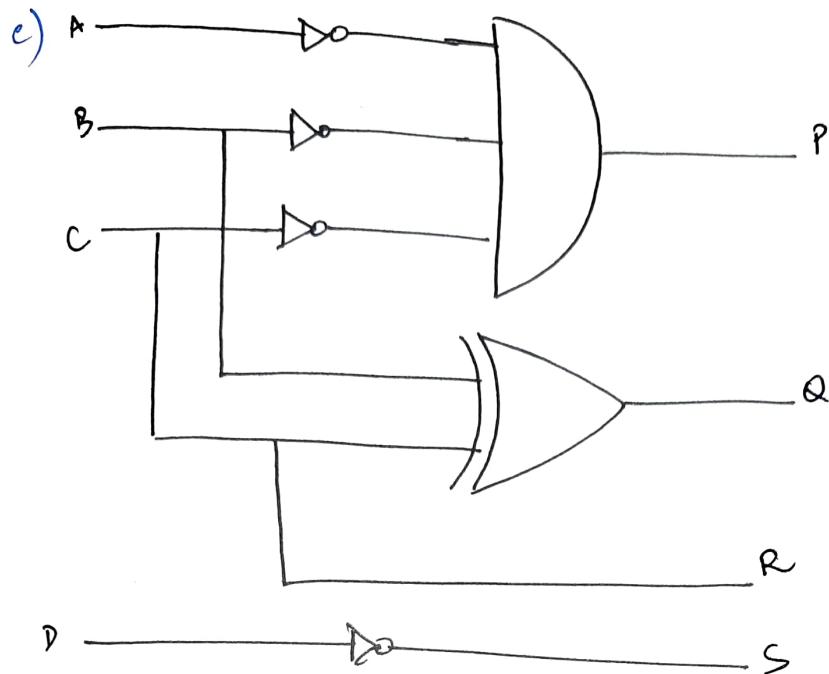
$= BC + \bar{B}C = B \oplus C$

$$R = \sum m(2, 3, 6, 7) + d(10, 11, 12, 13, 14, 15)$$



$$S = \sum m(0, 2, 4, 6) + d(10, 11, 12, 13, 14, 15).$$





d) entity BINARY_4BIT_TO_4BIT_GRAY IS

```

Port ( A: in STD_LOGIC;
      B: in STD_LOGIC;
      C: in STD_LOGIC;
      D: in STD_LOGIC;
      P: out STD_LOGIC;
      Q: out STD_LOGIC;
      R: out STD_LOGIC;
      S: out STD_LOGIC);
```

end BINARY_4BIT_TO_4BIT_GRAY;

architecture dataflow of BINARY_4BIT_TO_4BIT_GRAY is

begin

```

P <= (not A) and (not B) and C;
Q <= B xor C;
R <= C;
S <= not D;
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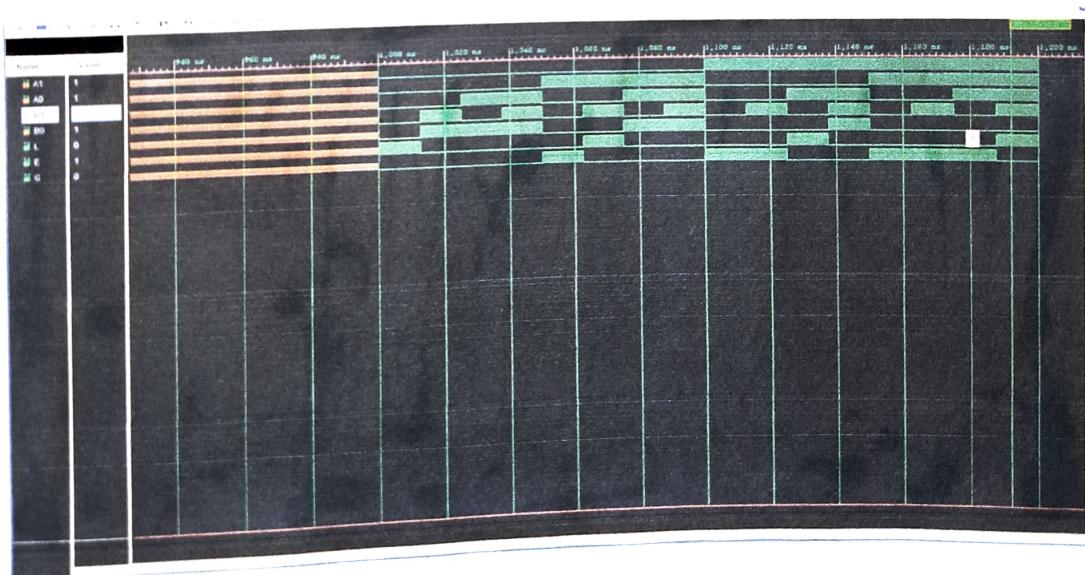
end dataflow;

III. LAB:

Software required : VHDL

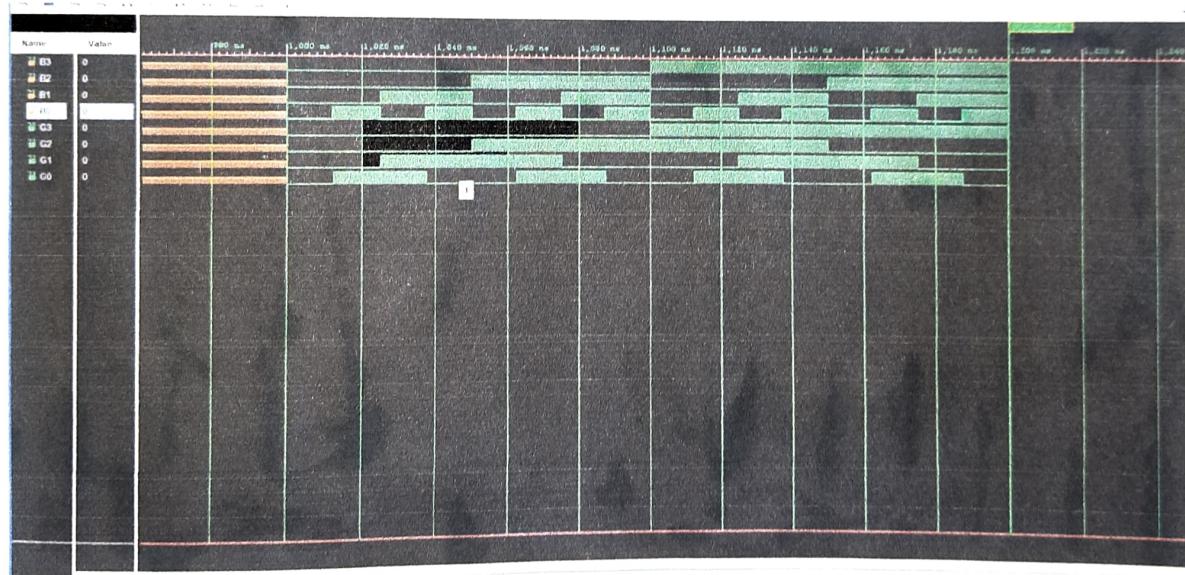
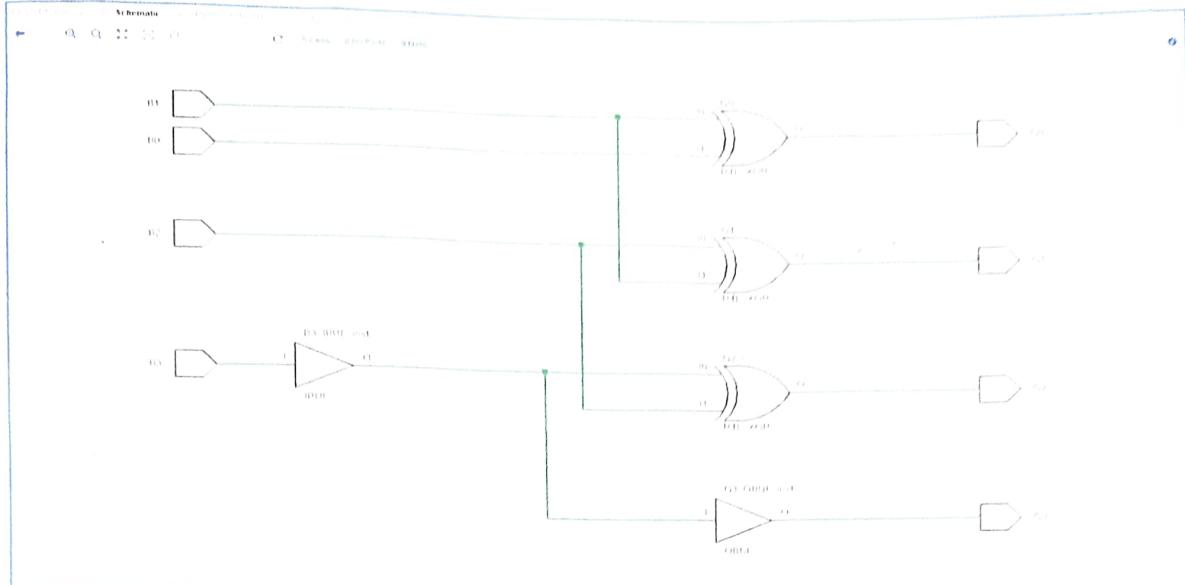
Observation :

Objective - 1 :

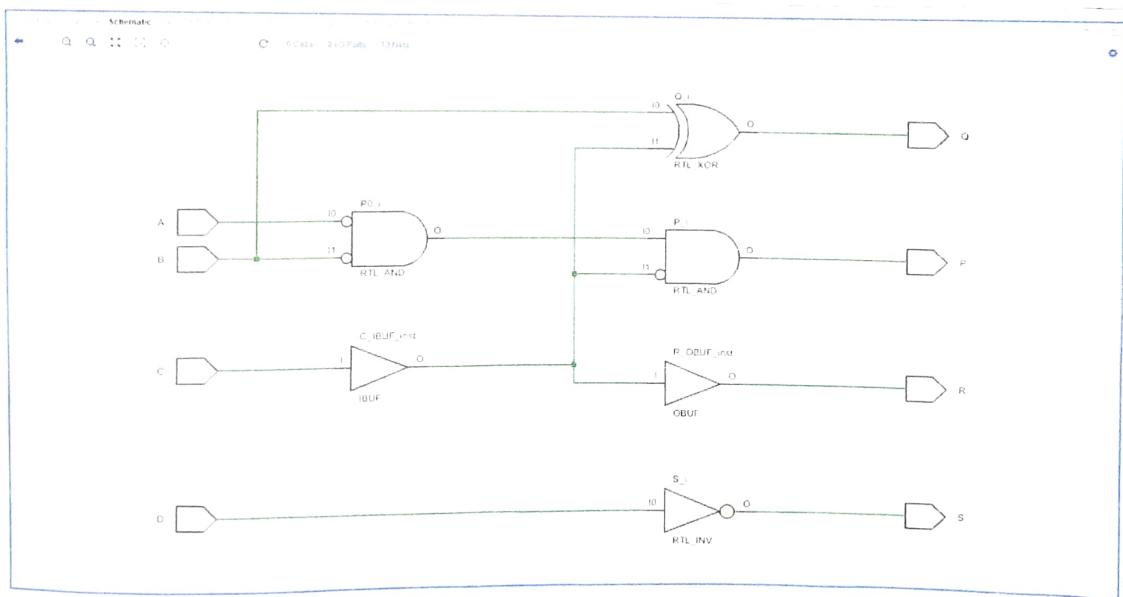


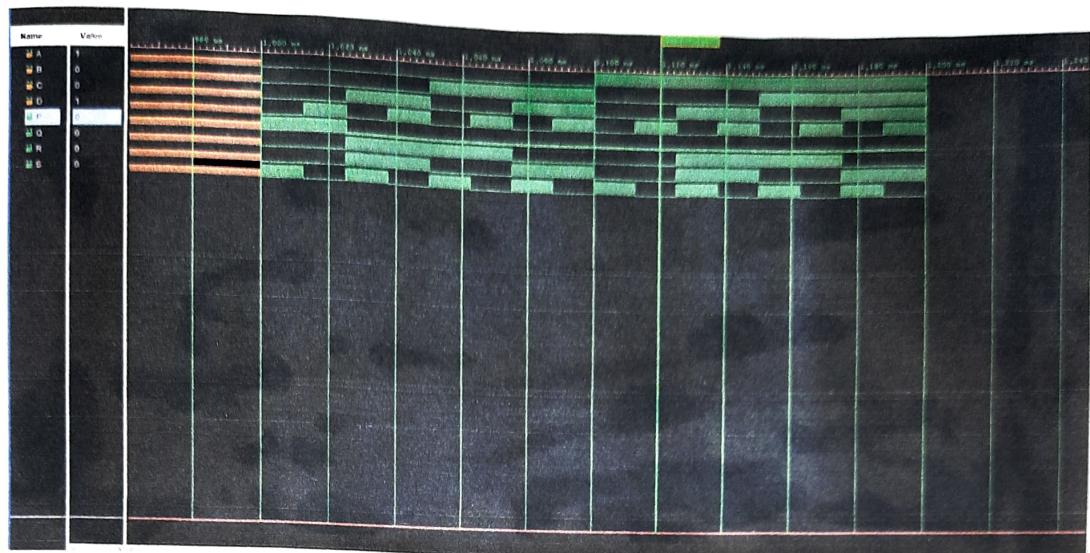
Objective-2 :

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objective-3 :





IV. CONCLUSION:

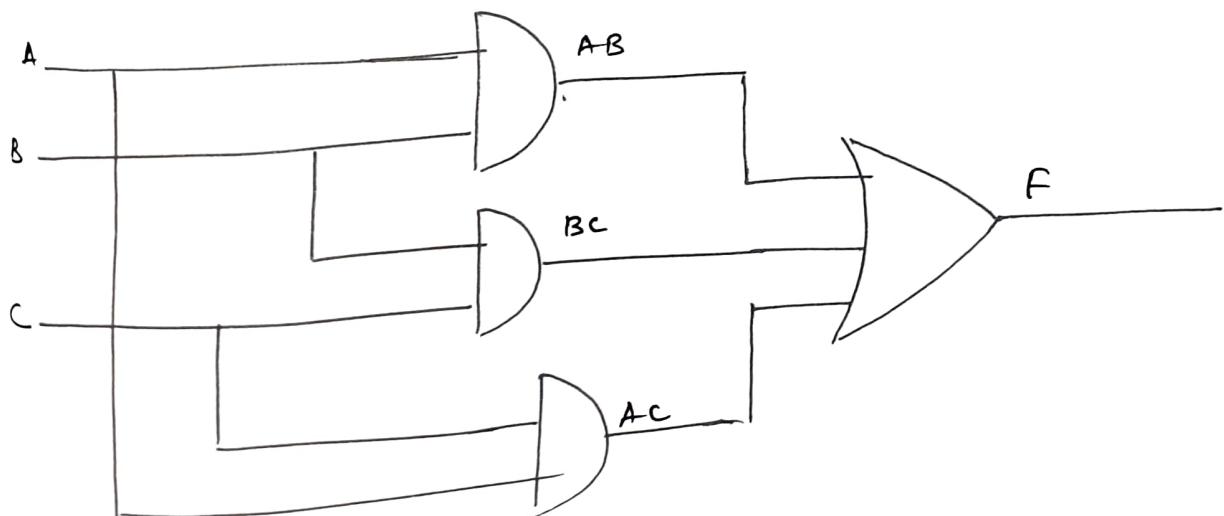
we have successfully designed 2-bit comparator, 4-bit Binary to 4-bit Gray, BCD to 9's complement generator. Each circuit's truth table, Boolean expression, logic diagrams were created and verified through VHDL simulations.

V. POST - LAB:

1. Design a 4-bit majority circuit.

<u>Ans.</u>	A	B	C	F
	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	1
	1	1	1	1

$$f = \sum_m (3, 5, 6, 7) = \overline{ABC} + A\overline{B}C + AB\overline{C} + ABC \\ = AB + BC + AC.$$



2. What is the advantages of Gray code?

Ans. It minimize switching errors, as one bit changes everytime / at a time which reduces the risk of misinterpretation in digital system. It simplifies circuit diagrams and enhances error detection compatibilities, making it ideal for applications like rotatory encoders and digital communication system.

3. Draw the logic circuit that converts a 4-bit Gray code to 4-bit Binary code.

Ans.

