DECODER:

(Reverse of Encoder)

- convert n no. of binary inputs and give 2n no. of output line (unique).

- if n bits coded information has unused combination, then the decoder may have less than 2 n output.

* No. of inputs = a?

* 2 to 4 line Decoder:

)。
*	2 line -	D,
y -	to 4 line	2
0	η μ	D3

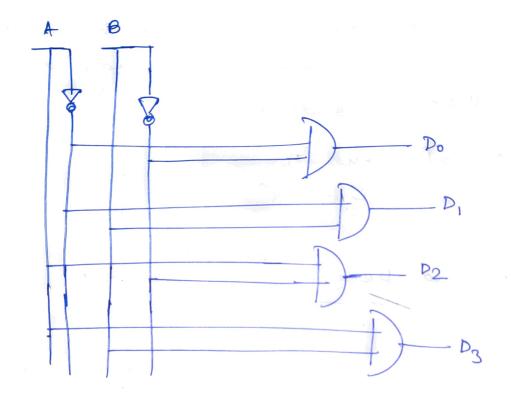
X	y	D.	\mathbb{D}_1	D2	D3
0	6	P	0	0	В
Ø	l	0	(0	0
l	0	0	~ O	1	0
()		0	0	O 1	L

$$D_0 = xy$$

$$D_1 = xy$$

$$D_2 = xy$$

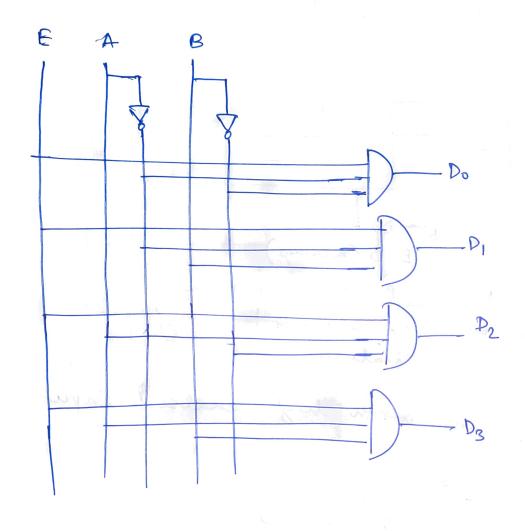
$$D_3 = xy$$



Decoder with Enabled Input: Enable F=1(always) E=O (always) off -> 1 on that off: O on that place correspondes to corresponds to Brany input Binary value. value. ex 2 to y line with high enabled enput. 0 0 0

FEETE-

 $D_0 = E \overline{A} \overline{B}$ $D_1 = E \overline{A} \overline{B}$ $D_2 = E \overline{A} \overline{B}$ $D_3 = E \overline{A} \overline{B}$



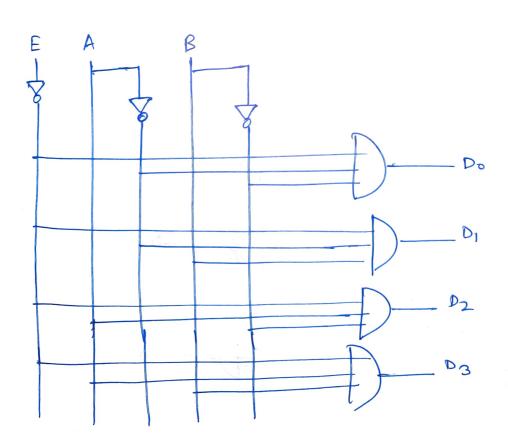
ex. 2 to 4 line with active high input.

$$D_0 = \vec{E} \cdot \vec{A} \cdot \vec{B}$$

$$D_1 = \vec{E} \cdot \vec{A} \cdot \vec{B}$$

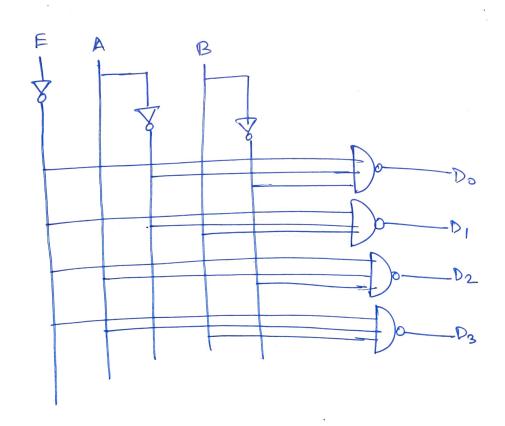
$$D_2 = \vec{E} \cdot \vec{A} \cdot \vec{B}$$

$$D_3 = \vec{E} \cdot \vec{A} \cdot \vec{B}$$

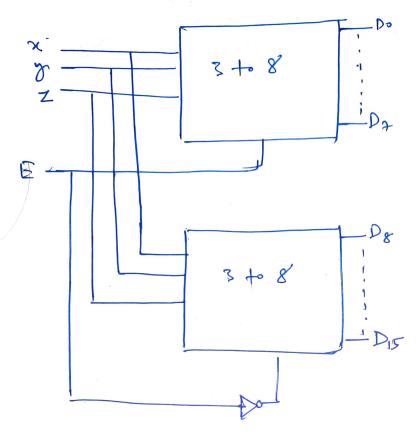


Q. Derign Q to 4 line we decoder using active low enabled NAND gate.

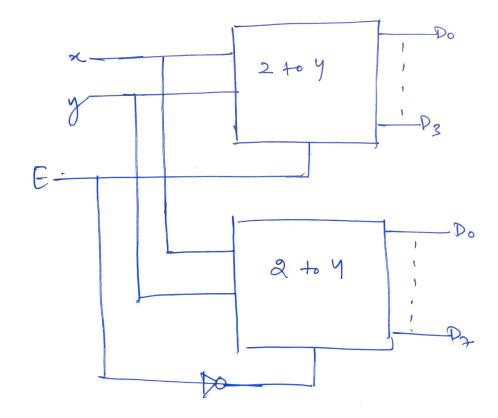
E	A	B	Do	D	D2	D ₃
1	×	×	1		1	
0	0	0	0	l	l	1
0	0	1 .	ł	0	1	1
0	1	0	1	1	0	1
0	l	1	1	1	1	0



Q. Design a full adder neing decoder. No. of inputs = 3 $sum = \sum m(1, 2, 4, 7)$ No. of output = $2^3 = 8^4$ carry = $\sum m(3, 5, 6, 7)$ Q. Derign a 4×16 decoder using two 3×8 decoder

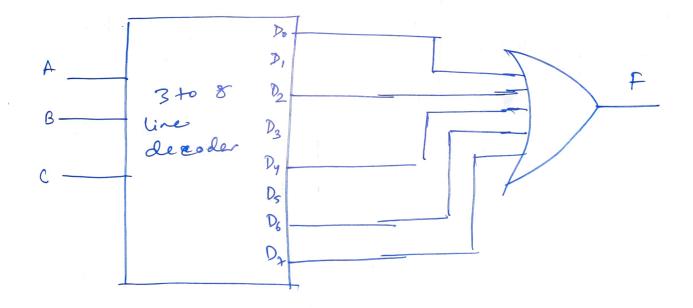


Q. Design 3 to 8 decoder veig two 2 to 4 decoder



B. Design $\mp(A_1B_1C_1) = \overline{C} + AB$ using decoder.

Any ABC \overline{C} AB $\overline{C} + AB$ 0 0 1 0 0 1



The same

Q. Constanct 5x32 decoder using four 3 to 8 line decoder with enable and a to 4 line decoder. Vie block diagram for component. 3 108 2 to y DIG 3 +0 8

& Construct 4 x16 decodor using fine 2 xy decolor with enable. D. D, 02 Dy D6 3 240 . Dg B - D11 DIZ \mathcal{D}_{13}

rice and

120