

DIGITAL LOGIC DESIGN LAB (EET1211)

LAB II: Examine and analyze the gate level minimization for Boolean function

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Marks: _____/10

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I. Objective :-

1. Construct a circuit for the Boolean function given below using basic gates and verify the truth table.

a) $F(A, B, C) = AB + AB'C$

b) $F(x, y, z) = xy + x'z + y'z$

2. Simplify the following Boolean functions to minimum no. of literals and design the circuit using minimum no. of gates..

II. Prelab :-

For each objective in prelab describe the following points.

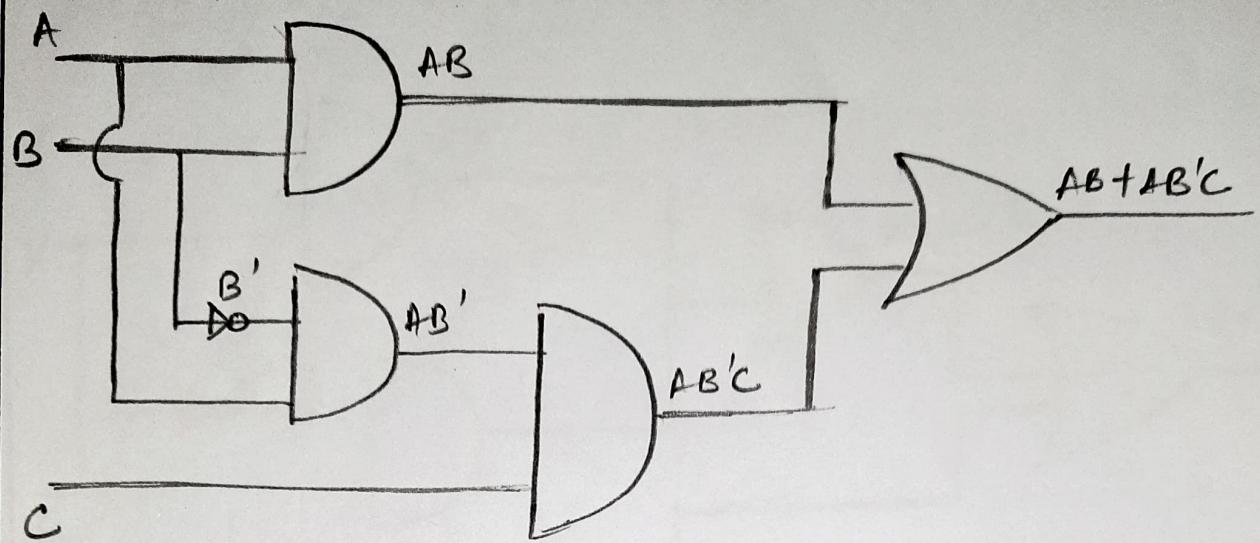
a) Draw the circuit diagram.

b) Obtain the truth table.

Ans.

a) $F(A, B, C) = AB + AB'C$.

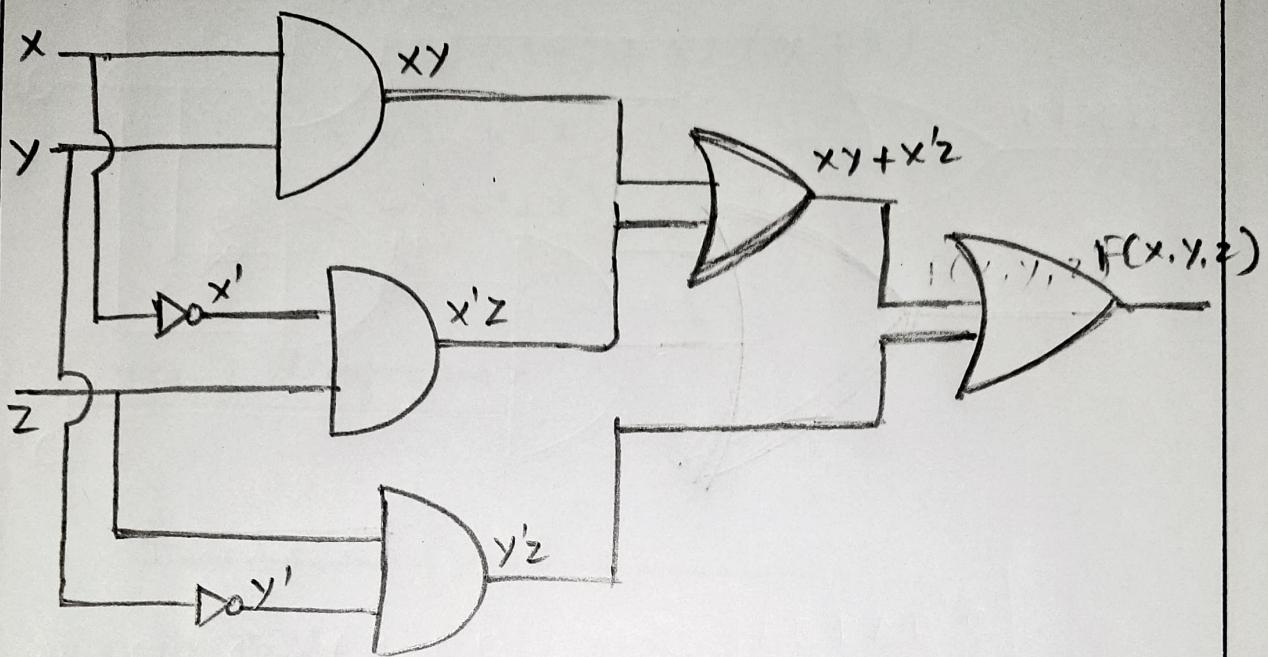
(P.T.O)



Truth table:

A	B	C	AB	B'	AB'C	AB + AB'C
0	0	0	0	1	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	1	0	1	1	1
1	1	0	1	0	0	1
1	1	1	1	0	0	1

b) $F(x, y, z) = xy + x'z + y'z$



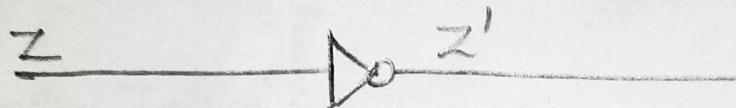
Truth table :

x	y	z	x'	y'	xy	$x'z$	$y'z$	$xy + x'z + y'z$
0	0	0	1	1	0	0	0	0
0	0	1	1	1	0	1	1	1
0	1	0	1	0	0	0	0	0
0	1	1	1	0	0	1	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	0	0	1	1
1	1	0	0	0	1	0	0	0
1	1	1	0	0	1	0	0	1

Q2.

$$\begin{aligned}
 a) F(x, y, z) &= x'y'z' + x'yz' + xy'z' + xyz' \\
 &= x'z'(y'+y) + xz'(y'+y) \\
 &= x'z' + xz' \\
 &= z'(x'+x) \\
 &= z'
 \end{aligned}$$

Circuit diagram :-



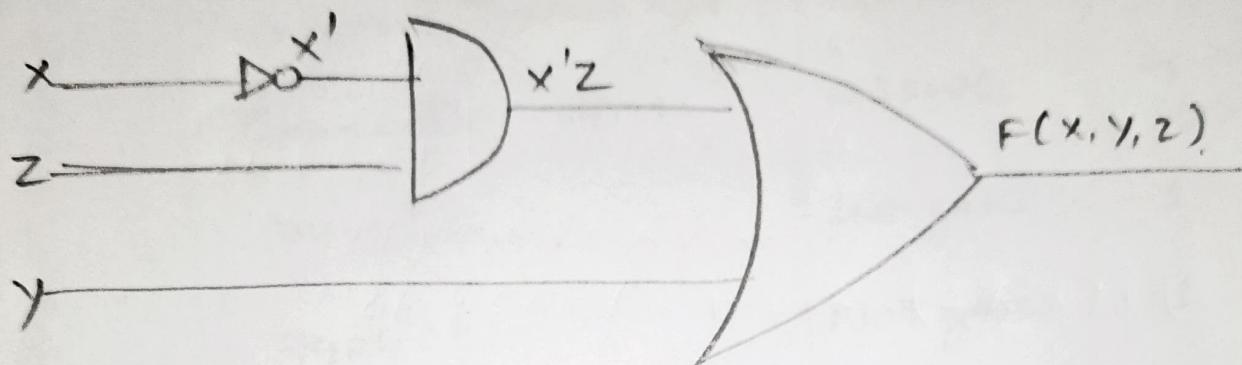
Truth Table :-

<u>z</u>	<u><u>z'</u></u>
0	1
1	0

$$\begin{aligned}
 b) F(x, y, z) &= xy'z' + x'y + x'z + yz \\
 &= y(xz' + x') + x'z + yz \\
 &= y[(x'+x)(x'+z')] + x'z + yz \\
 &= y(x'+z) + x'z + yz \\
 &= x'y + xz + x'z' + yz \\
 &= \cancel{x'y} + z(\cancel{x+x'}) + \cancel{yz} \\
 &= x'y + xz + yz + x'z \\
 &= x'y + y(z' + z) + x'z
 \end{aligned}$$

$$\begin{aligned} &= x'y + y + x'z \\ &= y + x'z \end{aligned}$$

Circuit Diagram :



Truth Table :

x	y	z	x'	$x'z$	$x'z + y$
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	0	0	1

III. LAB :-

Sl.no.	Name of the Component	Specification	Quantity
1.	Universal Trainer Kit	MicroLab	1
2.	Connecting wires	23 SWG	A few required
3.	7408 IC	AND gate	1
4.	7404 IC	NOT gate	1
5	7432 IC	OR gate	1.

OBSERVATION:-

7408 IC (AND gate) :

I/P	O/P	status
1, 2	3	working
4, 5	6	working
7, 10	8	working
12, 13.	11	working

7404 IC (NOT gate) :

<u>I/P</u>	<u>O/P</u>	<u>Status</u>
1	2	working
3	4	working
5	6	working
7	8	working
11	10	working
13	12	working

7432 IC (OR gate)

<u>I/P</u>	<u>O/P</u>	<u>Status</u>
1, 2	3	working
4, 5	6	working
9, 10	8	working
12, 13	11	working

IV. CONCLUSION :-

Objective 1 :

- i) we built the circuits for the given boolean expression using required logic gates and made the truth table.

ii) we found that the circuit worked as expected for every input combination. which shows the gates were functioning properly.

Objective 2 :

- i) First, we simplified the Boolean functions to few gates.
- ii) After constructing the logic diagrams and truth table, we found the outputs were matched the original boolean expression. which proves after simplifying Boolean functions it made our circuit simpler to construct.

V. POST-LAB :-

1. Prove the following equations using truth table.

$$(x+y)(x'+z) = xz + xy.$$

Ans.

LHS

x	y	z	x'	$x+yz'$	$x'+z$	$(x+y) \cdot (x'+z)$
0	0	0	1	0	1	0
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	1	0	1	1	1
1	1	0	0	1	0	0
1	1	1	0	1	1	1

RHS

x	y	z	x'	xz	$x'y$	$xz + x'y$
0	0	0	1	0	0	0
0	0	1	1	0	0	0
0	1	0	1	0	0	1
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	1	0	1	0	1
1	1	0	0	0	0	0
1	1	1	0	1	0	1

From, the table, we found

$LHS = RHS$ (proved)

2. Draw a circuit that uses only one AND gate and one OR gate to realise the Boolean function $F = WXYZ + VXYZ + UXYZ$.

Ans.

$$F = WXYZ + VXYZ + UXYZ \\ \Rightarrow XYZ(W + V + U)$$

