DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VII: Construct and Test the operation of various FLIP-FLOP circuits using VHDL

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: ____/10

Remarks:

Teacher's Signature

I. Objective:

1. Design and test of D flip-flop with negative edge-triggering.
2. Design and test of JK flip-flop with active low asynchronous reset and positive edge-triggering.
3. Design and test of T flip-flop with active low asynchronous reset and positive edge-triggering.

II. Pre-lab:

Obj. 1:

a) Obtain the characteristics table.
b) Derive the characteristics equation of the D flip-flop.
c) Draw the circuit diagram for the circuit.
d) Write VHDL code.

Obj. 2:

a) Obtain the characteristics table.
b) Derive the characteristics equation of the JK flip-flop.
c) Draw the circuit diagram for the circuit.
d) Write VHDL code.

Obj. 3:

a) Obtain the characteristics table.
b) Derive the characteristics equation of the T flip-flop.
c) Draw the circuit diagram for the circuit.
d) Write VHDL code.

III. LAB:

Software Required:

Observation:

Attach screenshot of Source code, Test bench, Schematic diagram, and waveform):

IV. CONCLUSION:

V. POST LAB:

1. Differentiate between a latch and a flip-flop.

2. If both inputs of a SR NOR Latch are low, what will happen to the output?

a) The output will reset.

b) The output will toggle.

c) The output will become unpredictable.

d) The output will not be changed

3. If both inputs of SR NAND Latch are low, what will happen to the output?

a) The output will reset.

b) The output will toggle.

c) The output will become unpredictable.

d) The output will not be changed

4. Which of the following describes the operation of a positive edge-triggered D-type flip-flop?

a) If both inputs are high, the output will toggle.

b) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.

c) When both inputs are LOW, an invalid state exists.

d) The output will follow the input on the leading edge of the clock.