DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VI: Design of Multiplexer, Decoder, and Encoder Circuits using VHDL

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: ____/10

Remarks:

Teacher's Signature

I. Objective:

1. Design a 2 X 1 Multiplexer that will select the binary information from one of the two input lines and direct it to a single output line based on the value of a selection line.

2. Design a 3-to-8-line decoder with active low enable input using NAND gates only.

3. Design a full adder using a 3-to-8-line decoder and external OR gates.

4. Design a 4-bit priority encoder with inputs D3 (MSB), D2, D1 and D0 (LSB) and outputs X, Y and V. The priority assigned to inputs is D3 > D2 > D1 > D0. The output V shows a value 1 when one or more inputs are equal to one. If all inputs are 0, V is equal to 0. When V=0, then other two outputs are not inspected and are specified as don't care conditions.

II. Pre-lab:

Obj. 1:

a) Obtain the truth table.
b) Derive the Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 2:

a) Obtain the truth table.
b) Derive the Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 3:

a) Obtain the truth table.
b) Derive the Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

Obj. 4:

a) Obtain the truth table.
b) Derive the Boolean expression for each output of the circuit.
c) Draw the logic diagram for the circuit.
d) Write VHDL code.

III. LAB:

Software Required:

Observation:

Attach screen-shot of Source code, Test bench code (Optional), Schematic diagram, and waveform):

IV. CONCLUSION:

V. POST LAB:

1. Design a 2-input Ex-OR gate using a 4X1 MUX.

2. Design an 8X1 MUX using a 4X1 MUX?

3. Implement the following functions using a 3-to-8-line decoder with active-high enable input:

F(a, b, c)=∑m(0,2,3,7) and G(a, b, c)=∑m(1,4,6,7)