#100rtldays Challenge

#Day_12

Design a half adder
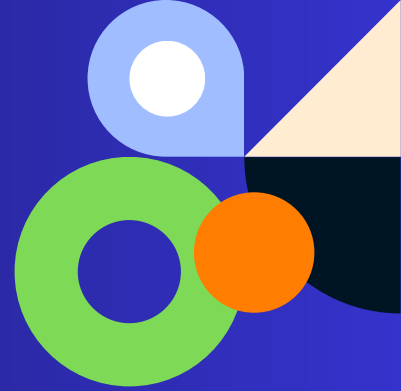
inputs :a,b

outputs :out,carry_out

DESIGN

```verilog
module half_adder(
input    a                    ,
input    b                    ,
output   out                  ,
output   carry_out)           ;

assign   out       =  a ^ b   ;
assign   carry_out =  a & b   ;
endmodule
```
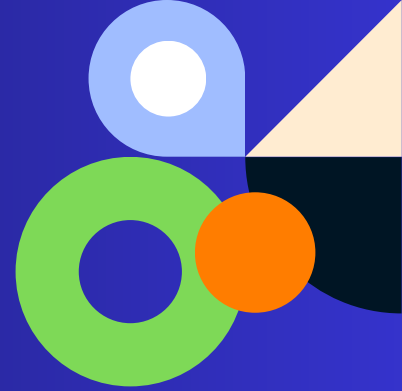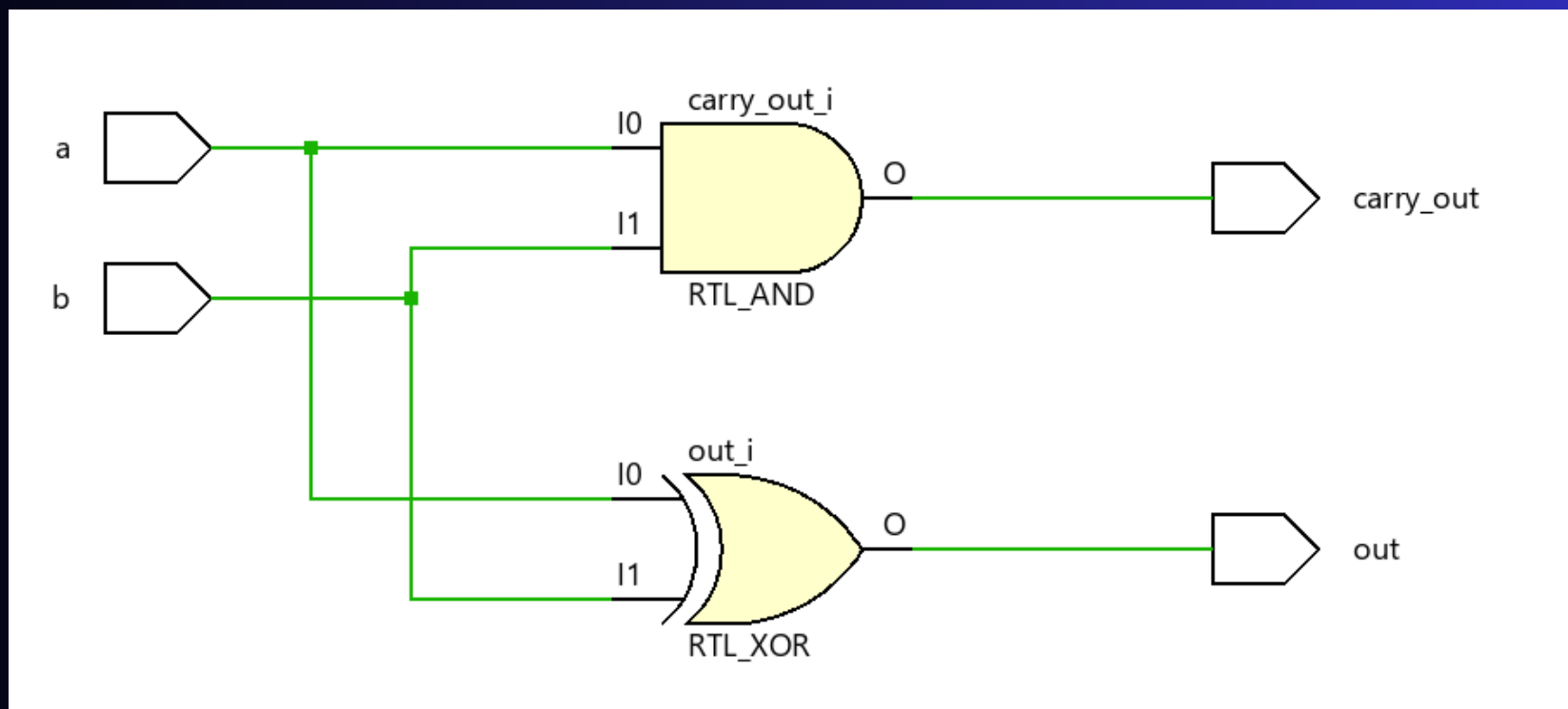
TEST BENCH

```verilog
module half_adder_tb        ;
reg   a , b                 ;
wire  out , carry_out       ;

half_adder uut(.a(a),.b(b),.out(out),.carry_out(carry_out))  ;

initial begin
      a=1'b0 ; b=1'b0 ;
#10    a=1'b0 ; b=1'b1 ;
#10    a=1'b1 ; b=1'b0 ;
#10    a=1'b1 ; b=1'b1 ;
#10
$finish                ;

end
endmodule
```

SCHEMATICS

SIMULATION