#100rtldays Challenge

_ew=vc.shortcode_view

#Day Lile1 Lisobjec

window.MdTabsView.__super

Design a 1 bit wide, 256 to 1 multiplexer. 'in' is a 256 bit vector input and output y. if sel=0; y=in[0]

sel=1; y=in[1] etc...

<u>DESIGN</u>



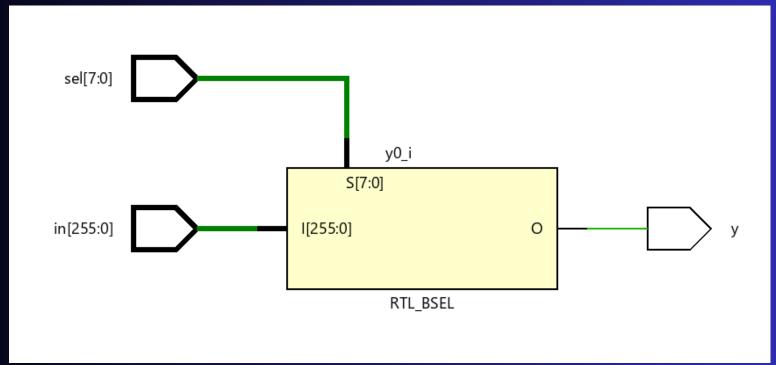
TEST BENCH



```
module mux_256_1_tb
reg [255:0] in
reg [7:0]
            sel
wire
mux_256x1 uut(.in(in),.sel(sel),.y(y))
initial begin
   in=256'hf3f6f920fcfa5
      sel = 8'd1
     sel = 8'd2
#10
     sel = 8'd3
#10
     sel = 8'd4
#10
     sel = 8'd5
#10
     sel = 8'd6
#10
#10
  $finish
end
endmodule
```

SCHEMATICS





SIMULATION

Name	Value	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns
> i n[255:0]	000000000000000000000000000000000000000						
> 💆 sel[7:0]	06	01	02	03	04	05	06
¹ ä y	0						
						 	
¥ [12]	0						
V [11]	1						
¥ [10]	1						
U [9]	1						
4 [8]	1						
¥ [7]	1						
¥ [6]	0						
¥ [5]	1						
₩ [4]	0						
W [3]	0						
₩ [2]	1						
₩ [1]	0						
₩ [O]	1						
> W sel[7:0]	06	01	02	03	04	05	06
1 6 y	0						
- ,							