100rtldaysChallenge

#DAY17 DATE: 15/10//2023

AIM:

TO DESIGN A D FLIP-FLOP.

DESIGN CODE:

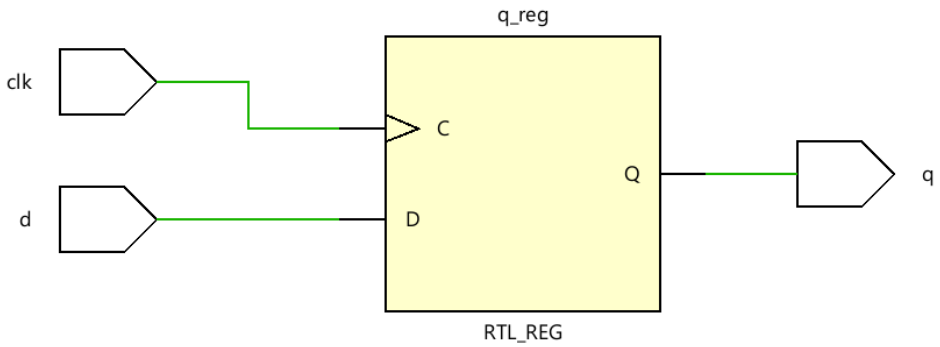
```
   //declaring d flip flop module
module D_FF(
    input       clk         , //clk input
    input       d           , //data input
    output reg q)           ; //q output

always@(posedge clk)begin  // Use a clocked always block
     q<=d                 ; // copy d to q at every positive edge of clk
    end
endmodule
```

TEST BENCH CODE:

```
module D_ff_tb                          ;

reg d                                   ;
reg clk                                 ;
wire q                                  ;
// Instantiate the D flip-flop module
D_FF uut(.d(d),.q(q),.clk(clk))         ;

// Toggle the clock signal every 5 time units
always
    #5 clk=~clk                         ;

initial begin
    clk = 0                             ;
    d   = 0                             ;

    #10 d = 1                           ;   // Apply data input
    #10 d = 0                           ;   // Change data input
```

```
    #10
 $finish                                ;
end
endmodule
```

SCHEMATICS:



SIMULATION: