100rtldaysChallenge

#DAY15 DATE: 13/10//2023

AIM:

TO DESIGN 8 'BIT 2'S COMPLEMENT ADDER ALSO CHECK WHETHER AN OVERFLOW OCCURRED OR NOT.

DESIGN CODE:

```
module day_15(
  input   [7:0] a       ,
  input   [7:0]b        ,
  output  [7:0]s        ,
  output  overflow
    )                   ;

  assign s=a+b          ;   //sum of two 8 bit vector
    //checking whether a overflow occurred .an overflow occur when both
the input are positive and the output is negative
     //or both the inputs are negative and the output is positive.
  assign overflow=(~a[7]&~b[7]&s[7]) | (a[7]&b[7]&~s[7]);
endmodule
```

TEST BENCH CODE:

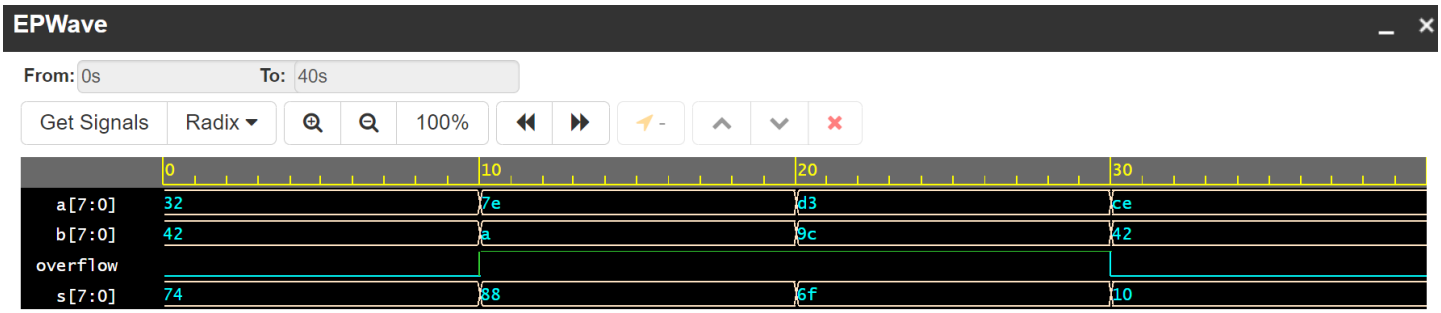
```
module day15_tb          ;
reg [7:0] a              ;
reg [7:0] b              ;
wire [7:0] s             ;
wire overflow            ;

  day_15 uut (.a(a),.b(b),.s(s),.overflow(overflow)); //instantiation
```

```
initial begin
$dumpfile("dump.vcd"); $dumpvars;
    a = 8'd50  ;   //both positive but sum less than 127
    b = 8'd66  ;   //over flow not occurred
    #10
    a = 8'd126 ;   //both positive but sum greater than 127
    b = 8'd10  ;   //overflow occurred
    #10
    a = -8'd45 ;   //both negative but sum below -127
    b = -8'd100;   //overflow occurred
    #10
    a = -8'd50 ;   //one positive and one negative but sum within -127 to
+127
    b = 8'd66  ;   //overflow not occurred
    #10
    $finish;

end
endmodule
```

SIMULATION:



Note: To revert to EPWave opening in a new browser window, set that option on your user page.