#100rtldays Challenge

#Day_11

Design a 1 bit wide, 256 to 1 multiplexer. 'in' is a 256 bit vector input and output y.

if sel=0 ; y=in[0]

sel=1 ; y=in[1] etc...

DESIGN

```
module mux_256x1(
input [255:0] in     ,
input [7:0]   sel    ,
output   reg  y
    );
always@(*)begin
      y = in[sel]    ;
 end
endmodule
```

TEST BENCH

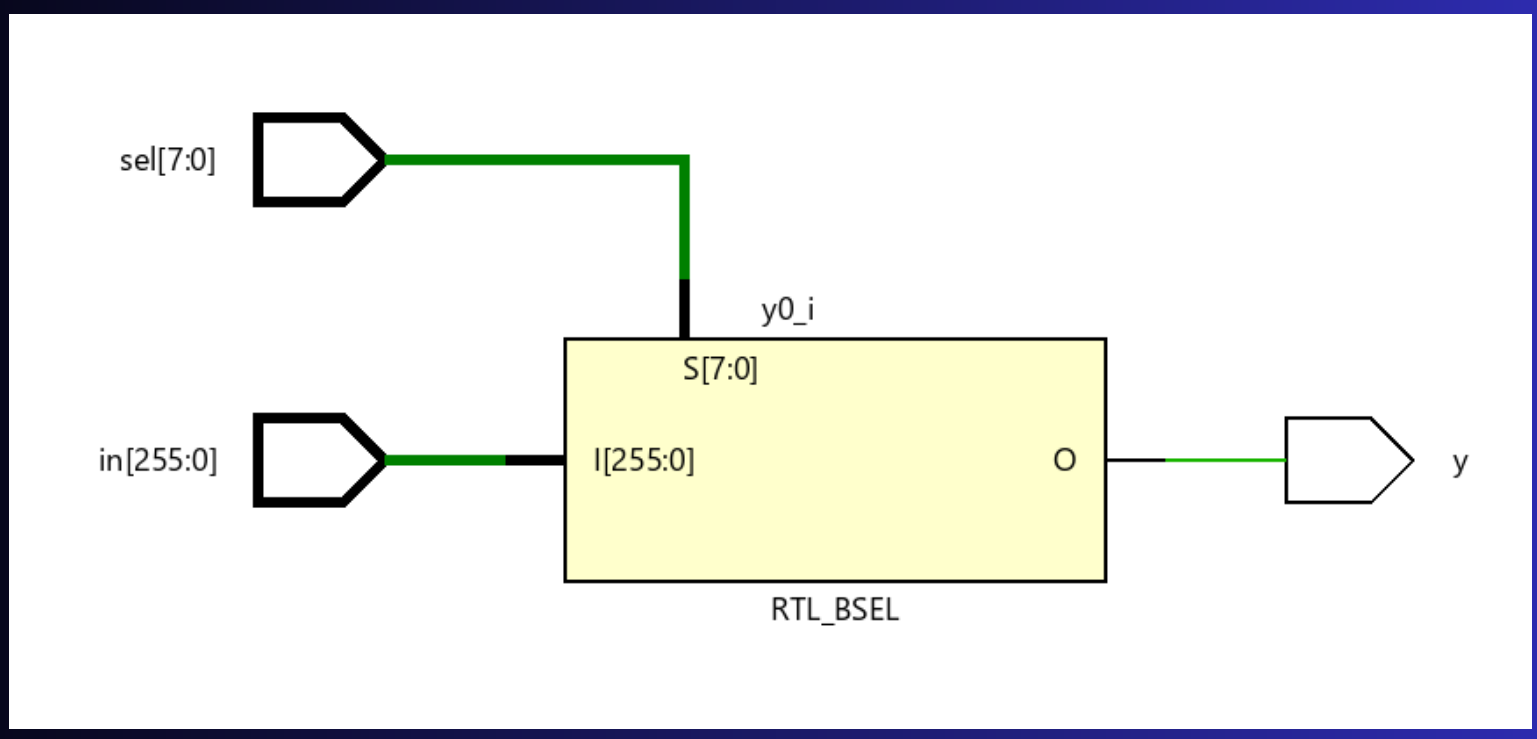
```
module mux_256_1_tb                          ;

reg [255:0] in                               ;
reg [7:0]   sel                              ;
wire        y                                ;
mux_256x1 uut(.in(in),.sel(sel),.y(y))       ;

initial begin
   in=256'hf3f6f920fcfa5                     ;

      sel = 8'd1                             ;
 #10  sel = 8'd2                             ;
 #10  sel = 8'd3                             ;
 #10  sel = 8'd4                             ;
 #10  sel = 8'd5                             ;
 #10  sel = 8'd6                             ;
 #10
   $finish                                   ;
 end
endmodule
```

SCHEMATICS



SIMULATION