#100rtldays Challenge

#Day_9

Design a 100 bit wide 2x1 multiplexer.

inputs: a,b,sel

output:y

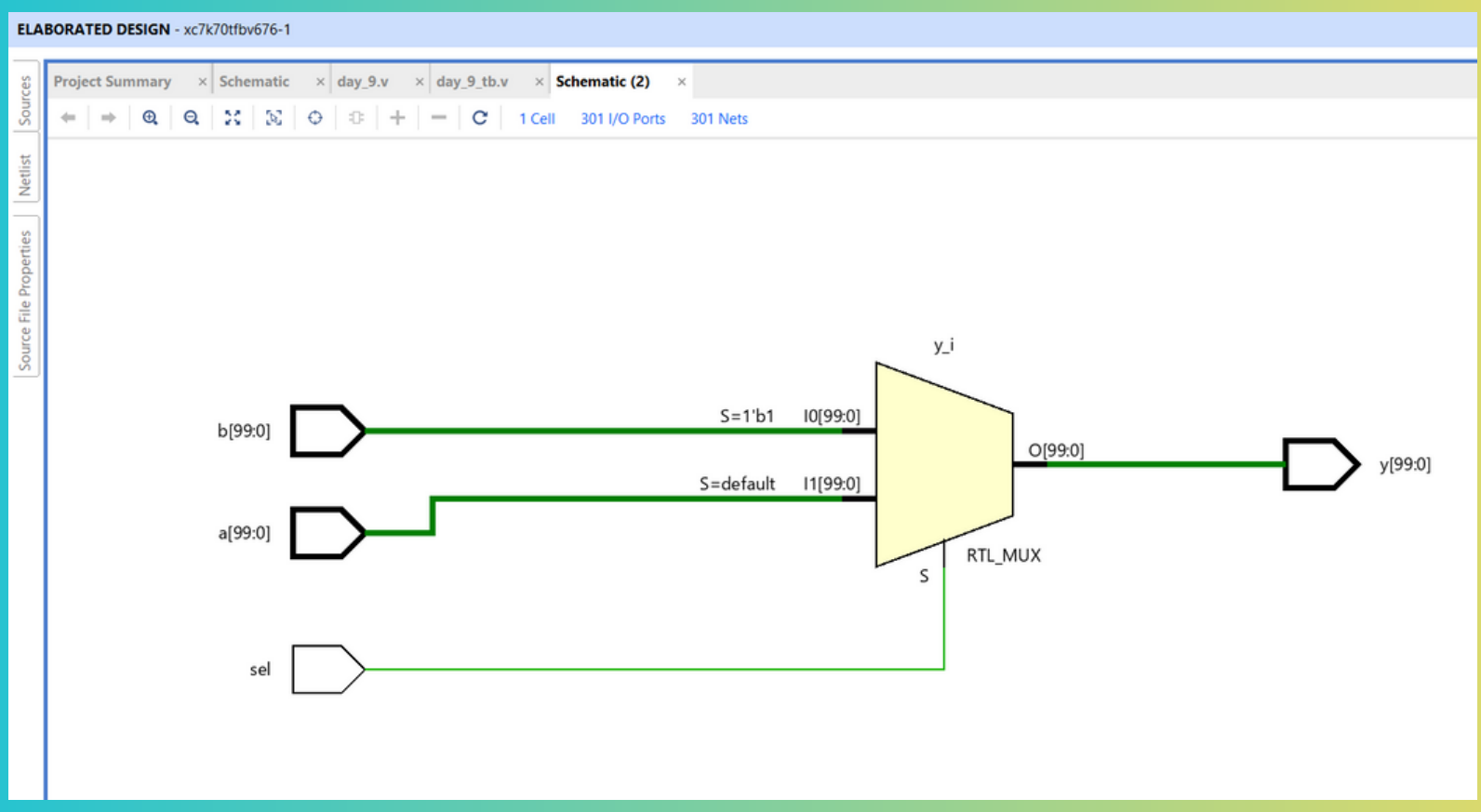
DESIGN

```
module mux2_1(
input [99:0]a          ,
input [99:0]b          ,
input sel              ,
output [99:0]y
 );

 assign y= sel ? b : a ;
//assign y = (~sel & a) | (sel & b);

endmodule
```

TEST BENCH

```
module day_9_tb                          ;
  reg   [99:0]a, b                       ;
  reg   sel=0                            ;
  wire  [99:0]y                          ;

  // Instantiate the 2:1 mux module
  mux2_1 uut(.a(a),.b(b),.sel(sel),.y(y));

 //changinig value of sel continuously

 always begin
 #5 sel=~sel                             ;
 end

  initial begin

    a = 100'd37                          ;
    b = 100'd21                          ;
    #10
    a = 100'd15                          ;
    b = 100'd55                          ;
    #10

    $finish                              ;
  end
endmodule
```

SCHEMATICS



SIMULATION