Suryansh Upadhyay

Graduate Research Assistant, Department of Electrical Engineering, The Pennsylvania State University
814-777-6641 | sju5079@psu.edu | LinkedIn | Google Scholar | ***Research Interests: Quantum computing, QML, Security*** |

Summary

Expertise in *Quantum Computing, Quantum Security, Hardware Design, ML, and Fabrication*. Proven collaboration skills with interdisciplinary teams and strong communication abilities. Actively involved in publishing and reviewing research. Proficient in quantum computers and related tools: ***Qiskit, Pennylane, Stim, Cirq, Intel Quantum SDK and CUDA-Q.***

Education

The Pennsylvania State University — August 2021 – Expected Graduation Summer 2026
Ph.D.- Electrical and Electronics Engineering; GPA: 3.8/4.0 — *University Park, State College, Pennsylvania*

Birla Institute of Technology and Science Pilani — August 2014 – July 2018
B.E. in Electronics and Instrumentation Engineering; GPA: 8.18/10 — *Pilani, India*

Skills

- **Software and Tools:** Matlab, PSpice, Cadence Virtuoso, Sentaurus TCAD
- **Industrial:** RTL Design, Physical Design
- **Languages:** Python, C, LaTeX, Verilog
- **Python Libraries:** PyTorch, Numpy, Pandas, Matplotlib, SK Learn, TensorFlow

Experience and Research

The Pennsylvania State University, *Graduate Teaching Assistant* — **Aug 2024 - present**

1. **Computing with Commercial Quantum Computers:** *Delivered lectures and interactive tutorials* to maximize student comprehension and engagement in quantum computing; led focused *doubt-clearing sessions* and *designed assignments* | *Student Engagement* | *Qiskit* | *Intel Quantum SDK* |
2. **Analog Circuit Design:** Led hands-on lab sessions focused on circuit design and simulation using *Cadence Virtuoso*
3. **Electronic Circuit Design I:** Instructed lab sessions on circuit design using *oscilloscope, DMM, signal generator*, and *breadboard*

The Pennsylvania State University, *Graduate Research Assistant* — **Aug 2021 - present**

1. **Quantum security:**
   (a) ***Machine Learning for encoding detection:*** Developed a hybrid quantum-classical ML model to detect vulnerabilities in QNNs; designed a feature extraction pipeline to analyze gate-sequence patterns, rotational angles, and qubit entanglement. | *Feature Engineering* | *Security Mitigation* | *MLP* |
   (b) ***Securing QML:*** Identified novel attack vector for *labeled training data extraction* during model training by adversaries in quantum clouds and proposed defenses | *QML* | *Pennylane* | *Classifier* | *Python* |
   (c) ***Multi-Tenant Quantum Computing:*** Identified novel attack model leveraging scheduler policies to inject Swaps. Developed defense heuristics fortifying security at scheduler level. | *Scheduler Policy* | *Optimization* | *Swap* | *Qiskit* |
   (d) ***Quantum Computation in Untrusted Cloud:*** Explored novel security threats in cloud quantum computing and developed heuristics like obfuscation etc to enhance security. Validated methods for quantum and hybrid algorithm QAOA. | *Cloud Security* | *QAOA* | *MAX-Cut problem* | *Threat Analysis* | *Security Heuristics* | *Python* |
   (e) ***Quantum Hash:*** Parameterized Quantum Circuits (PQCs) to generate quantum hash | *Qiskit* | *Pennylane* | *Python* |
2. **Community-Based Dynamic Hardware Partitioning for multi-tenant quantum computing:** Novel equitable hardware allocation leveraging community algorithms while addressing security risks, boosting hardware utilization with minimal PST reduction | *Crosstalk* | *Community Algorithms* | *Qiskit* | *Python* |
3. **Quantum compiler optimization for Trapped-ion systems:** *Program-adaptive initial mapping policy* optimizing gate execution for deep, qubit-intensive quantum programs | *Trapped-ion* | QCCD | *Optimization* | *Transpilation* |

4. **Quantum Generative Adversarial Networks (qGANs):** qGAN for *image generation* using a Parameterized Quantum Circuit (PQC) for the generator. Utilized sub-generators to create and integrate image patches (8x8 Digits dataset), optimizing training and inference times for NISQ devices. | *Pennylane* | *QML* | *qGANs* | *PyTorch* | *Qiskit* |
5. **RTL design**
   (a) ***Asymmetric FIFO with Flush Functionality:*** Designed a 128-bit FIFO with 4-bit write and 32-bit read interfaces, featuring flush mechanism for partial data handling and concurrent write support during flush operations | *Interface protocol design* | *Verilog* |
   (b) ***NoC Skid Buffer Implementation:*** Implemented a skid buffer to improve timing in a Network-on-Chip (NoC) system by registering the "ready" signal between ingress and egress ports while maintaining network throughput | *Handshake mechanisms* | *Pipeline design* | *Verilog* |
   (c) ***Request Buffer with Ordering Constraints:*** Designed a high-performance buffer module managing ordered and unordered requests between RX and TX interfaces | *Request ordering* | *Asynchronous reset handling* | *Verilog* |
   (d) ***AXI Stream Converter with Selective Buffering:*** Designed a module to convert AXI Stream responses to valid-ready requests, incorporating selective buffering and handling variable device operating modes | *Verilog* |
6. **Reinforcement learning for Finance and Portfolio management:** Worked with MDP frameworks for stock trading, focusing on optimizing returns. Leveraged a selection of actor-critic algorithms (*DDPG, A2C, PPO, SAC, TD3*) to compare performance in simulated environments. | *MDP* | *FinRL* | *Virtual Environment* | *Actor-Critic* | *Git* | *Python* |
7. **Analog front end system for ECG (0.5um CMOS) and SAR-ADC:** Engineered *low-noise*, *low-power* solutions for enhanced ECG signal detection using Cadence Virtuoso. Designed analog front end (precision IA with a low-power OTA in closed-loop), *8-bit SAR ADC*, and integrated signal conditioning block with optimized layout | *Low-power/Low-noise Design* | *ADC Design* | *Cadence Virtuoso* | *Analog Front-End* | *Layout* | *Floor-planning* |

Centre for Nano Science and Engineering, IISC Bangalore, *Research Assistant* **Sep 2018 - June 2021**

1. **Design, fabrication and characterization of AlGaN/GaN HEMT on Si for power applications:** Demonstrated *high on-current (≈10 A), ultra-low gate leakage (≈20 nA), gate width: 50 mm, 100v 3-T breakdown* AlGaN/GaN MOS-HEMTs, on 2-inch Si substrate; Experience in state of the art, fabrication and characterization tools | *Sentaurus TCAD* | *Fabrication* | *Characterization* | *Class 100 cleanroom* |

Professional Contributions and Selected Publications

Book Chapter

1. **S. Upadhyay**, M. Alam, S. Ghosh."Architectures for Quantum Information Processing" ***Handbook of Computer Architecture, Springer Nature***

Journal Publications

1. **S. Ghosh and S. Upadhyay**, A.A. Saki. "A Primer on Security of Quantum Computing." ***Proceedings of the IEEE (PIEEE); Current Status: Accepted with minor revisions; Imapct Factor: 23.2***
2. **S. Upadhyay**, S. Ghosh. "Trustworthy Computing using Untrusted Cloud-Based Quantum Hardware." ***Frontiers in Computer Science 2024; Impact Factor 3.2***
3. S. Kundu, R. Roy, Rahman, **Suryansh Upadhyay**, Topaloglu, S.E Mohney, S. Ghosh "Exploring Topological Semi-Metals for Interconnects." ***Journal of Low Power Electronics and Applications, 13(1), 16.***

Conference Presentations

1. **S. Upadhyay**, et al. "Quantum Computing and Cybersecurity Education: A Novel Curriculum for Enhancing Graduate STEM Learning", ***ASEE 2025; Acceptance Rate: 20-25%***
2. **S. Upadhyay**, S. Ghosh "Quantum Quandaries: Unraveling Encoding Vulnerabilities in Quantum Neural Networks" ***International Symposium on Quality Electronic Design (isQED) 2025 ; Acceptance rate: 25%***
3. **S. Upadhyay**, S. Ghosh "Quantum Data Breach: Reusing Training Dataset by Untrusted Quantum Clouds" ***isQED 2025; ; Acceptance rate: 25%***
4. **S. Upadhyay**, S. Ghosh "SHARE: Secure Hardware Allocation & Resource Efficiency in Quantum Systems" ***International Conference of Quantum Computing and Engineering (QCE) 2024***

5. **S. Upadhyay**, S. Ghosh "Stealthy SWAPs: Adversarial SWAP Injection " ***International Conference on VLSI Design (VLSID) 2024; Acceptance rate: 20%***
6. **S. Upadhyay**, R. Roy, S. Ghosh . "Designing Hash and Encryption Engines using Quantum Computing." ***VLSID 2024, ; Acceptance rate: 20%***
7. **S. Upadhyay**, and S. Ghosh. "Obfuscating Quantum Hybrid-Classical Algorithms for Security & Privacy."***isQED 2024; ; Acceptance rate: 25%***
8. **S. Upadhyay**, and S. Ghosh. "Robust and Secure Hybrid Quantum-Classical Computation on Untrusted Cloud-Based Quantum Hardware." ***Hardware and Architectural Support for Security and Privacy (HASP) 2022, ; Acceptance rate: 30%***
9. **S. Upadhyay**,A.A. Saki, R.O. Topaloglu and S. Ghosh."An Efficient Initial mapper to Reduce the Number of Shuttles in Trapped-Ion Quantum Computers." ***Great Lakes Symposium on VLSI (GLSVLSI) 2022; Acceptance rate: 25%***
10. **S. Upadhyay**,R. Baby,et. el"500V AlGaN/GaN HEMT on silicon with ultralow gate leakage." ***5th International Conference on Emerging Electronics(IEEE-ICEE 2020.)*** **Awarded as the best poster**
11. Rijo Baby,**Suryansh Upadhyay**,et. el"Process issues and passivation effects in large-periphery 5 A, 100 V AlGaN/GaN HEMT on silicon." *5th International Conference on Emerging Electronics(IEEE-ICEE 2020).*

Provisional Patents

1. **Upadhyay, S.**, Ghosh, S., "Trustworthy Computing using Untrusted Cloud-Based Quantum Hardware", Provisional Patent App: 63/498,659, 2023.
2. **Upadhyay, S.**, Ghosh, S., "Obfuscating Quantum Hybrid-Classical Algorithms for Security and Privacy", Provisional Patent App: 63/498,657, 2023.
3. **Upadhyay, S.**, Ghosh, S., "Robust and Secure Hybrid Quantum-Classical Computation on Untrusted Cloud-Based Quantum Hardware", Provisional Patent App: 63/498,664, 2023.

Tutorial Presentation

1. Led hands-on IBMQ quantum circuit demonstration and cross-talk fault injection demo. *Design, Automation and Test in Europe Conference (**DATE 2022**)*

Guest Lecture

1. Delivered a comprehensive lecture on Quantum Computing and Security. *IIT Roorkee, India(2023)*

Services

1. **Technical Program Committee (TPC):** Served as a TPC member for QSYS track. *International Conference of Quantum Computing and Engineering (**QCE 2024**); Appointed to serve as a TPC member (**QCE 2025**)*
2. **Reviewer:** Journals: ***MICRO, CAL, TQE***; Conferences: ***HOST, DAC, HASP, VLSID, DATE, QCE***

Leadership and Awards

1. **Engineering Graduate Student Council** **Fall 2022 – Fall 2024**
   College of Engineering Research Symposium(CERS 2023,2024), Chair *Penn State University*
   1. Led organization and planing of annual research symposium hosting 200+ attendees, securing $8000+ in funding. Enlisted CEO of SpotLESS Materials as keynote speaker.
   2. Collaborated with faculty and graduate students to curate a diverse range of research topics and high-quality presentations, managing abstract recruitment and program development.
   3. Acted as the primary liaison for CERS, handling communication with presenters, attendees, and industry partners.

   | *Project leadership* | *Elevator pitch* | *Event management* | *Stakeholder engagement* |
2. **Melvin P. Bloom Memorial Graduate Fellowship** **2024**
   Awarded Bloom fellowship for academic and research excellence *Penn State University*
3. **5th International Conference on Emerging Electronics(IEEE-ICEE)** **2020**
   ***Best poster award** for "500V AlGaN/GaN HEMT on silicon with ultralow gate leakage"* *Indian Institute of Science*