Assignment 1- Basic introduction to IC of microcontroller and microprocessor kit.

Submitted By
Group no. 3

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MC 1489p

Specifications

Product Attribute Attribute Value

Manufacturer: ON Semiconductor

Product Category: RS-232 Interface IC

RoHS: N

Mounting Style: Through Hole

Package/Case: PDIP-14

Specifications

Height: 3.68 mm (Max)

Length: 19.56 mm (Max)

Supply Type: Single Supply

Width: 6.6 mm (Max)

Brand: ON Semiconductor

Operating Supply Voltage: 5 V

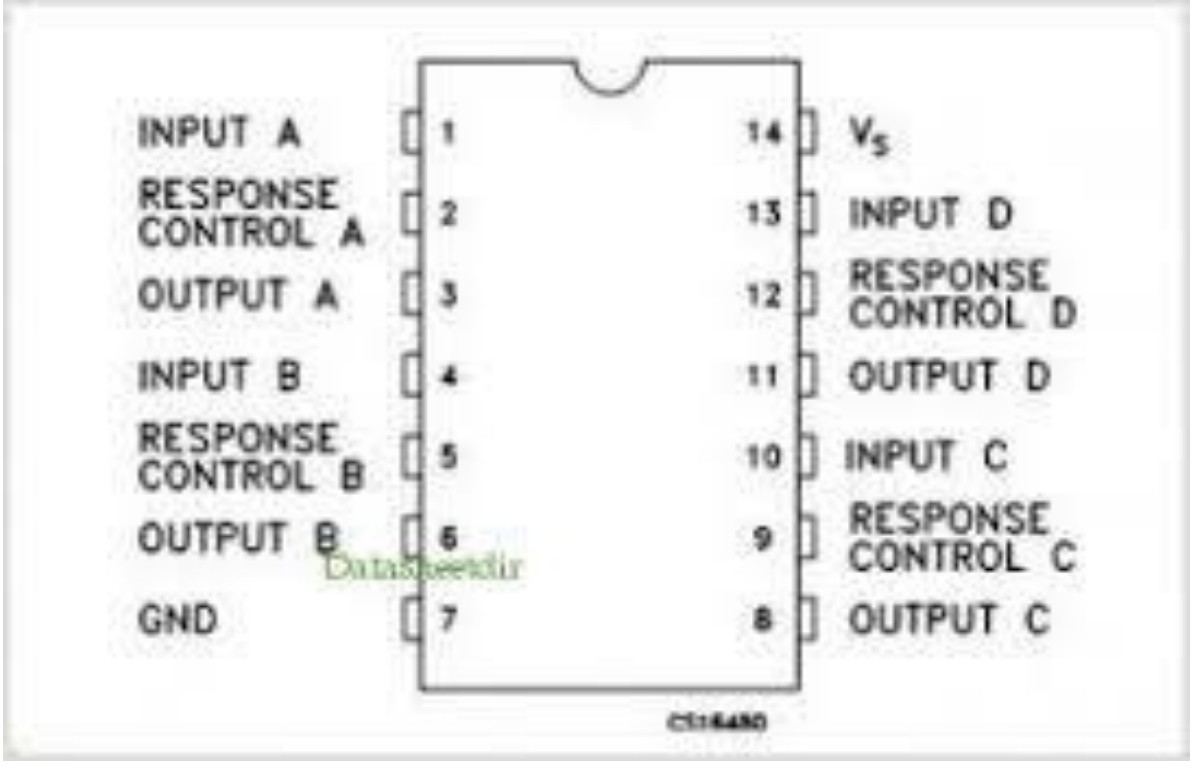
Product Type: RS-232 Interface IC

Factory Pack Quantity: 500

Subcategory: Interface ICs

Unit Weight: 1.620 g

Pin configuration



DS 1488N MC1488P

Specifications

Product Attribute Attribute Value

Manufacturer: ON Semiconductor

Product Category: RS-232 Interface IC

RoHS: N

Mounting Style: Through Hole

Package/Case: PDIP-14

Specifications

Function: Driver

Number of Drivers: 1 Driver

Operating Supply Current: 34 mA

Minimum Operating Temperature: 0 C

Maximum Operating Temperature: + 75 C

Packaging: Tube

Height: 3.68 mm (Max)

Length: 19.56 mm (Max)

Output Type: Single-Ended.

Product: RS-232.

DriversSubcategory: Interface ICs

Unit Weight: 1.620 g

Supply Type: Dual Supply

Width: 6.6 mm (Max)

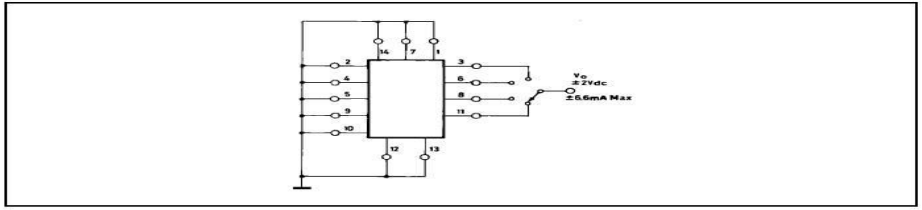
Brand: ON Semiconductor

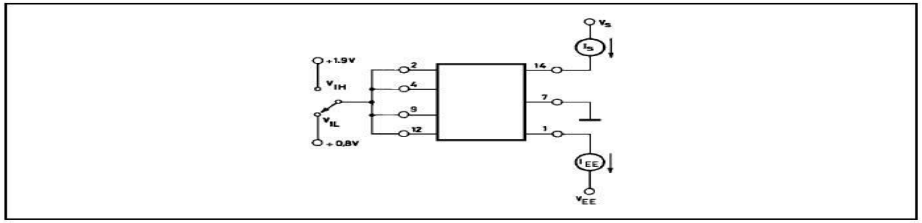
Product Type: RS-232 Interface IC

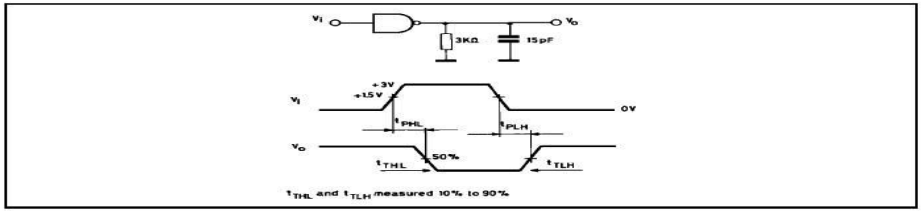
Protocol Supported: RS-232

Factory Pack Quantity: 500

Pin configuration







89C2051

Specifications

Lead Count: 20
Package Type: SOIC
Temp Range: -40C to +85C
Packing Media: Tape and reel (1000)

It is 8 bit microcontroller.

Manufactured by Atmel corporation

Specifications

arrowCompatible with MCS-51 Products
arrow2K Bytes of Reprogrammable Flash Memory
arrow2.7 to 6V Operating Range
arrowFully Static Operation: 0 Hz to 24 MHz
arrowTwo-level Program Memory Lock
arrow128 x 8-bit Internal RAM
arrow15 Programmable I/O Lines
arrowTwo 16-bit Timer/Counters
arrowSix Interrupt Sources
arrowProgrammable Serial UART Channel
arrowDirect LED Drive Outputs
arrowOn-chip Analog Comparator
arrowLow-power Idle and Power-down Modes
arrow20-pin DIP

About.

All four ports in the AT89C51 and AT89C52 are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer. The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content. All the Port 3 pins, and two Port 1 pins (in the AT89C52)are multifunctional. The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin is stuck at 0. It has less complex feature than other microprocessor.

Pin configuration

Pin Number	Description	9	P3.5 - Port 3 - T1.	18	p1.6 port 1
1	RESET - Reset	10	GND - Ground.	19	p1.7 Port 1
2	P3.0 - Port 3 - RXD	11	P3.7 - Port 3.	20	vcc positive supply
3	P3.1 - Port 3 - TXD	12	P1.0 - Port 1 - AIN0		
4	XTAL2 - Crystal	13	P1.1 - Port 1 - AIN1		
5	XTAL1 - Crystal	14	P1.2 - Port 1		
6	P3.2 - Port 3 - INT0	15	P1.3 - Port 1		
7	P3.3 - Port 3 - INT1	16	P1.4 - Port 1		
8	P3.4 - Port 3 - TO	17	P1.5 - Port 1		

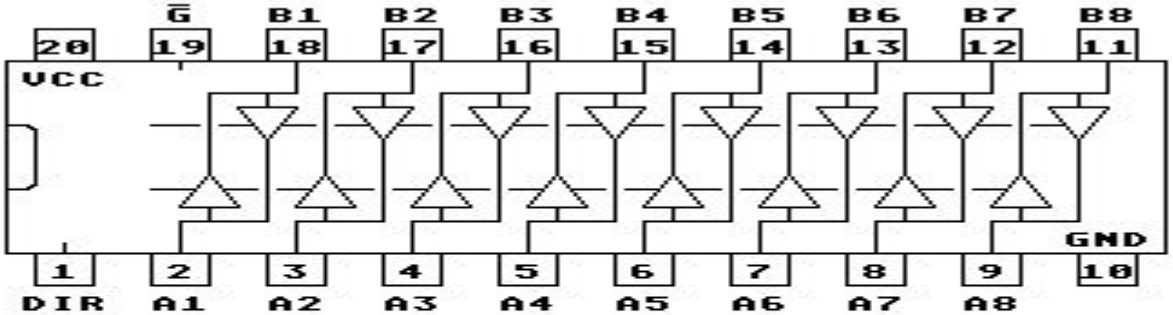
74245

Specifications

- **1** bidirectional bus transceive in a High density of 20 pin package.
  2 3 State output drive bus lines directly.
  3 pnp input reduce DC loading on bus line.
  4 hysterics at bus input reduce noise margin.
  5 typical proportion delay time 8ns.
  6 typical enable disable time 17 ns.
  7 sinc current 24mA a source current -15mA.

Pin configuration

74245 Octal Bus Transceiver



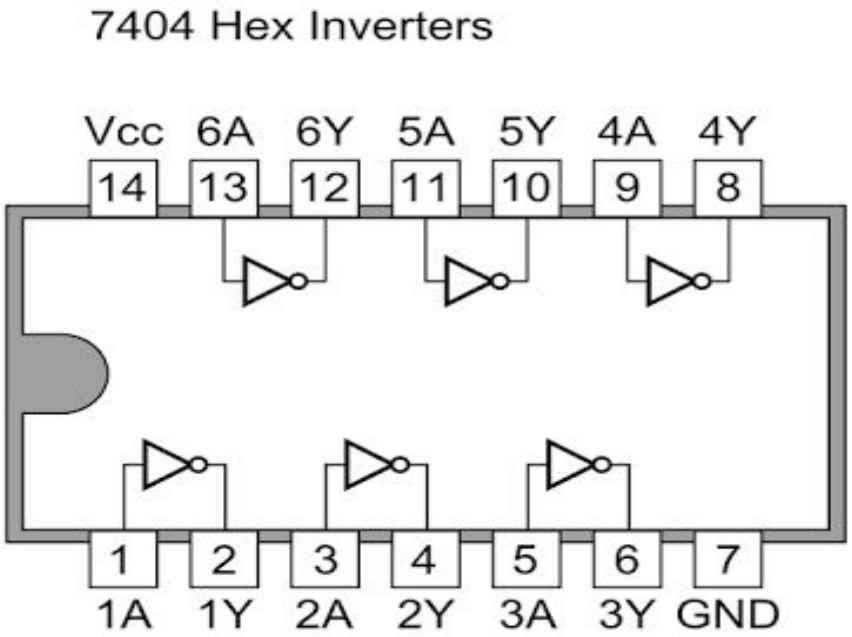
Truth Table		
$\overline{G}$	DIR	Output
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

7404 ic

Specifications.

The hex inverter is an integrated circuit that contains six (hexa-) inverters. For example, the 7404 TTL chip which has 14 pins.

Not gate is use



1403

A precision band–gap voltage reference designed for criticalinstrumentation and D/A converter applications. This unit is designed to workwith D/A converters, up to 12 bits in accuracy, or as a reference for powersupply applications.• Output Voltage: 2.5 V "25 mV• Input Voltage Range: 4.5 V to 40 V• Quiescent Current: 1.2 mA Typical• Output Current: 10 mA• Temperature Coefficient: 10 ppm/°C Typical• Guaranteed Temperature Drift Specification• Equivalent to AD580• Standard 8–Pin DIP, and 8–Pin SOIC PackageTypical Applications• Voltage Reference for 8 to 12 Bit D/A Converters• Low TC Zener Replacement• High Stability Current Reference• Voltmeter System Reference.

Specifications

Product Attribute Attribute Value

Manufacturer: Microchip

Product Category: SPLD - Simple Programmable Logic Devices

RoHS: Details

Product: ATF16V8C

Number of Macrocells: 8

Maximum Operating Frequency: 62 MHz

Propagation Delay - Max: 15 ns
Operating Supply Voltage: 5 V
Minimum Operating Temperature: - 40 C
Maximum Operating Temperature: + 85 C
Mounting Style: Through Hole
Package/Case: PDIP-20
Packaging: Tube
Height: 4.95 mm
Length: 26.92 mm
Width: 7.11 mm
Brand: Microchip Technology / Atmel
Operating Supply Current: 105 mA
Product Type: SPLD - Simple Programmable Logic Devices

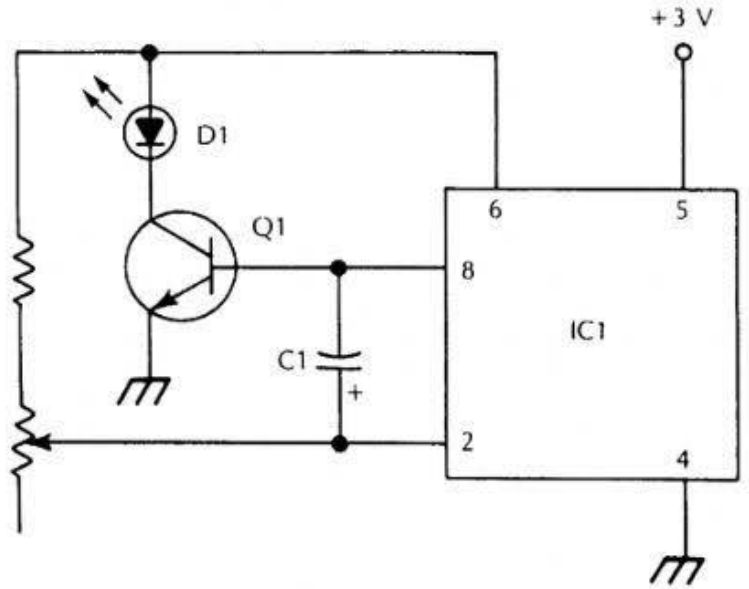
IC diagram

Subcategory: Programmable Logic ICs

Supply Voltage - Max: 5.5 V

Supply Voltage - Min: 4.5 V

Unit Weight: 2.260 g



IC1	LM3909 LED flasher/oscillator IC
Q1	NPN transistor (2N3904, Radio Shack RS2009 or similar)
D1	LED
C1	100 µF 5 V electrolytic capacitor
R1	470 Ω ¼ W 5% resistor
R2	50 kΩ potentiometer

W27C512 70

The W27C512 is a high speed, low power Electrically Erasable and Programmable Read OnlyMemory organized as 65536× 8 bits that operates on a single 5 volt power supply. The W27C512provides an electrical chip erase function.

FEATURES•

High speed access time:45/70/90/120 nS (max.)•.
Read operating current: 30 mA (max.)•
Erase/Programming operating current30 mA (max.)•
Standby current: 1 mA (max.)• Single 5V power supply
14V erase/+12V programming voltage• Fully static operation• All inputs and outputs directly TTL/CMOScompatible• Three-state outputs•
Available packages: 28-pin 600 mil

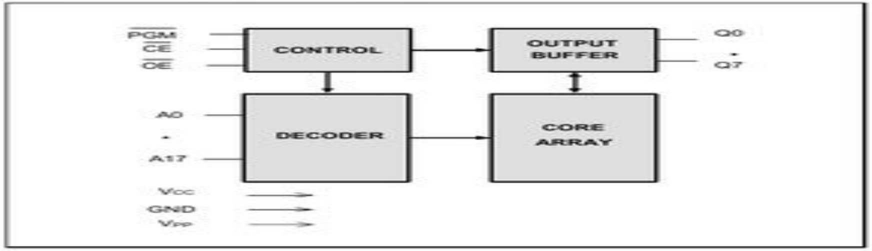
Pin configuration

le 5V power supply

• Available packages: 32-pin 600 mil DIP and PLCC

CONFIGURATIONS

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A17	Address Inputs
Q0–Q7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Program/Erase Supply Voltage
VCC	Power Supply
GND	Ground

Publication Release Date: September 1998
Revision A1

HY6264A LP10

SPECIFICATIONS

Mfr

Package Description 0.600 INCH, PLASTIC, DIP-28

REACH Compliant Yes.

Status Discontinued

Sub Category SRAMs

Access Time-Max 100.0 ns.

I/O Type COMMON

ESD-30 Code R-PDIP-T28

JESD-609 Code e0

Memory Density 65536.0 bit

Memory IC Type STANDARD SRAM.

Memory Width 8

Number of Functions 1

Number of Ports 1

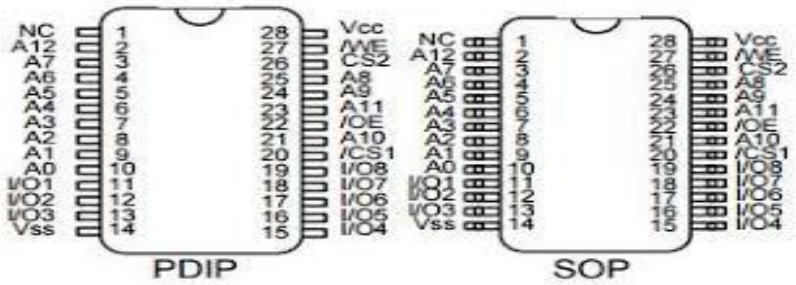
Number of Terminals 28

Specifications.

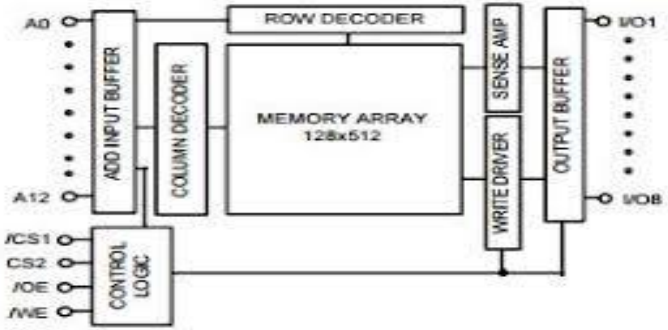
Number of Words	8192.0 words
Number of Words Code	8K
Operating Mode	ASYNCHRONOUS
Operating Temperature-Min	0.0 Cel
Operating Temperature-Max	70.0 Cel
Organization	8KX8
Output Characteristics	3-STATE
Output Enable	YES
Package Body Material	PLASTIC/EPOXY
Package Code	DIP
Package Equivalence Cod	DIP28,.6
Power Supplies (V)	5

Pin configuration

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select 1	I/O1-I/O8	Data Input/Output
CS2	Chip Select 2	Vcc	Power(+5V)
/WE	Write Enable	Vss	Ground
/OE	Output Enable	NC	No Connect
A0-A12	Address Inputs		

7437

Features s Choice of 8 latches or 8 D-type flip-flops in a single package s 3-STATE bus-driving outputs s Full parallel-access for loading s Buffered control inputs s P-N-P inputs reduce D-C loading on data lines.

IC.

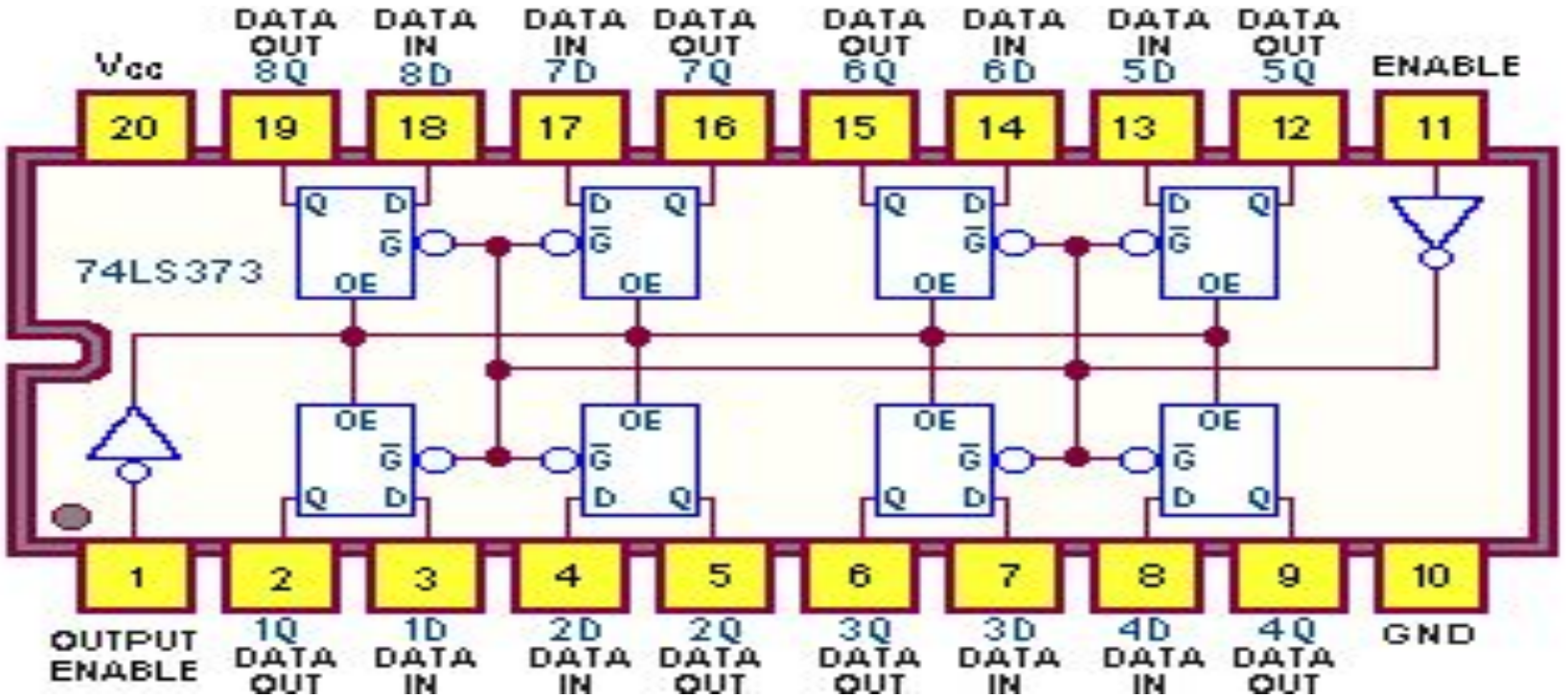
Transistor transistor logic

Latch and D type flip flop

VCC min4.75 vcc max5.25

Pin 20 operating temperature 0 _70

Pin configuration



NEC 82C55AC -2 221

- It is a CMOS programmable peripheral interface
- It is a general purpose input output device.
- It can be used with 8/16 bit CPU.
- It has 24 programmable input output pin
- It is compatible with 80xx series microprocessor.
- It has direct bit set reset compatibility.
- It is TTL compatible.
- It requires single +5v (±10%) power supply.
- It’s programmable I/O pins that interface peripheral equipment with CPU.

Pin configuration of 82C55AC -2 221

- It is a 40 pin IC
- 24 I/O pins may be individually configured into two groups of 12 each.
- Each group has major mode of operation 0, 1 and 2.
- In mode 0 each group of 12 I/O pins may be programmed in sets of four inputs or four outputs.
- In mode 1 each group of 12 I/O pins may be grouped as 8 bit I/O data port and one 4 bit control/ status port.
- Mode 2 is used in group A only, as one 8 bit bidirectional port as one 5 bit control status port.

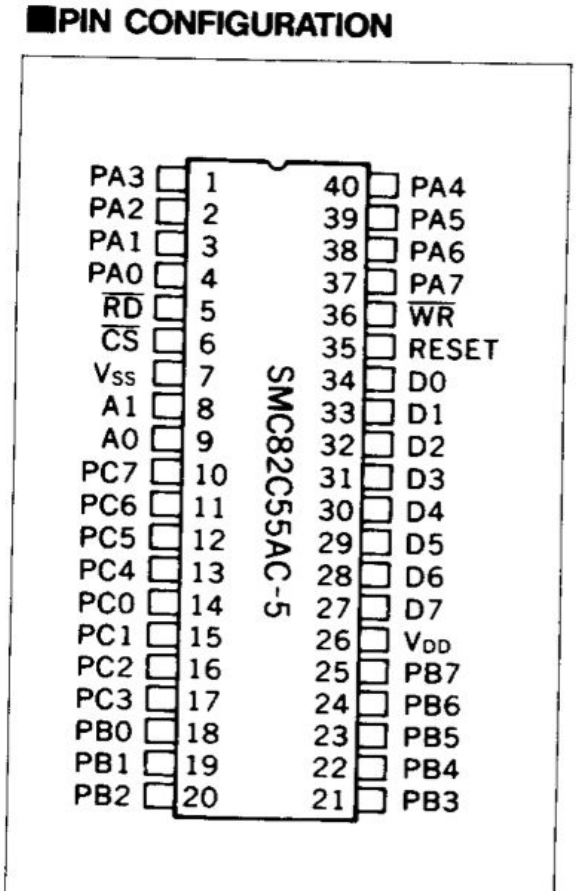


Fig. Pin configuration of 82C55AC

NEC D8253C

- It is a programmable interval timer.
- It contains three programmable, multimode 16 bit counter/ timer.
- It is designed as a general purpose device.
- D8253C interface directly to the buses of processor as an array of I/O port.
- It can generate accurate time delay under control of system software.
- Three independent 16 bit counter can be clocked at rates from DC to 5MHz.
- System software controls the loading and starting of counters to provide multiple accurate time delay.
- It is a binary counter or BCD.
- It requires single +5v supply $\pm$ 10%.

Pin description of D8253C

- **D7 - D0 (Data Bus) -** These pin form a three state bidirectional data bus that interfaces with 8080AF/ 8085 microprocessor system.
- **CLF 0,1,2 (Counter clock input 0 -2) -** clock 0, clock 1 and clock 2 input the clock signal for counter 0, counter 1 and counter 2 respectively.
- **OUT 0,1,2(Counter output 0 - 2) -** OUT 0, OUT 1, OUT 2 are output signal for counter 0, counter 1 and counter 2 respectively.
- **GATE 0,1,2 (counter gate input 0-2) -** Gate 0, 1, 2 are input gate counter 0, counter 1, counter 2 respectively.
- GND - ground
- **A0 - A1 -** Counter select.- these inputs are generally coneccted to the processor address bar and function is to select which of three counter is to be opened on

- CS(bar) - Chip select - A low level input will enable D8253C. Reading and writing will not occur until this is selected.
- Vcc - +5V
- RD(bar) - Read Counter - A low level input to this pin instructs the D8253C to send the selected counter value to the processor.
- WR(bar) - Write command or Data - A low level input to this pin instructs the D8253C to receive mode information or counter input data from the processor.

TMP 8085AP

- It is a 8 bit microprocessor unit.
- TMP8085AP uses a multiplexed data bus.
- Address is split between 8 bit address bus and 8 bit data bus.
- It requires +5v power supply.
- It has on chip clock generator.
- It has on chip system controller; cycle status information available for large system control.
- It is 4 vectored interrupts.
- It can perform Decimal, Binary and double precision arithmetic.
- It has serial in serial out port.
- It has direct addressing capability up to 64 Bytes of memory space.
- It is compatible with intel 8085A.
- It consumes low power.

Pin description of TMP8085AP

- **X1, X2 (Input)** - Crystal, LC ir RC network are also converted to X1 and X2 to drive internal clock generator.
- **CLK(output)** - clock output for use as a system clock.
- **RESETIN(bar) Input -** It initializes the processor by clearing the program counter instruction register, SOD latch, interrupt emable flip flop and HLDA flip flop.
- **RESET OUT (**OUTPUT) - RESET OUT signal indicates that the TMP8085A is being reset. It can be used as a system reset.
- **SOD**(output) - Serial output data line
- **SID(**input**) -** Serial input data line.
- **INTR (Input) -** INTERRUPT REQUEST signal provides a mechanism for external devices to modify the instruction flow of the program in progress.

- **INTR(bar) (**Output**) - INTERRUPT ACKNOWLEDGE -** Occurs in response to an interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus.
- **TRAP (**Input) - Trap interrupt is a nonmaskable RESTART interrupt. It is sampled at the same time as INTR or RST 5.5 - 7.5.
- **AD0 - AD7 (**Input/ output, 3 state) - Lower 8 bit of the memory address appear on the bus during the first clock cycle of a machine cycle.
- **AD0 - AD7 (**Input/ output 3-state) Lower 8 bits of the memory address appear on the bus during the first clock cycle of a machine cycle.
- **A8 - A15(**Output, 3 state**) -** Upper 8 bit of the memory address or the 8 bits of the I/O address, 3 stated during Hold and Halt modes and during RESET.
- **ALE (**Output) - Address latch enable.
- **WR(**bar) - Write control - Low on WR(bar) indicates the data on the data bus is to be written into the selected memory or I/O location.

- **RD(**bar) - Read control - A low level on RD(bar) indicates the selected memory or I/O device to be read and the data Bus is available for the data transfer.
- READY (input) - When READY is low, it indicates the external operation has not been complete yet the processor will enter the wait side.
- **HOLD (**input**) -** The hold cause TMP8085A to release control over the address bus and the data bus.
- **HLDA**(output) - The hold acknowledge output HLDA signal is a response to a HOLD input.
- Vcc = +5v supply
- Vss - ground reference

W27C512

- W27C512 is a high speed, low power electrically erasable and programmable Read only memory organized as 65536 x 8 bits.
- It operates on a single 5V power supply.
- It has High speed access time 45/70/90/120 nS(max)
- Read operating current is 30mA
- Erase programming operating current is 30 mA.
- Standby current 1mA
- +14V erase and +12V programing voltage required
- Its operation is fully static.
- All inputs and outputs directly TTL and CMOS compatible.
- It has three stage output.
- Available package are 28-pin 600 mil DIP and 300mil 32 pin PLCC.

Pin description of W27C512

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
Q0 - Q7	Data Input/output
CE(bar)	Chip enable
OE(bar)/ Vpp	Output enable program/erase supply voltage
Vcc	Power supply
GND	Ground
NC	No connection