IIITDM Kancheepuram

Semester – 4

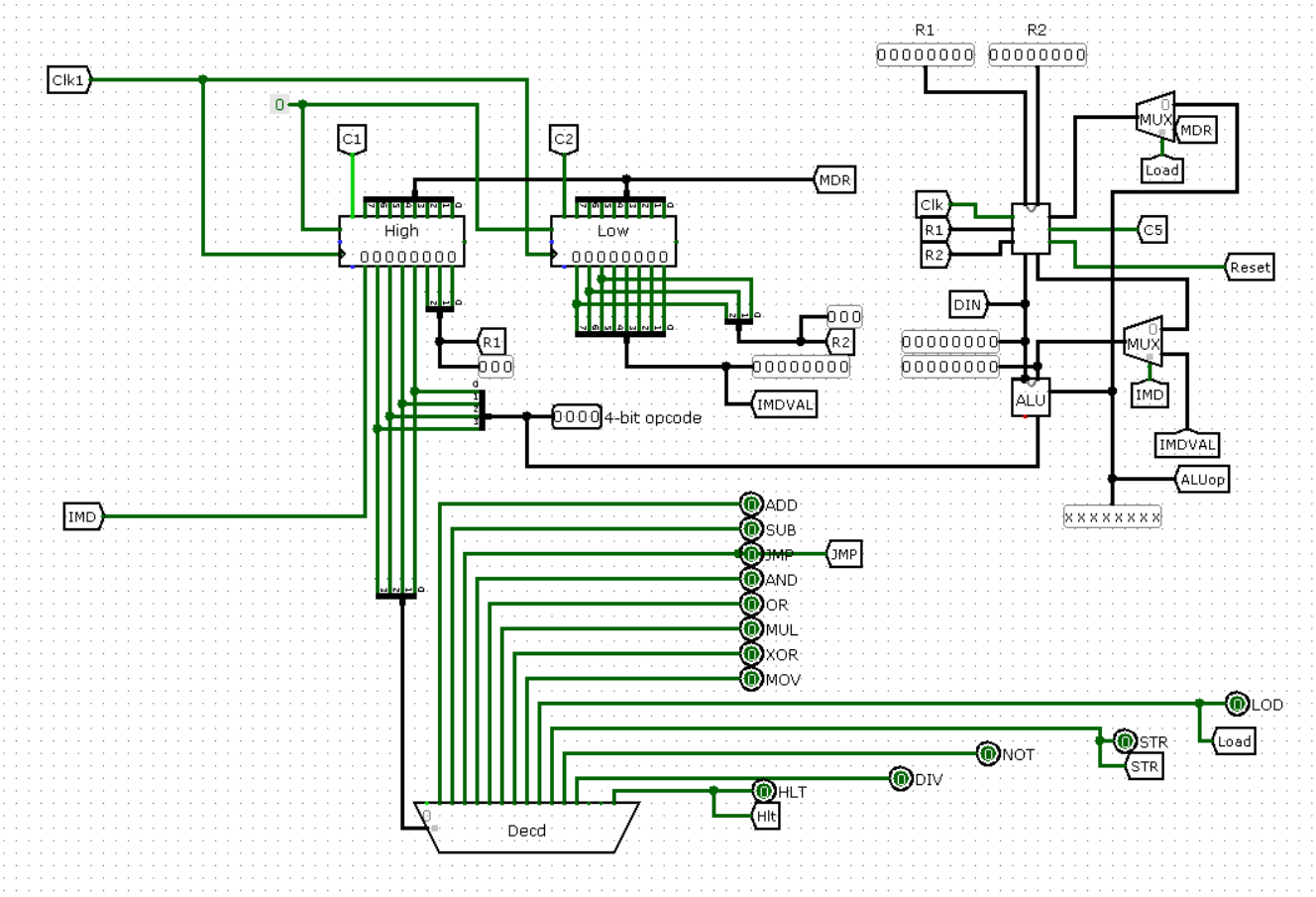
Computer Architecture and Organization

Project

8-bit CPU

Name Surya Raghav B
Roll No CS21B2042

Main Circuit Diagram (CU, ALU, ID)

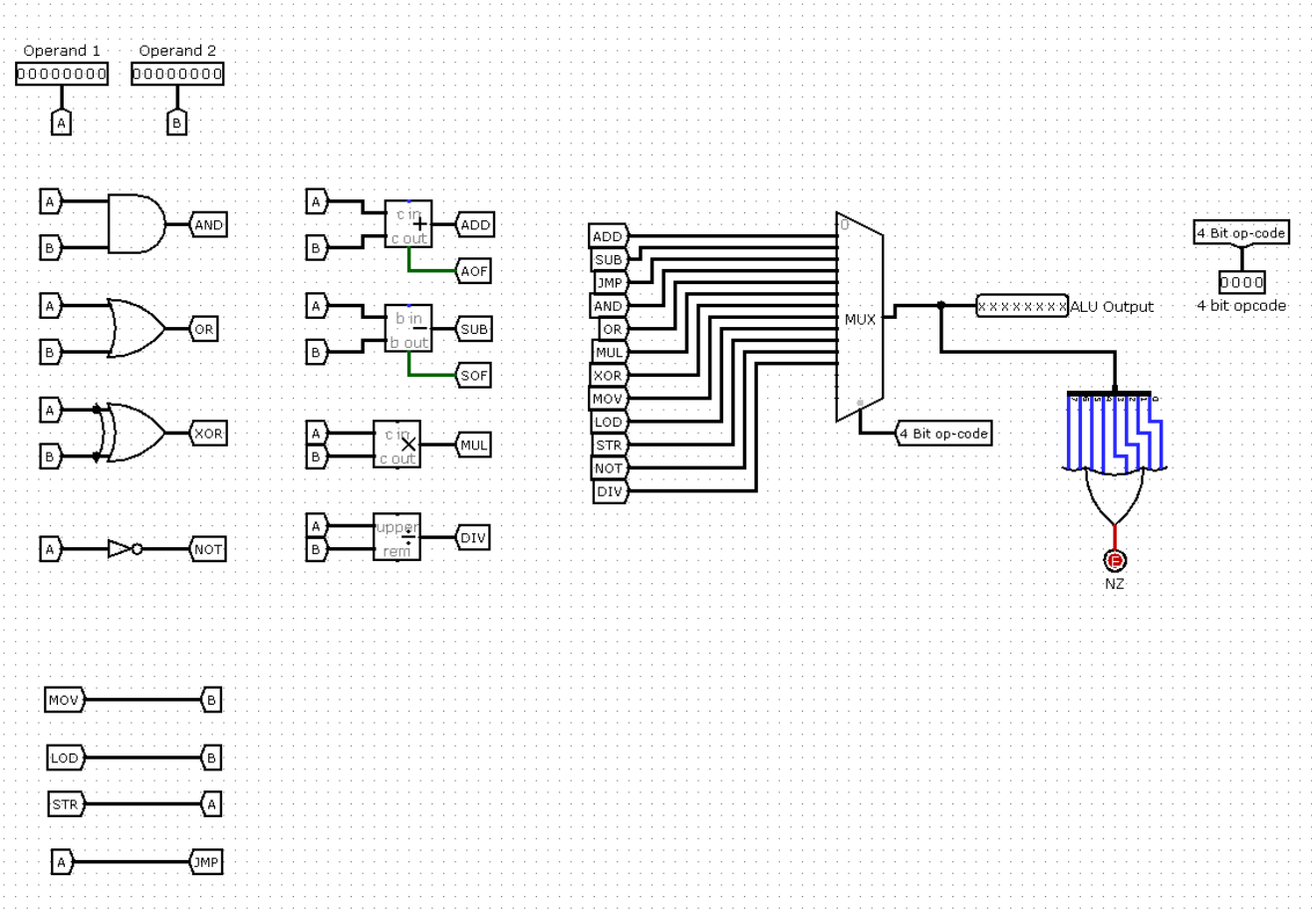


Instructions are 16-bit

- First bit denotes whether source-2 is immediate addressing or direct register addressing
- Next 4 bits denote the opcode for the ALU instruction
- Next 3 bits denote the Source-1 register selection
- Either next 3 bits denote Source-2 register selection or the next 8 bits denote the value of immediate addressing

#	####	###	########
Immediate	Op-code	Source-1	Source-2 (or) Immediate value

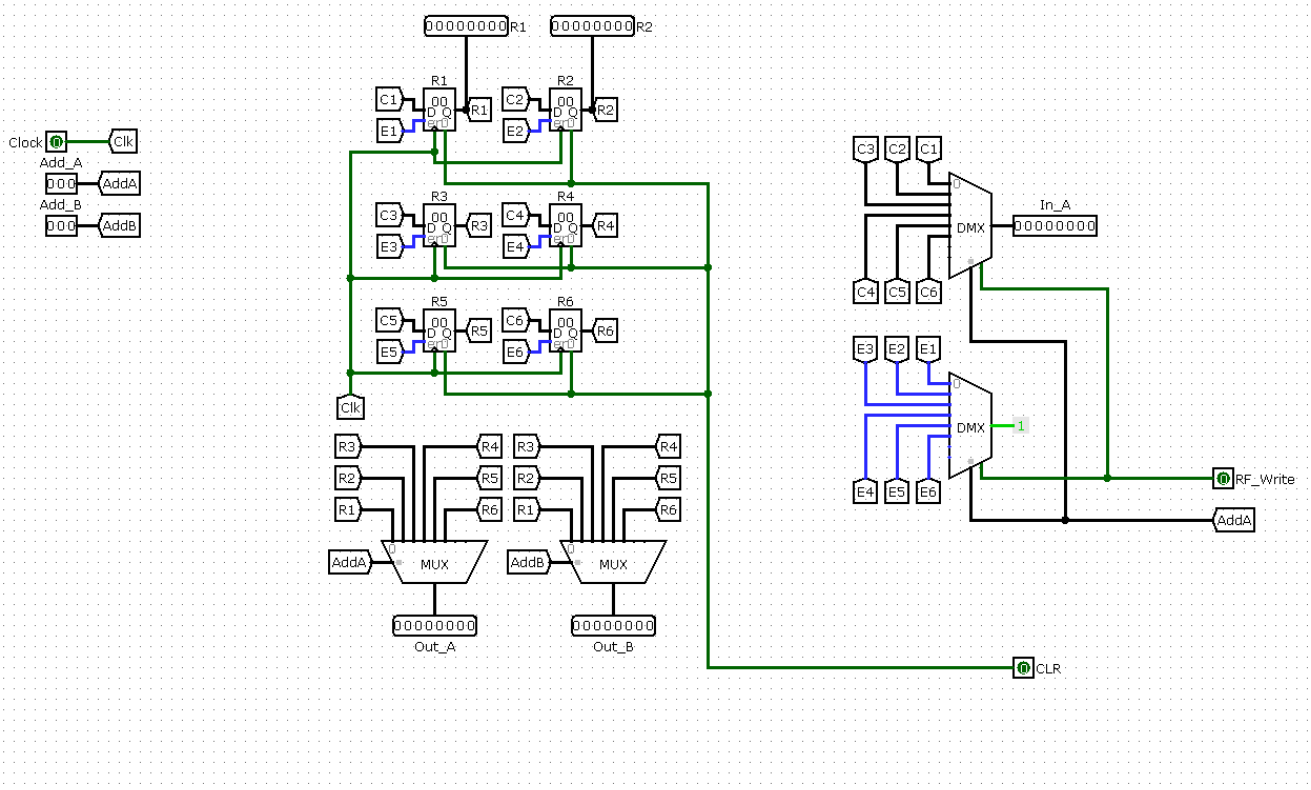
Arithmetic Logic Unit



Instruction Set

Opcode	Instruction
0001	ADD
0010	SUB
0011	JMP
0100	AND
0101	OR
0110	MUL
0111	XOR
1000	MOV
1001	LOD
1010	STR
1011	NOT
1100	DIV
1111	HLT

Register File



We have 6 registers R1, R2, R3, R4, R5, R6
We have 6 register enables E1, E2, E3, E4, E5, E6

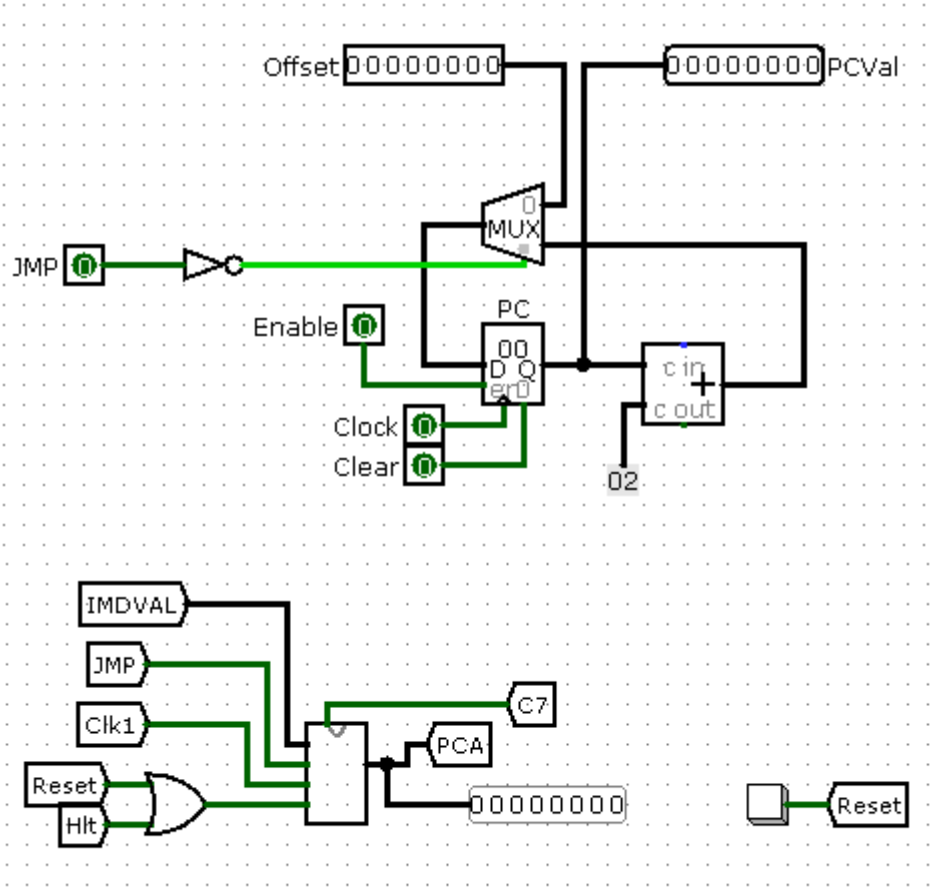
AddA – denotes which registers value must be sent as source-1
AddB – denotes which registers value must be sent as source-2

The two Mux's use AddA and AddB to select the registers

In_A can be either the ALU output or an instruction from MDR depending upon the load or write signals

First DMX selects which register should the data and send it via its corresponding bus
Second DMX enables the corresponding register based the Read_Write signal

Program Counter



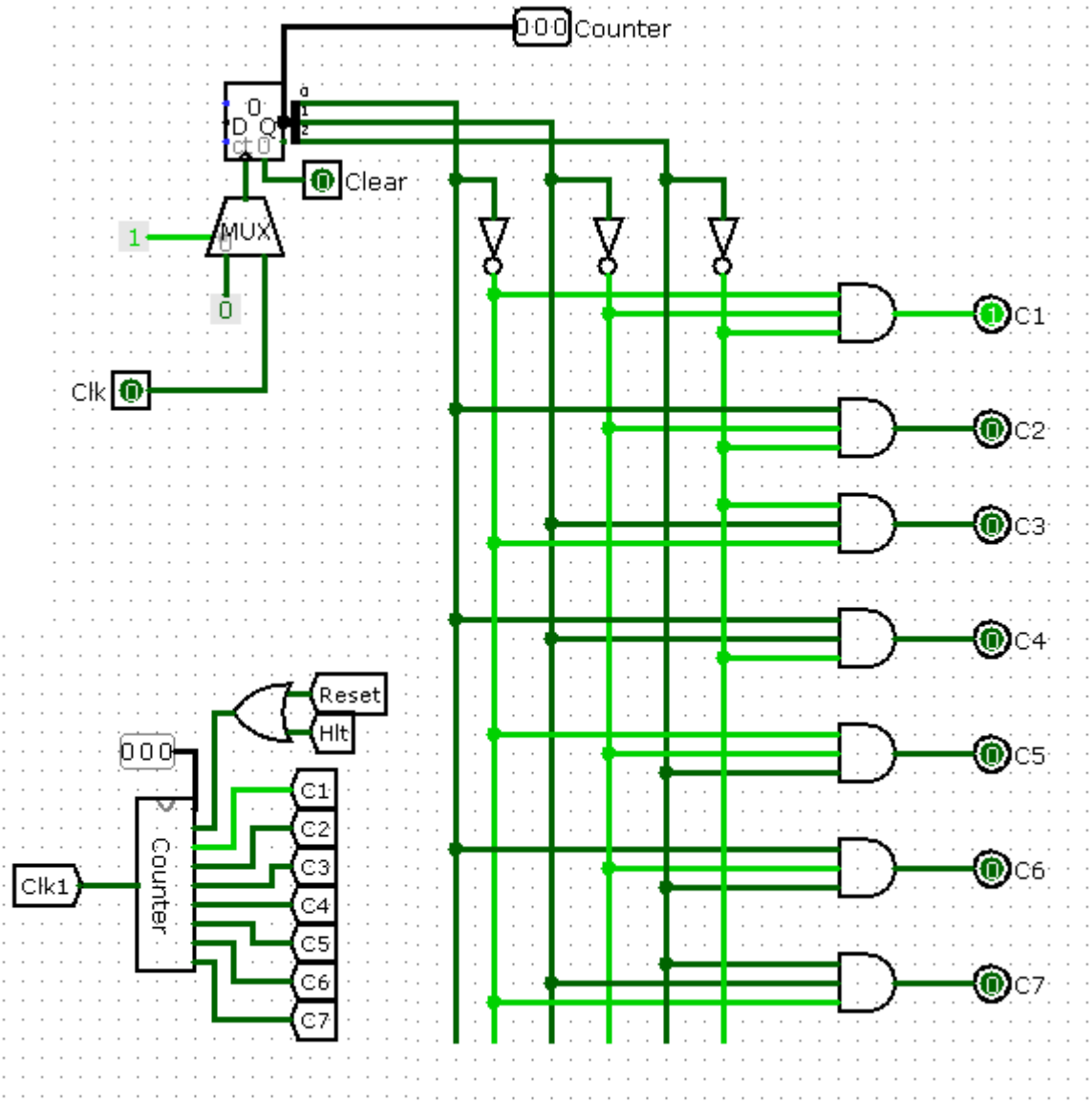
It stores the address of the next instruction to be executed.
It's incremented after every clock cycle.

When the JMP Instruction is enabled the jump offset is added to the program counter so that the control can shifted to different part of the program.

Control signal C7 denotes enable for PC which which goes high after every clock cycle.

An 8-bit full adder is used to add to either the current address or the current address with the offset.

Control Unit Signals



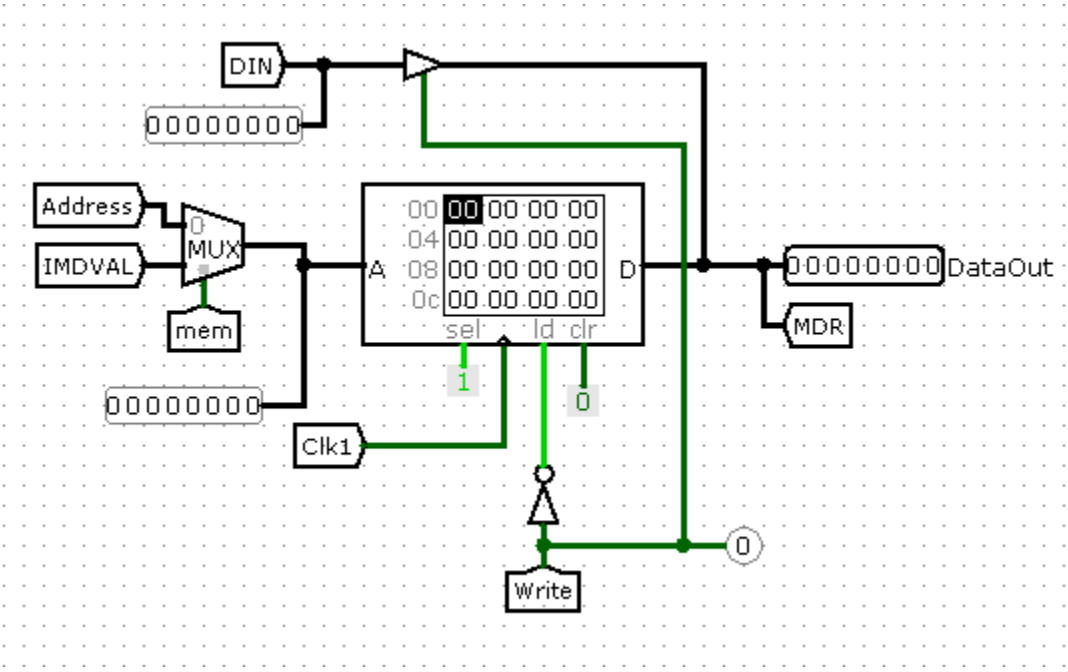
Each Control Unit signal server different purpose.

Generally C1 to C6 are used for data enable for the six registers.

C1 – used to select current 8-bit instruction is the higher part
C2 – used to select current 8-bit instruction is the lower part

C4 – used for Load access for read
C5 – used for Store access for write
C7 – used for Program counter enable

Main Memory



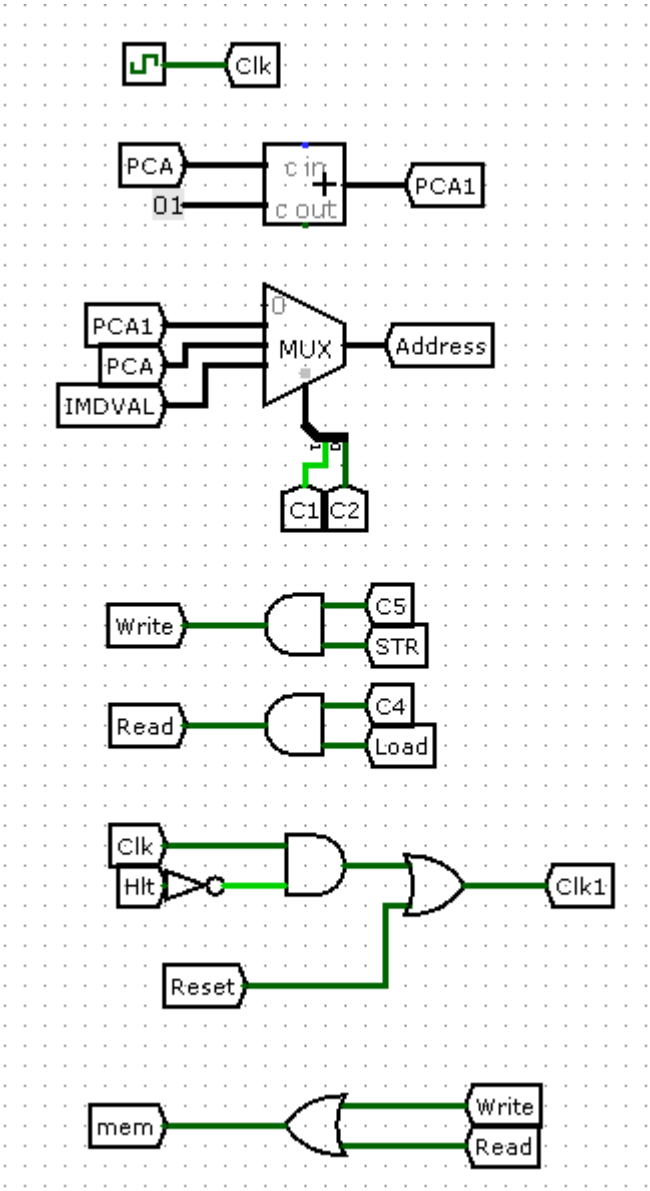
Depending the Read\Write signal the data is read or written to the main memory.

The mem selection selects whether retrieved data is an address or the immediate value for immediate data addressing

The Write writes the value from DIN into the corresspoding Address value

The fetched data or instruction is loaded into the the Memory Data Register(MDR) which is then sent to the register file.

Main Clock and Read\Write Flags



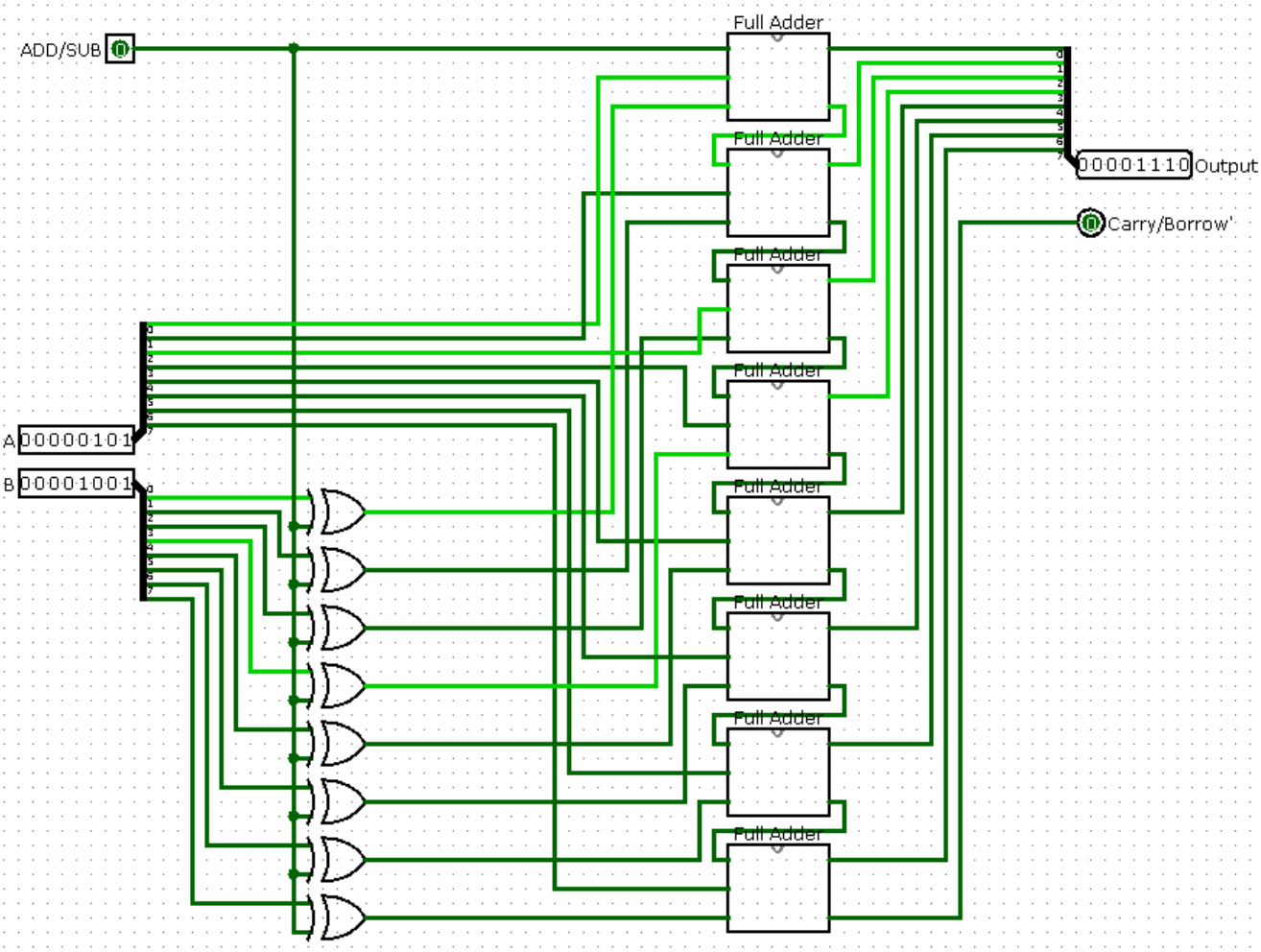
PCA is the current program counter address, PCA1 is 1 added to PCA

PCA – denotes the address when direct addressing is used
PCA1 – denotes the address when immediate addressing is used

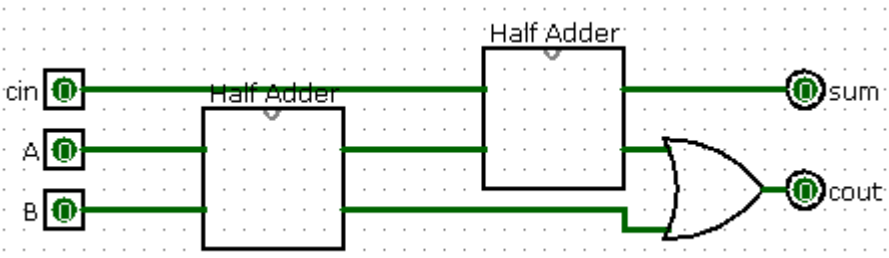
PCA or PCA1 or Immediate value is selected using the MUX with control signals C1 and C2

The mem is set to high if either a Read or Write is to be done in the memory

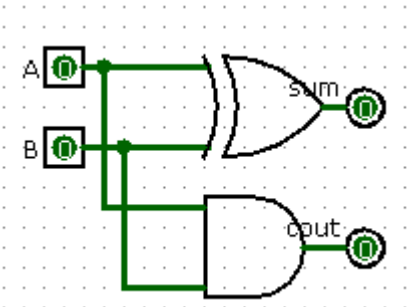
Adder/Subtractor in detail



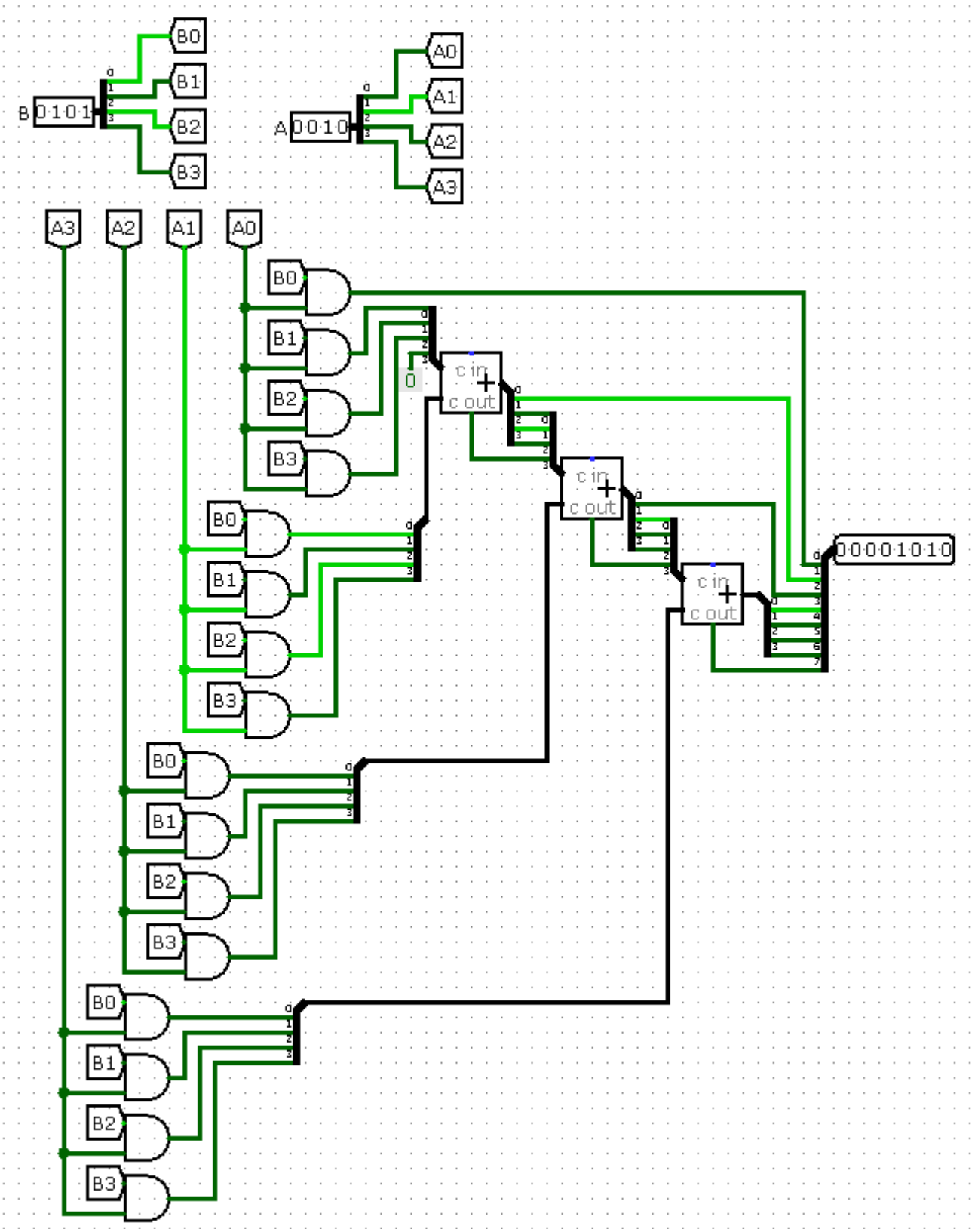
Full Adder



Half Adder



Multiplier in detail



Restoring Array divider in detail