Simulation performed for #gates = 3482 #faults = 5552 system mode = analysis pattern source = internal patterns							
simulated	coverage	in list d	etected	patterns	<pre># test patterns it = 300/100</pre>		RE/AU/AAB
						0.82 sec	20/0/2
64	85.26%	908	4624	61	61	0.87 sec	
						1.44 sec	81/4/56
128	95.35%	280	563	51	112	1.44 sec	
						1.79 sec	117/10/76
192	98.53%	79	159	49	161	1.79 sec	
						1.79 sec	117/10/76
242	99.65%	11	68	38	199	1.79 sec	
Performing redundant fault identification for 11 faults deterministic ATPG invoked with abort limit = 300							
	# non-red.				ess test	process	
	faults				coverac		
2	0	9		0 100.0			

Statistics Report Stuck-at Faults						
Fault Classes	#faults (total)					
FU (full)	6218					
UO (unobserved) DS (det_simulation) DI (det_implication) UU (unused) RE (redundant) AU (atpg_untestable)	9 (0.14%) 5414 (87.07%) 630 (10.13%) 36 (0.58%) 119 (1.91%) 10 (0.16%)					
Fault Sub-classes						
UC+U0 AAB (atpg_abort) Coverage	9 (0.14%)					
test_coverage fault_coverage atpg_effectiveness	99.69% 97.20% 99.86%					
<pre>#test_patterns #simulated_patterns CPU_time (secs)</pre>	199 242 3.6					

	s test d coverage istic ATPG in		etected		<pre># test patterns nit = 300/100</pre>	process CPU time	RE/AU/AAB
						0.75 sec	11/0/21
64	86.91%	787	4686	60	60	0.80 sec	
						1.21 sec	66/0/79
128	96.14%	230	502	56	116	1.21 sec	, -,
						1.37 sec	100/0/93
192	98.97%	61	135	55	171	1.37 sec	
						1.37 sec	100/0/93
226	99.85%	9	52	30	201	1.37 sec	
Performing redundant fault identification for 9 faults deterministic ATPG invoked with abort limit = 300							
# red.	# non-red.	# abort	# rem	n. progi	ess test	process	
faults	faults	faults	faul	ts	coverage	CPU time	
Θ	2	7		0 100.0	99.85%)	0.05 sec	

Fault Classes	#faults (total)
FU (full)	6024
UO (unobserved) DS (det_simulation) DI (det_implication) RE (redundant)	9 (0.15%) 5375 (89.23%) 540 (8.96%) 100 (1.66%)
Fault Sub-classes	
UC+UO AAB (atpg_abort)	9 (0.15%)
Coverage	
test_coverage fault_coverage atpg_effectiveness	99.85% 98.19% 99.85%
#test_patterns #simulated_patterns CPU_time (secs)	201 226 2.6

Flow	#Faults	Test Coverage	#Patterns	Run time
DC+TMAX	4419	99.29%	151	0.28s
TS	6218	99.69%	199	3.6s
DC+TS	6024	99.85%	201	2.6s