Pre_norm scan

Area

```
Number of ports:                          285
Number of nets:                           972
Number of cells:                          759
Number of combinational cells:            682
Number of sequential cells:                71
Number of macros/black boxes:               0
Number of buf/inv:                        183
Number of references:                      45

Combinational area:               2906.338053
Buf/Inv area:                      418.437016
Noncombinational area:            1302.566048
Macro/Black Box area:                0.000000
Net Interconnect area:          101313.842743

Total cell area:                  4208.904101
Total area:                     105522.746844
```

Clock slack

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
pre_norm           wl10                  l90sprvt_typ

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
signb_r_reg/CK (LSDFQM2N)                0.00       0.00 r
signb_r_reg/Q (LSDFQM2N)                 0.18       0.18 r
U806/Z (XOR2M1N)                         0.13       0.31 f
U805/Z (OAI211B100M0N)                   0.16       0.47 f
U803/Z (OAI21M0N)                        0.19       0.65 r
result_zero_sign_reg/D (LSDFQM2N)        0.00       0.65 r
data arrival time                                   0.65

clock clk (rise edge)                   10.00      10.00
clock network delay (ideal)              0.00      10.00
result_zero_sign_reg/CK (LSDFQM2N)       0.00      10.00 r
library setup time                      -0.24       9.76
data required time                                  9.76
-----------------------------------------------------------
data required time                                  9.76
data arrival time                                  -0.65
-----------------------------------------------------------
slack (MET)                                         9.11
```

Power

```
Design          Wire Load Model            Library
------------------------------------------------
pre_norm                wl10               l90sprvt_typ


Global Operating Voltage = 1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =  98.1690 uW   (37%)
  Net Switching Power  = 167.1530 uW   (63%)
                         ---------
Total Dynamic Power    = 265.3220 uW  (100%)

Cell Leakage Power     =   5.7013 uW
```

```
Patn 10: #merges=0    #failed_merges=1    #faults=1  #det=1  CPU=0.28 sec
Patn 11: #merges=0    #failed_merges=1    #faults=1  #det=2  CPU=0.28 sec
Patn 12: #merges=0    #failed_merges=1    #faults=1  #det=2  CPU=0.28 sec
Patn 13: #merges=0    #failed_merges=1    #faults=1  #det=2  CPU=0.28 sec
Patn 14: #merges=0    #failed_merges=1    #faults=1  #det=2  CPU=0.28 sec
Patn 15: #merges=1    #failed_merges=1    #faults=2  #det=2  CPU=0.28 sec
Patn 16: #merges=0    #failed_merges=1    #faults=1  #det=2  CPU=0.28 sec
Patn 17: #merges=1    #failed_merges=1    #faults=2  #det=3  CPU=0.28 sec
Patn 18: #merges=0    #failed_merges=4    #faults=1  #det=1  CPU=0.28 sec
Patn 19: #merges=1    #failed_merges=0    #faults=2  #det=2  CPU=0.28 sec
Patn 20: #merges=1    #failed_merges=1    #faults=2  #det=2  CPU=0.28 sec
Patn 21: #merges=0    #failed_merges=1    #faults=1  #det=1  CPU=0.28 sec
Patn 22: #merges=0    #failed_merges=1    #faults=1  #det=1  CPU=0.28 sec
Patn 23: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.28 sec
Patn 24: #merges=0    #failed_merges=1    #faults=1  #det=1  CPU=0.28 sec
Patn 25: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.28 sec
Fault simulation: 2 patterns were dropped due to no added detection.
151           44     50       52/1/59    99.14%      0.28
```

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	5888
Possibly detected	PT	0
Undetectable	UD	85
ATPG untestable	AU	1
Not detected	ND	50
total faults		6024
test coverage		99.14%

Pattern Summary Report

#internal patterns	151
#basic_scan patterns	151

Collapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	4336
detected_by_simulation	DS	(3836)
detected_by_implication	DI	(500)
Possibly detected	PT	0
Undetectable	UD	52
undetectable-redundant	UR	(52)
ATPG untestable	AU	1
atpg_untestable-not_detected	AN	(1)
Not detected	ND	30
not-controlled	NC	(2)
not-observed	NO	(28)
total faults		4419
test coverage		99.29%

Pattern Summary Report

#internal patterns	151
#basic_scan patterns	151

Pre_norm unscan

Area

```
Number of ports:                          274
Number of nets:                           961
Number of cells:                          759
Number of combinational cells:            682
Number of sequential cells:                71
Number of macros/black boxes:               0
Number of buf/inv:                        183
Number of references:                      45

Combinational area:               2906.338053
Buf/Inv area:                      418.437016
Noncombinational area:             901.771015
Macro/Black Box area:                0.000000
Net Interconnect area:           94687.141235

Total cell area:                  3808.109068
Total area:                      98495.250304
```

Clock slack

```
clock clk (rise edge)                    10.00      10.00
clock network delay (ideal)               0.00      10.00
result_zero_sign_reg/CK (LDFQM2N)         0.00      10.00 r
library setup time                       -0.18       9.82
data required time                                   9.82
-----------------------------------------------------------
data required time                                   9.82
data arrival time                                   -0.62
-----------------------------------------------------------
slack (MET)                                          9.20
```

Power

```
Design        Wire Load Model            Library
------------------------------------------------
pre_norm              wl10               l90sprvt_typ


Global Operating Voltage = 1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =  91.8773 uW   (36%)
  Net Switching Power  = 162.1575 uW   (64%)
                         ---------
Total Dynamic Power    = 254.0348 uW  (100%)

Cell Leakage Power     =   5.4875 uW
```

```
-------------------------------------------------------------
#patterns  #faults        #ATPG faults  test       process
stored     detect/active  red/au/abort  coverage   CPU time
---------  ------------   ------------  --------   ----------
255              4     26       4/210/3     96.51%      1947.75  ( 32:27.75 )
256              2     24       4/210/3     96.55%      1947.75  ( 32:27.75 )
257              1     23       4/210/3     96.56%      1947.75  ( 32:27.75 )
258              2     21       4/210/3     96.60%      1947.76  ( 32:27.76 )
259              3     18       4/210/3     96.65%      1947.76  ( 32:27.76 )
260              1     17       4/210/3     96.67%      1947.76  ( 32:27.76 )
261              1     16       4/210/3     96.69%      1947.77  ( 32:27.77 )
262              1     14       4/211/3     96.70%      1947.77  ( 32:27.77 )
263              1     13       4/211/3     96.72%      1947.77  ( 32:27.77 )
264              1     12       4/211/3     96.74%      1947.78  ( 32:27.78 )
265              1     11       4/211/3     96.76%      1947.78  ( 32:27.78 )
266              1     10       4/211/3     96.77%      1947.78  ( 32:27.78 )
266              0      4       4/214/3     96.77%      1947.84  ( 32:27.84 )
136 faults were identified as detected by implication, test coverage is now 97.97%.
```

```
TEST-T> report_summaries
      Collapsed Stuck Fault Summary Report
 -----------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT       3928
   detected_by_simulation         DS      (3792)
   detected_by_implication        DI       (136)
 Possibly detected                PT          8
   atpg_untestable-pos_detected   AP        (6)
   not_analyzed-pos_detected      NP        (2)
 Undetectable                     UD         12
   undetectable-redundant         UR       (12)
 ATPG untestable                  AU         70
   atpg_untestable-not_detected   AN       (70)
 Not detected                     ND          1
   not-observed                   NO        (1)
 -----------------------------------------------
 total faults                              4019
 test coverage                            98.13%
 -----------------------------------------------
            Pattern Summary Report
 -----------------------------------------------
 #internal patterns                         266
     #full_sequential patterns              266
 -----------------------------------------------
```

s38584_seq scan

Area

```
Number of ports:                        10446
Number of nets:                         20449
Number of cells:                        10308
Number of combinational cells:           7400
Number of sequential cells:              1452
Number of macros/black boxes:               0
Number of buf/inv:                       3241
Number of references:                    1544

Combinational area:              26074.905613
Buf/Inv area:                     6952.885330
Noncombinational area:           26642.624973
Macro/Black Box area:                0.000000
Net Interconnect area:         1170079.573273

Total cell area:                 52717.530586
Total area:                    1222797.103859
```

Clock slack

```
U6044/Z (INVM2N)                        0.09       3.73 f
U6325/Z (NR2M2N)                        0.16       3.89 r
U6045/Z (INVM2N)                        0.09       3.99 f
U6330/Z (NR2M2N)                        0.16       4.14 r
U6046/Z (INVM2N)                        0.09       4.24 f
U6331/Z (NR2M2N)                        0.16       4.40 r
U6048/Z (INVM2N)                        0.09       4.49 f
U6332/Z (NR2M2N)                        0.16       4.65 r
U6049/Z (INVM2N)                        0.09       4.74 f
U6333/Z (NR2M2N)                        0.16       4.90 r
U6050/Z (INVM2N)                        0.09       5.00 f
U6326/Z (NR2M2N)                        0.16       5.16 r
U6051/Z (INVM2N)                        0.09       5.25 f
U7269/Z (AOI32M2N)                      0.10       5.35 r
U7268/Z (OAI21M0N)                      0.12       5.46 f
DFF_990/D (dff_test_982)                0.00       5.46 f
DFF_990/Q_reg/D (SDFZRM0N)              0.00       5.46 f
data arrival time                                  5.46

clock CK (rise edge)                   10.00      10.00
clock network delay (ideal)             0.00      10.00
DFF_990/Q_reg/CK (SDFZRM0N)             0.00      10.00 r
library setup time                     -0.24       9.76
data required time                                 9.76
-----------------------------------------------------------
data required time                                 9.76
data arrival time                                 -5.46
-----------------------------------------------------------
slack (MET)                                        4.30
```

Power

```
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   2.2681 mW   (38%)
  Net Switching Power  =   3.6764 mW   (62%)
                         ---------
Total Dynamic Power    =   5.9445 mW  (100%)

Cell Leakage Power     =  64.9848 uW
```

```
-----------------------------------------------------------
#patterns     #faults     #ATPG faults  test      process
stored     detect/active  red/au/abort  coverage  CPU time
---------  -------------  ------------  --------  --------
Begin deterministic ATPG: #uncollapsed_faults=60687, abort_limit=250...
Patn  1: #merges=2050  #failed_merges=14   #faults=2051  #det=3714  CPU=0.02 sec
Patn  2: #merges=5579  #failed_merges=323  #faults=5580  #det=10838  CPU=0.05 sec
Patn  3: #merges=4027  #failed_merges=217  #faults=4028  #det=7279  CPU=0.08 sec
Patn  4: #merges=3000  #failed_merges=175  #faults=3001  #det=5330  CPU=0.10 sec
Patn  5: #merges=2301  #failed_merges=76   #faults=2302  #det=3698  CPU=0.11 sec
Patn  6: #merges=1611  #failed_merges=144  #faults=1612  #det=2612  CPU=0.13 sec
Patn  7: #merges=616  #failed_merges=5    #faults=617  #det=1715  CPU=0.13 sec
Patn  8: #merges=1767  #failed_merges=138  #faults=1768  #det=3051  CPU=0.15 sec
Patn  9: #merges=1518  #failed_merges=146  #faults=1519  #det=2535  CPU=0.16 sec
Patn 10: #merges=928  #failed_merges=106  #faults=929  #det=1409  CPU=0.17 sec
Patn 11: #merges=1060  #failed_merges=218  #faults=1061  #det=1796  CPU=0.18 sec
Patn 12: #merges=940  #failed_merges=165  #faults=941  #det=1570  CPU=0.19 sec
Patn 13: #merges=784  #failed_merges=155  #faults=785  #det=1363  CPU=0.20 sec
Patn 14: #merges=218  #failed_merges=3    #faults=219  #det=235  CPU=0.21 sec
Patn 15: #merges=597  #failed_merges=173  #faults=598  #det=1017  CPU=0.21 sec
Patn 16: #merges=511  #failed_merges=160  #faults=512  #det=876  CPU=0.22 sec
Patn 17: #merges=473  #failed_merges=65   #faults=474  #det=731  CPU=0.23 sec
```

```
Patn  0: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  1: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  2: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  3: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  4: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  5: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  6: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
Patn  7: #merges=0    #failed_merges=0    #faults=1  #det=1  CPU=0.42 sec
136             8      0          0/0/0   100.00%      0.42
```

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      70726
Possibly detected                PT          0
Undetectable                     UD         42
ATPG untestable                  AU          0
Not detected                     ND          0
-----------------------------------------------
total faults                                70768
test coverage                              100.00%
-----------------------------------------------
           Pattern Summary Report
-----------------------------------------------
#internal patterns                            136
    #basic_scan patterns                      136
-----------------------------------------------
```

```
      Collapsed Stuck Fault Summary Report
 -----------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT      42144
   detected_by_simulation         DS     (34999)
   detected_by_implication        DI      (7145)
 Possibly detected                PT          0
 Undetectable                     UD         36
   undetectable-unused            UU          (4)
   undetectable-tied              UT         (30)
   undetectable-blocked           UB          (2)
 ATPG untestable                  AU          0
 Not detected                     ND          0
 -----------------------------------------------
 total faults                                42180
 test coverage                              100.00%
 -----------------------------------------------
            Pattern Summary Report
 -----------------------------------------------
 #internal patterns                            136
     #basic_scan patterns                      136
 -----------------------------------------------
```

s38584_seq unscan

Area

```
Number of ports:                         6102
Number of nets:                         14671
Number of cells:                        10310
Number of combinational cells:           7402
Number of sequential cells:              1452
Number of macros/black boxes:               0
Number of buf/inv:                       1795
Number of references:                    1571

Combinational area:                28125.794631
Buf/Inv area:                       3893.820181
Noncombinational area:             18441.852310
Macro/Black Box area:                 0.000000
Net Interconnect area:          1034605.431976

Total cell area:                   46567.646941
Total area:                     1081173.078918
```

Clock slack

```
clock CK (rise edge)                    10.00      10.00
clock network delay (ideal)              0.00      10.00
DFF_990/Q_reg/CK (LDFQM0N)               0.00      10.00 r
library setup time                      -0.08       9.92
data required time                                  9.92
-----------------------------------------------------------
data required time                                  9.92
data arrival time                                  -5.56
-----------------------------------------------------------
slack (MET)                                         4.36
```

Power

```
Design        Wire Load Model            Library
------------------------------------------------
s38584_seq            wl10               l90sprvt_typ


Global Operating Voltage = 1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.1806 mW   (63%)
  Net Switching Power  = 683.3595 uW   (37%)
                         ---------
Total Dynamic Power    =   1.8640 mW  (100%)

Cell Leakage Power     =  55.4623 uW
```

```
-------------------------------------------------------
#patterns  #faults       #ATPG faults  test       process
stored     detect/active  red/au/abort  coverage   CPU time
---------  ------------  ------------  --------  ----------
13              0  44030       0/26/30     22.10%     29179.40  ( 8:06:19.40 )
14            390  43639       0/27/30     22.84%     29936.50  ( 8:18:56.50 )
15            274  43365       0/27/30     23.34%     29937.47  ( 8:18:57.47 )
15              0  43365       0/27/31     23.34%     31137.51  ( 8:38:57.51 )
16            412  42953       0/27/31     24.14%     31139.62  ( 8:38:59.62 )
16              0  42953       0/27/32     24.14%     32339.85  ( 8:58:59.85 )
16              0  42952       0/28/33     24.14%     33268.98  ( 9:14:28.98 )
17           2143  40809       0/28/33     28.03%     33272.15  ( 9:14:32.15 )
17              0  40809       0/28/34     28.03%     34472.46  ( 9:34:32.46 )
17              0  40808       0/29/35     28.03%     35674.74  ( 9:54:34.74 )
17              0  40808       0/29/36     28.03%     36874.78  ( 10:14:34.78 )

MAX total CPU time reached : timeUsed = 10:14:34.78, MAX = 10:00:00.00 ... Sequential Test Generation terminated
910 faults were identified as detected by implication, test coverage is now 28.85%.
```

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      15683
Possibly detected                PT        723
Undetectable                     UD         39
ATPG untestable                  AU         27
Not detected                     ND      39184
-----------------------------------------------
total faults                            55656
test coverage                           28.85%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                         17
    #basic_scan patterns                    4
    #full_sequential patterns              13
-----------------------------------------------
```

```
      Collapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT       9352
  detected_by_simulation         DS      (8442)
  detected_by_implication        DI       (910)
Possibly detected                PT        723
  atpg_untestable-pos_detected   AP          (4)
  not_analyzed-pos_detected      NP       (719)
Undetectable                     UD         36
  undetectable-unused            UU          (6)
  undetectable-tied              UT         (29)
  undetectable-blocked           UB          (1)
ATPG untestable                  AU         20
  atpg_untestable-not_detected   AN         (20)
Not detected                     ND      23820
  not-controlled                 NC      (4108)
  not-observed                   NO     (19712)
-----------------------------------------------
total faults                            33951
test coverage                           28.64%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                         17
    #basic_scan patterns                    4
    #full_sequential patterns              13
-----------------------------------------------
```

Pre_norm	Area	Power	Fault count	Coverage(collapsed)	ATPG Run times	Pattern number
Scanned	105522.746844	265.3220uW	4419	99.29%	0.28s	151
Non Scanned	98495.250304	254.0348uW	4019	98.13%	1947.84s	266

s38584_seq	Area	Power	Fault count	Coverage(collapsed)	ATPG Run times	Pattern number
Scanned	1222797.103859	5.9445mW	42180	100%	0.42s	136
Non Scanned	1081173.078918	1.8640mW	33951	28.64%	36874.78s	17