# Digital IC Design

## Lec 2: Device and DC Characteristics

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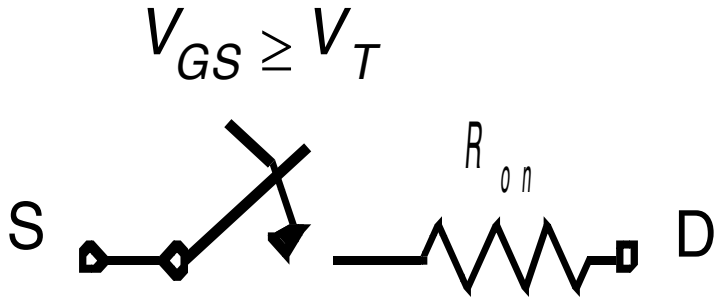
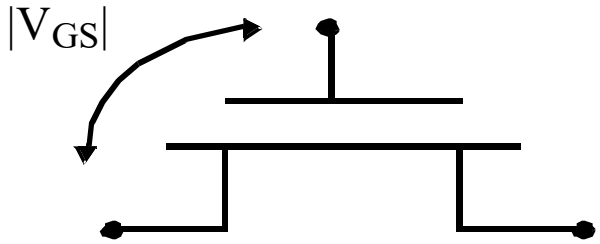
# What is Transistor?

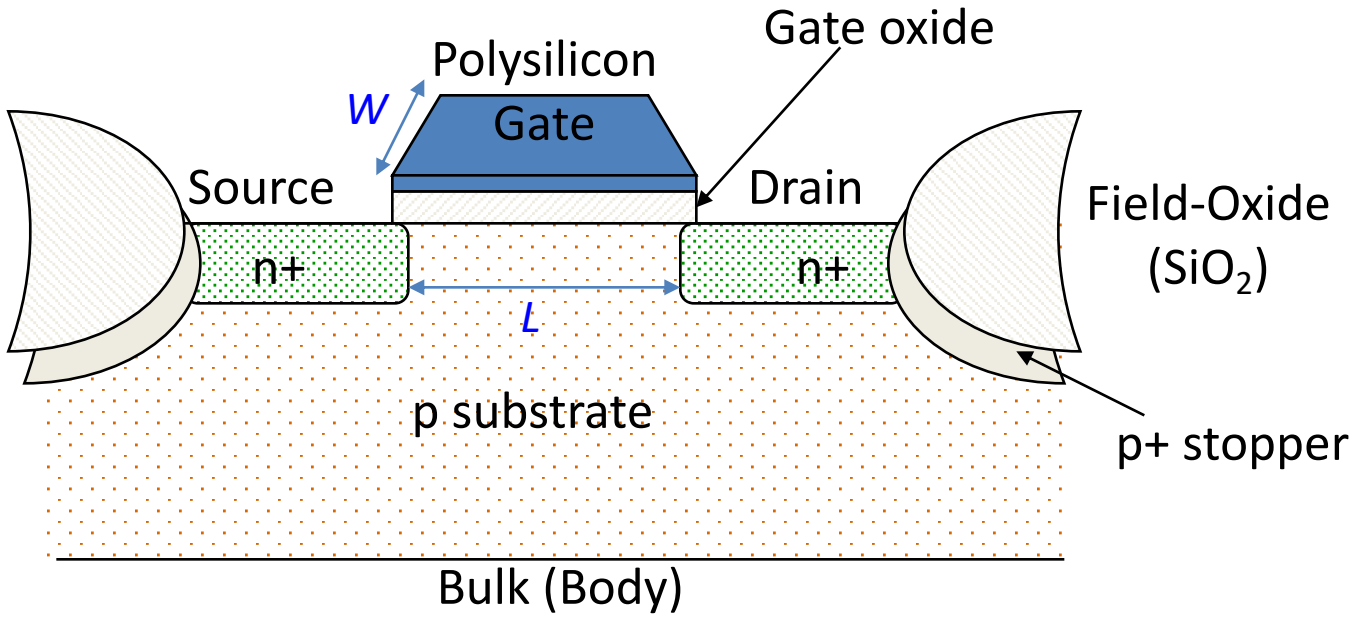
A Switch! ⟷ An MOS Transistor



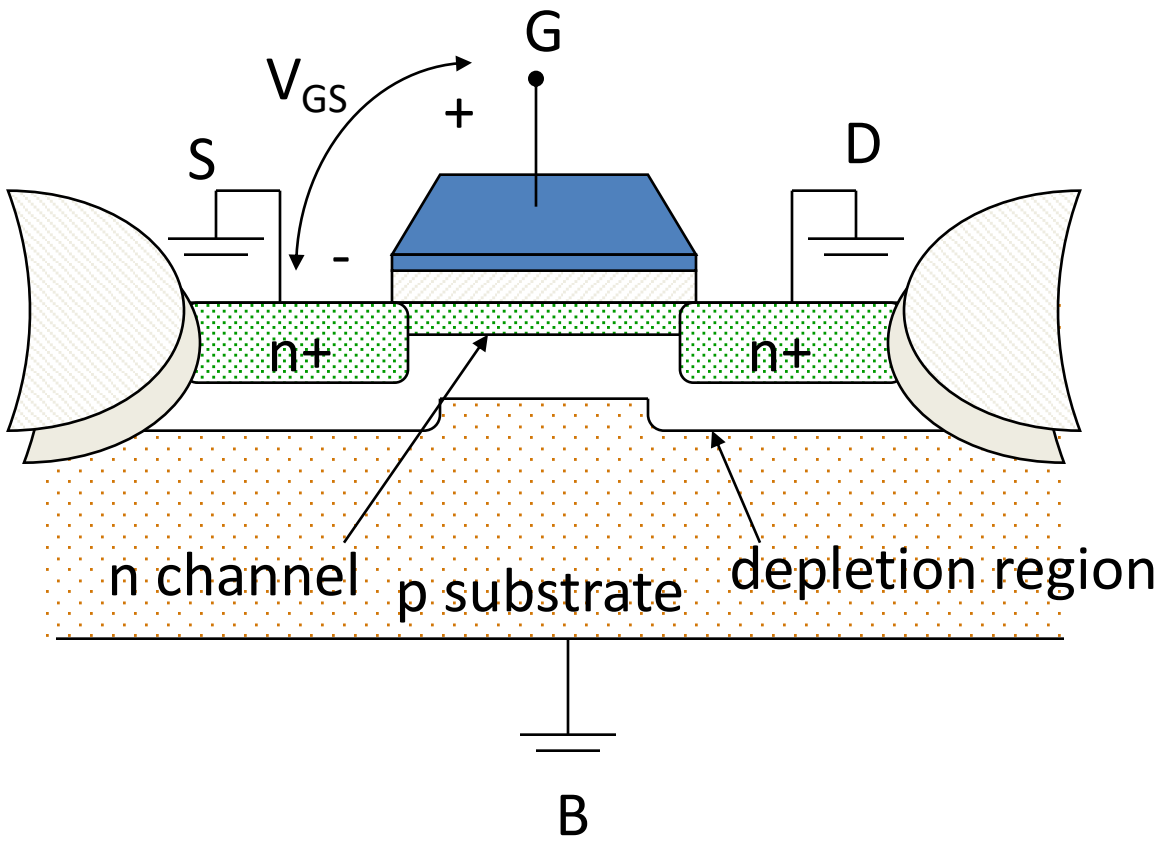
# The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration $N_D$ - electrons are the majority carriers



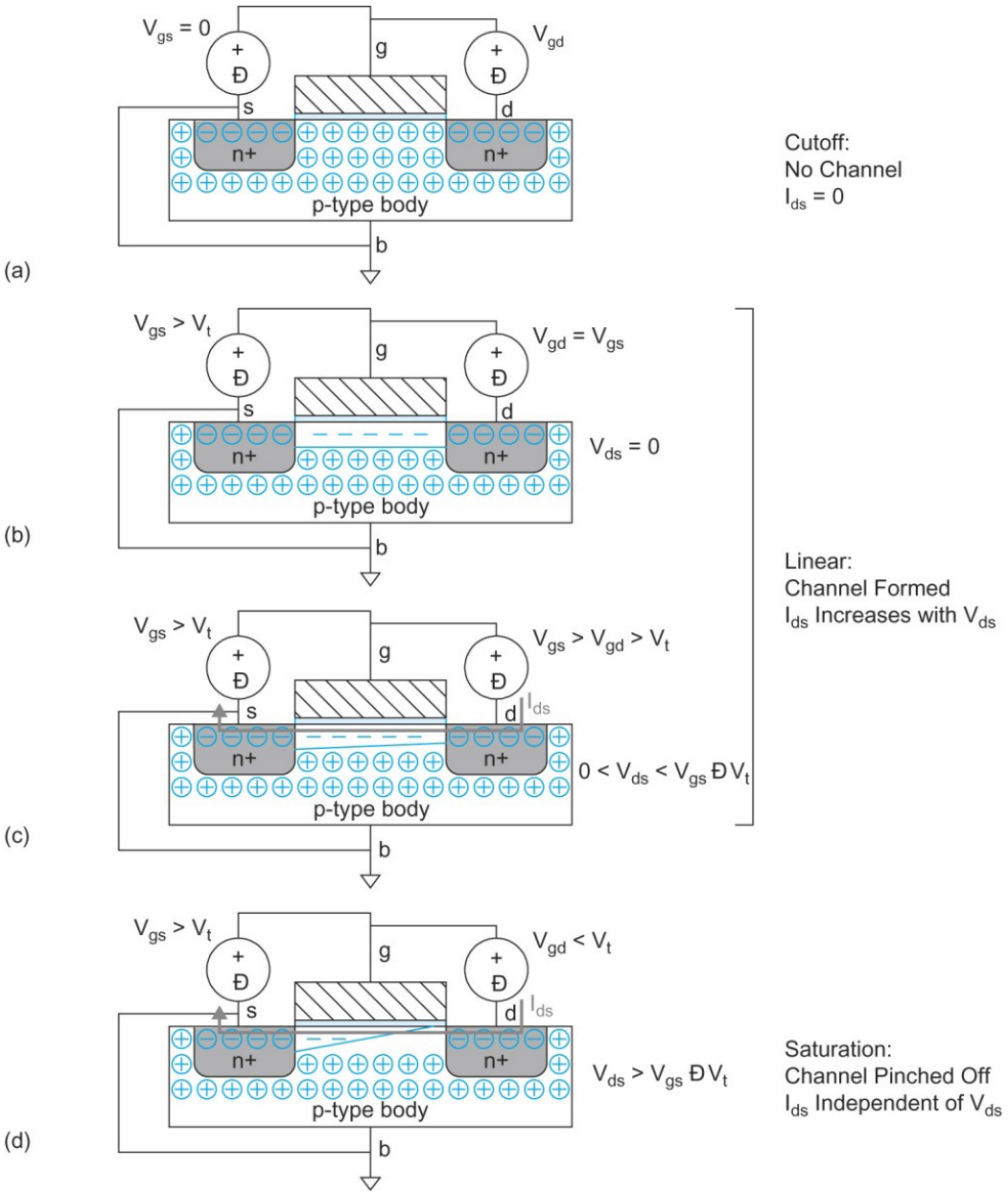

p areas have been doped with acceptor ions (boron) of concentration $N_A$ - holes are the majority carriers

# Threshold Voltage Concept




The value of $V_{GS}$ where strong inversion occurs is called the threshold voltage, $V_T$

# Operation of NMOS



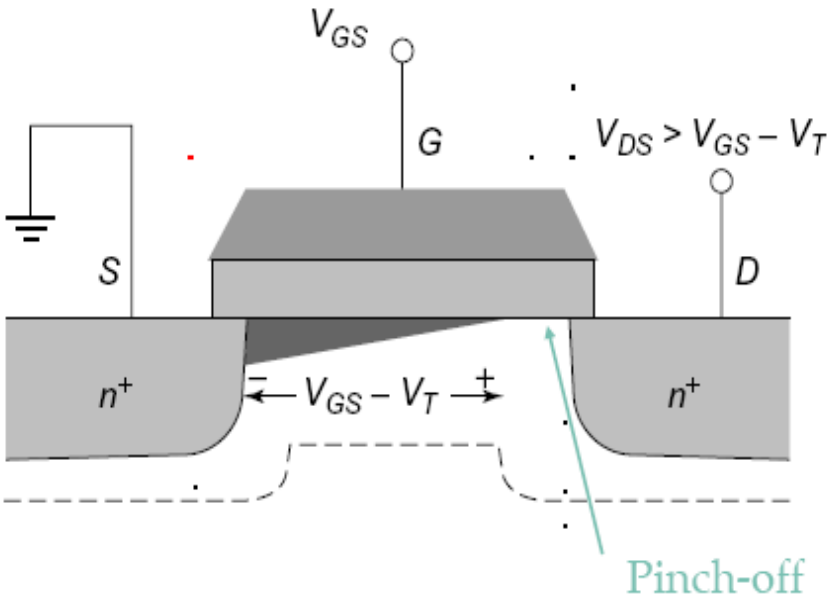
# MOS Current

- $I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_c(x))\,\mu E$
- $I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_c(x))\,\mu(V_c(x)/dx)$
- **When integrated over the channel:**

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{Th} - \frac{V_{DS}}{2}\right)V_{DS}$$

- Transistor saturates when $V_{GD} = V_{Th}$, - the channel pinches off at drain's side.

$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^2$$



# The Threshold Voltage

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

where

$V_{T0}$ is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process

- Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

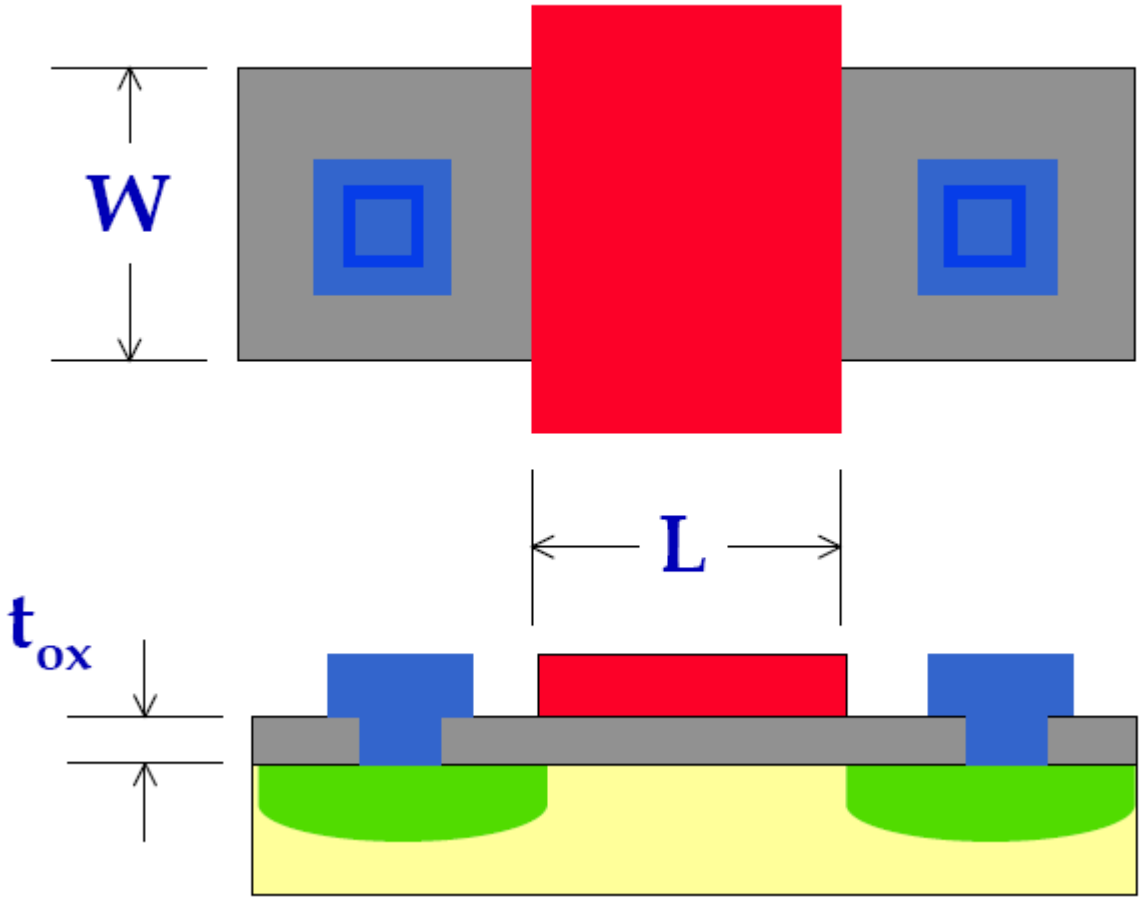
$V_{SB}$ is the source-bulk voltage

$\phi_F = -\phi_T \ln(N_A/n_i)$ is the Fermi potential ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; $N_A$ is the acceptor ion concentration; $n_i \approx 1.5 \times 10^{10}$ cm$^{-3}$ at 300K is the intrinsic carrier concentration in pure silicon)

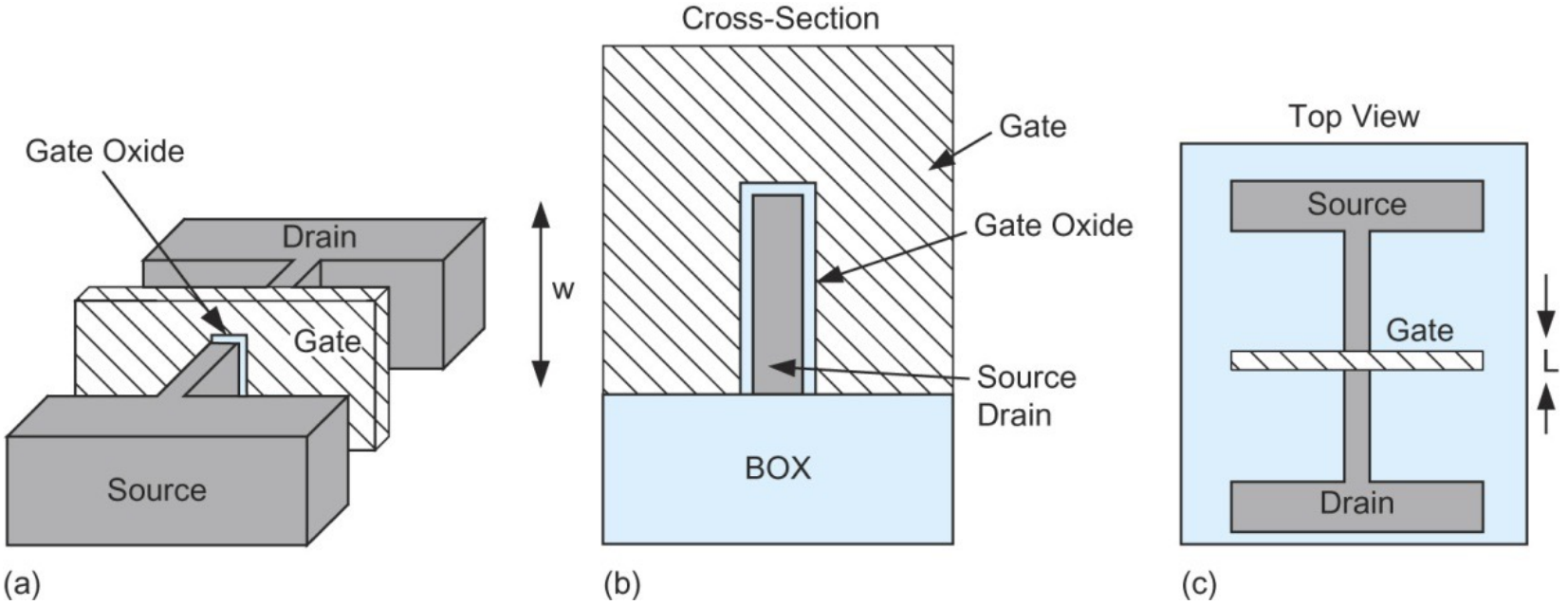
$\gamma = \sqrt{(2q\varepsilon_{si}N_A)}/C_{ox}$ is the body-effect coefficient (impact of changes in $V_{SB}$) ($\varepsilon_{si}=1.053 \times 10^{-10}$F/m is the permittivity of silicon; $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\varepsilon_{ox}=3.5 \times 10^{-11}$F/m)

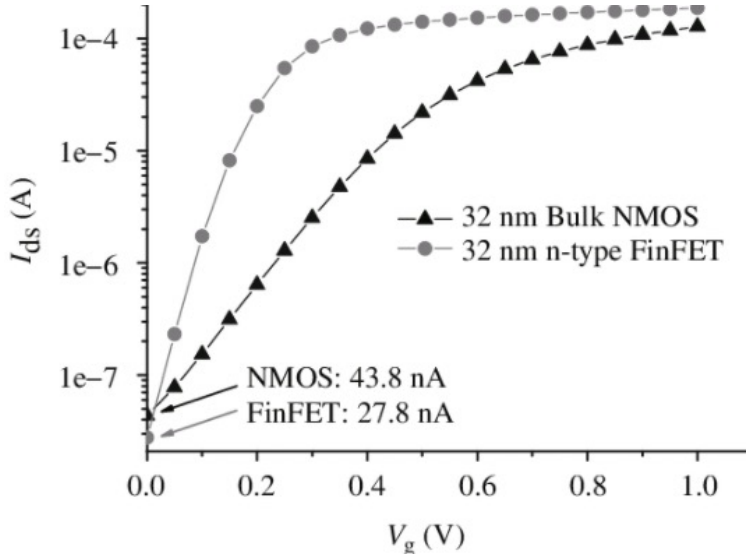
# Transistor Dimensions

- Parameter for design
  - W, L, tox, Vt



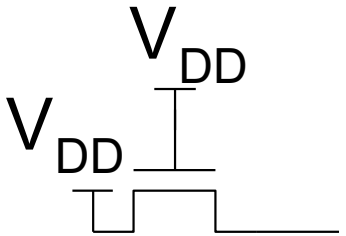
# FinFET


Gate Oxide
Drain
Gate
Source
(a)
w
Cross-Section
Gate
Gate Oxide
Source
Drain
BOX
(b)
Top View
Source
Gate
Drain
L
(c)


1e–4
1e–5
1e–6
1e–7
$I_{ds}$ (A)
32 nm Bulk NMOS
32 nm n-type FinFET
NMOS: 43.8 nA
FinFET: 27.8 nA
0.0
0.2
0.4
0.6
0.8
1.0
$V_g$ (V)

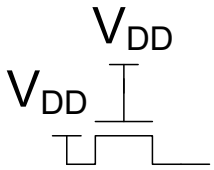
# Pass Transistors

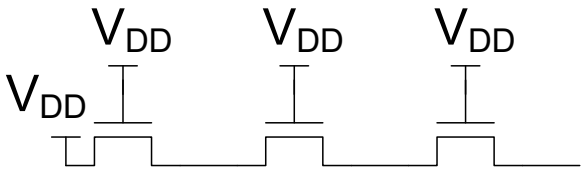
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing $V_{DD}$
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off

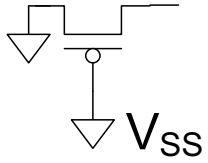


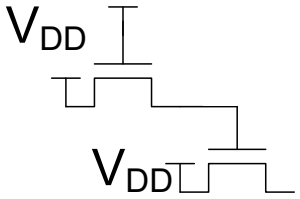

- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low $I_{ds}$)
- pMOS pass transistors pull no lower than $V_{tp}$
- Transmission gates are needed to pass both 0 and 1

# Pass Transistor Ckts



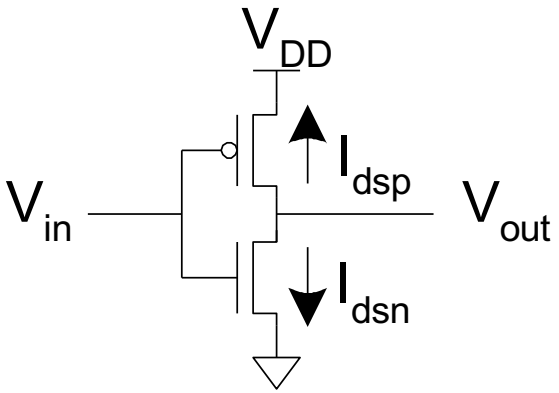



# DC Response

- DC Response: $V_{out}$ vs. $V_{in}$ for a gate
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, $V_{out}$ depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight

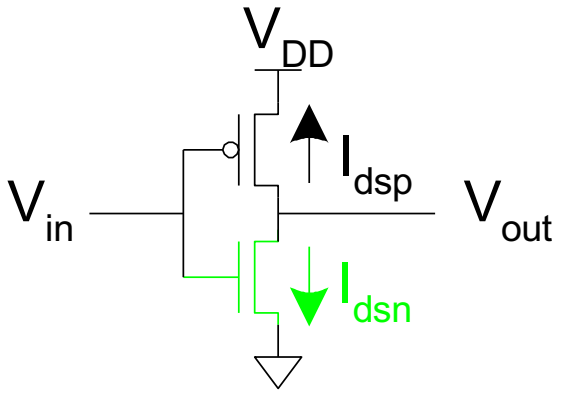


# Transistor Operation

- Current depends on region of transistor behavior
- For what $V_{in}$ and $V_{out}$ are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

# NMOS Operation

| Cutoff | Linear | Saturated |
|---|---|---|
| $V_{gsn} < V_{tn}$ | $V_{gsn} > V_{tn}$ | $V_{gsn} > V_{tn}$ |
| $V_{in} < V_{tn}$ | $V_{in} > V_{tn}$ | $V_{in} > V_{tn}$ |
| | $V_{dsn} < V_{gsn} - V_{tn}$ | $V_{dsn} > V_{gsn} - V_{tn}$ |
| | $V_{out} < V_{in} - V_{tn}$ | $V_{out} > V_{in} - V_{tn}$ |



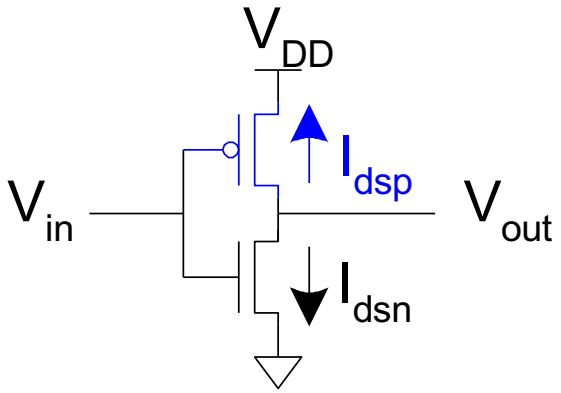
# PMOS Operation

| Cutoff | Linear | Saturated |
|---|---|---|
| $V_{gsp} > V_{tp}$<br>$V_{in} > V_{DD} + V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} > V_{gsp} - V_{tp}$<br>$V_{out} > V_{in} - V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} < V_{gsp} - V_{tp}$<br>$V_{out} < V_{in} - V_{tp}$ |

$V_{gsp} = V_{in} - V_{DD}$

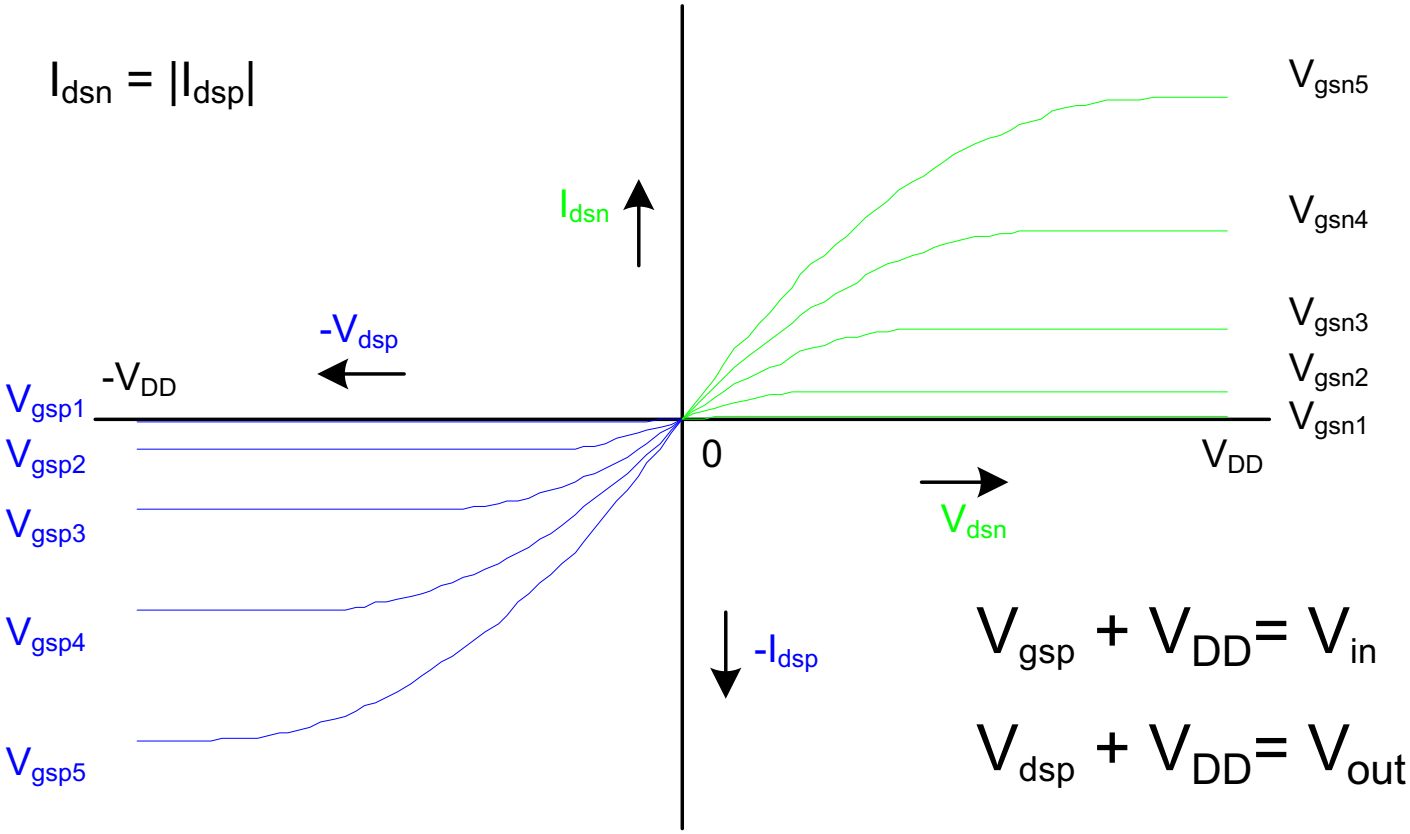
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$



# I-V Characteristics

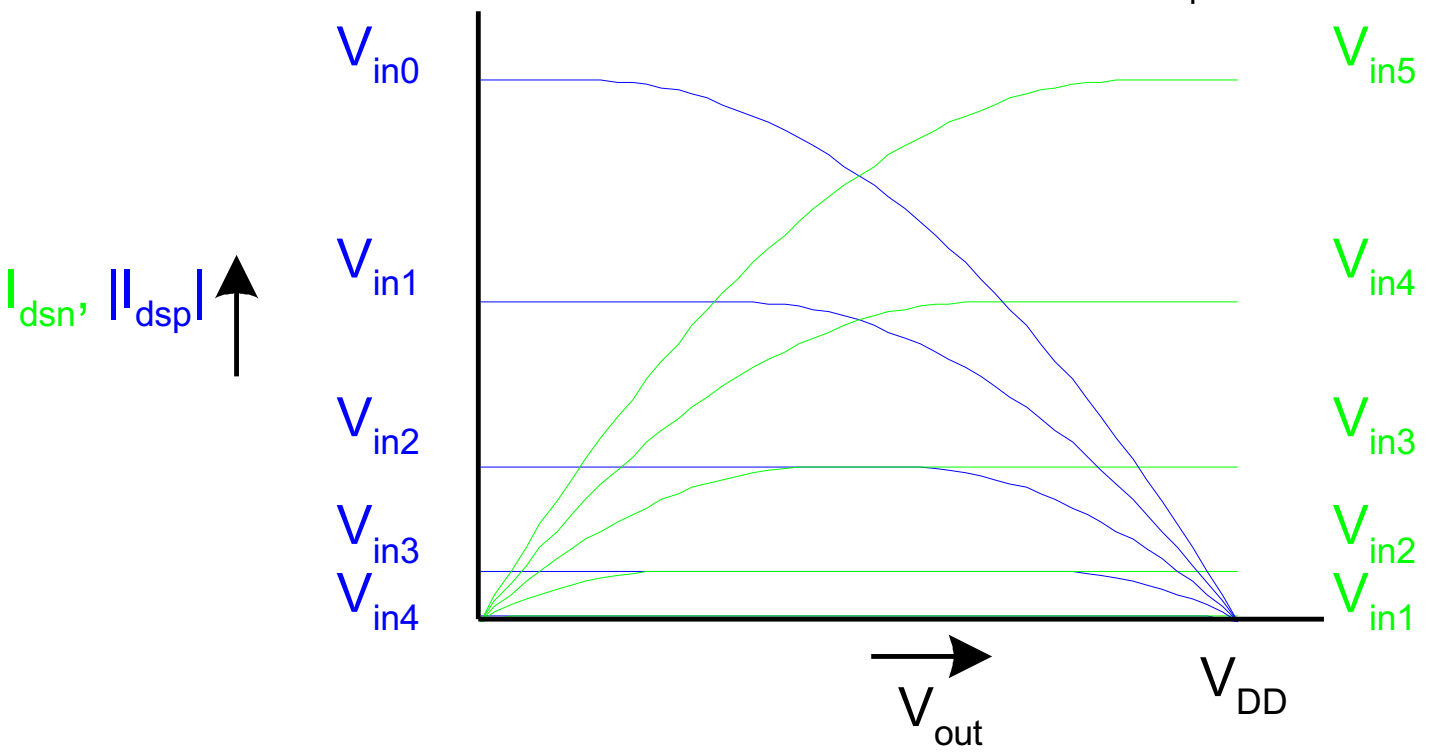
- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$



# Current vs. $V_{out}$, $V_{in}$

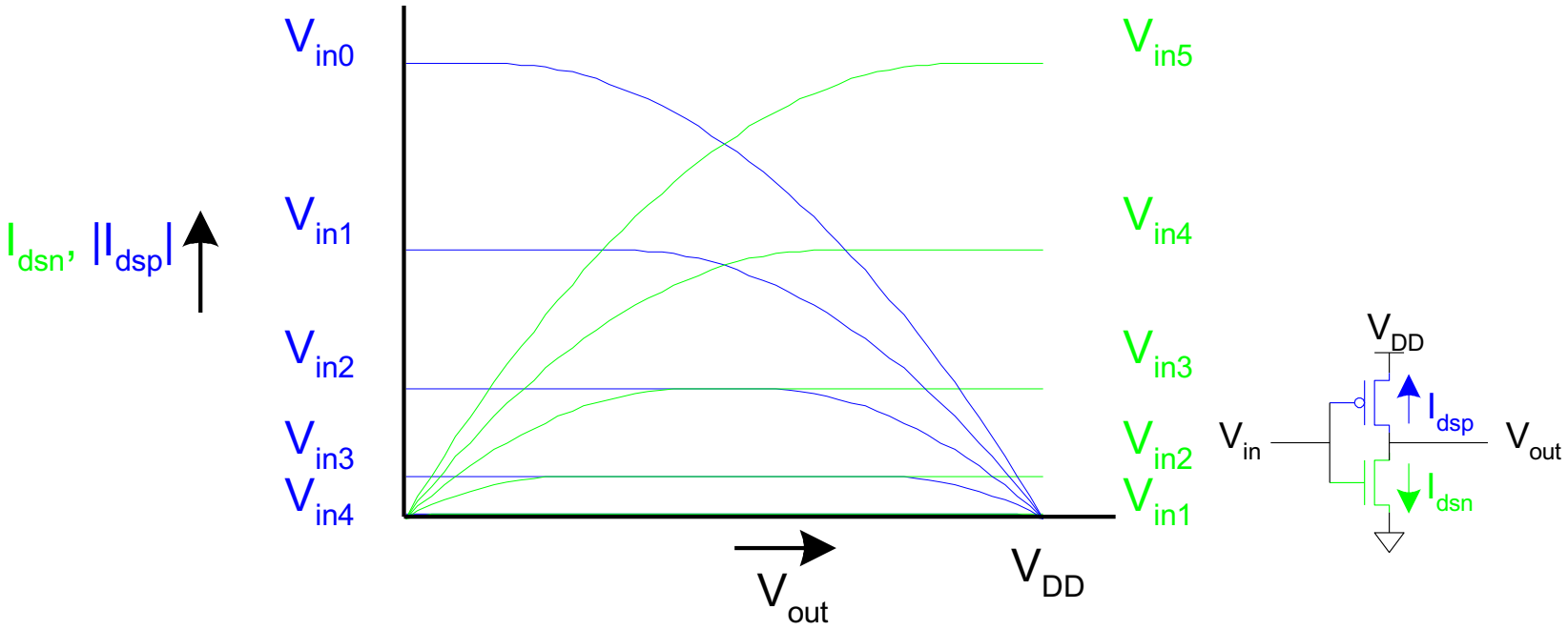
$V_{gsp} + V_{DD} = V_{in}$

$V_{dsp} + V_{DD} = V_{out}$



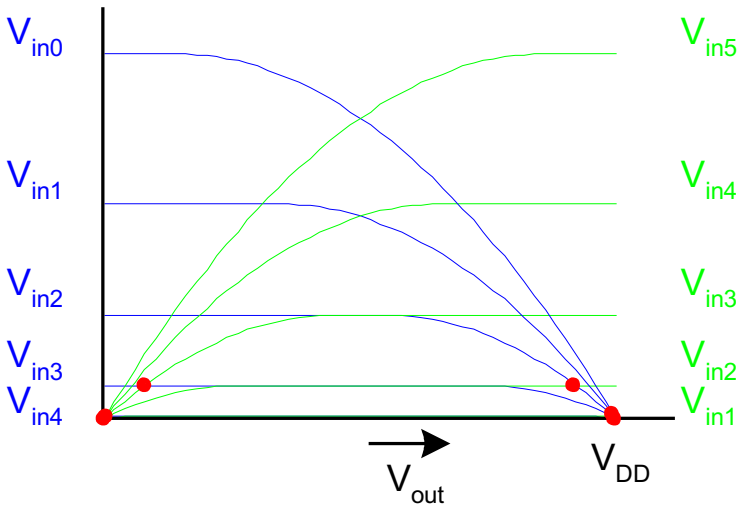
# Load Line Analysis

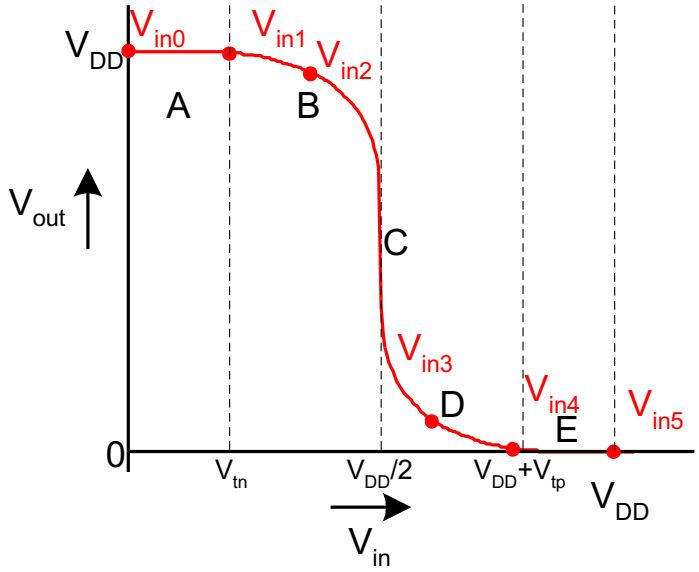
- For a given $V_{in}$:
  - Plot $I_{dsn}$, $I_{dsp}$ vs. $V_{out}$
  - $V_{out}$ must be where |currents| are equal in



# DC Transfer Curve

- Transcribe points onto $V_{in}$ vs. $V_{out}$ plot

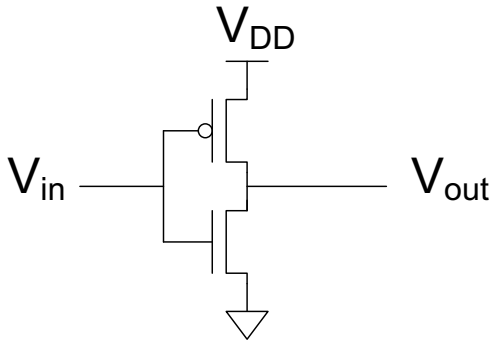


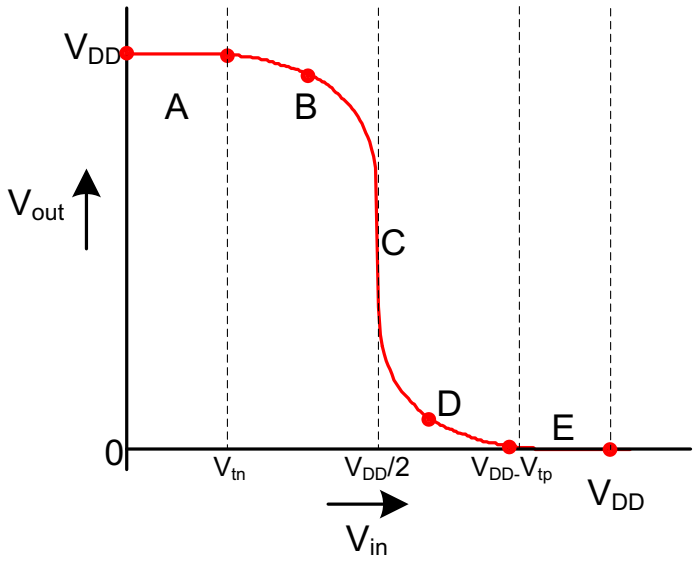



# Operating Regions

- Revisit transistor operating regions

| Region | nMOS | pMOS |
|---|---|---|
| A | Cutoff | Linear |
| B | Saturation | Linear |
| C | Saturation | Saturation |
| D | Linear | Saturation |
| E | Linear | Cutoff |

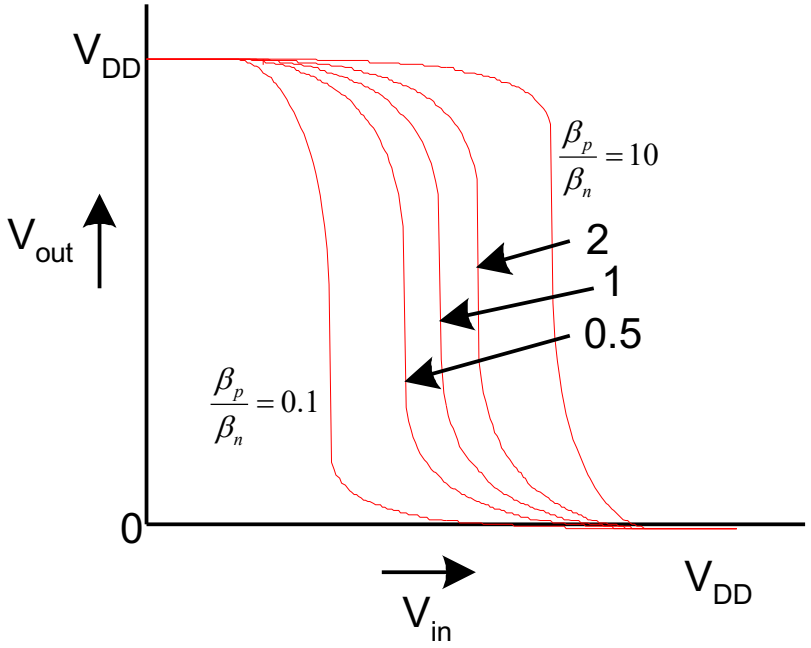



| Region | Condition | p-device | n-device | Output |
|---|---|---|---|---|
| A | $0 \le V_{in} < V_{tn}$ | linear | cutoff | $V_{out} = V_{DD}$ |
| B | $V_{tn} \le V_{in} < V_{DD}/2$ | linear | saturated | $V_{out} > V_{DD}/2$ |
| C | $V_{in} = V_{DD}/2$ | saturated | saturated | $V_{out}$ drops sharply |
| D | $V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$ | saturated | linear | $V_{out} < V_{DD}/2$ |
| E | $V_{in} > V_{DD} - \lvert V_{tp} \rvert$ | cutoff | linear | $V_{out} = 0$ |

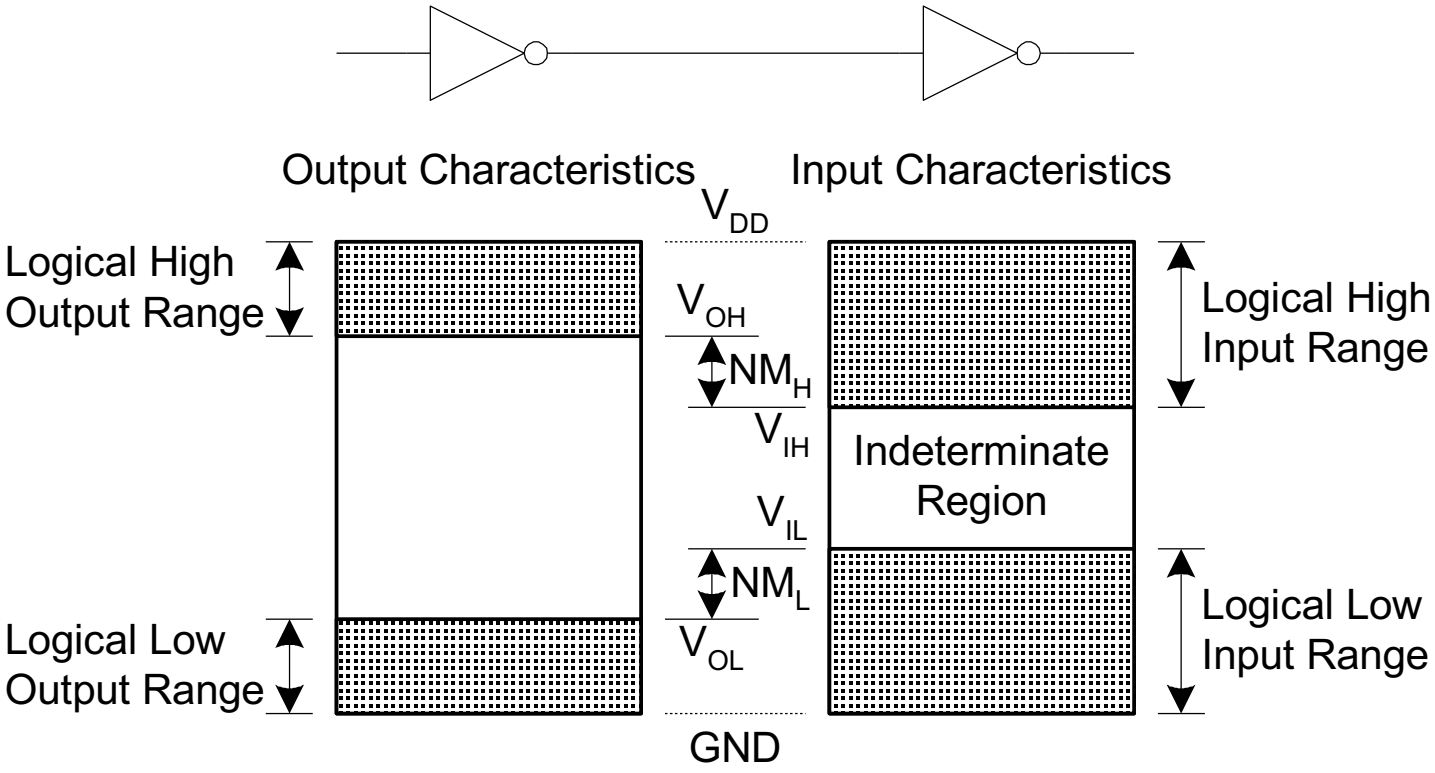
# Beta Ratio Effects

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



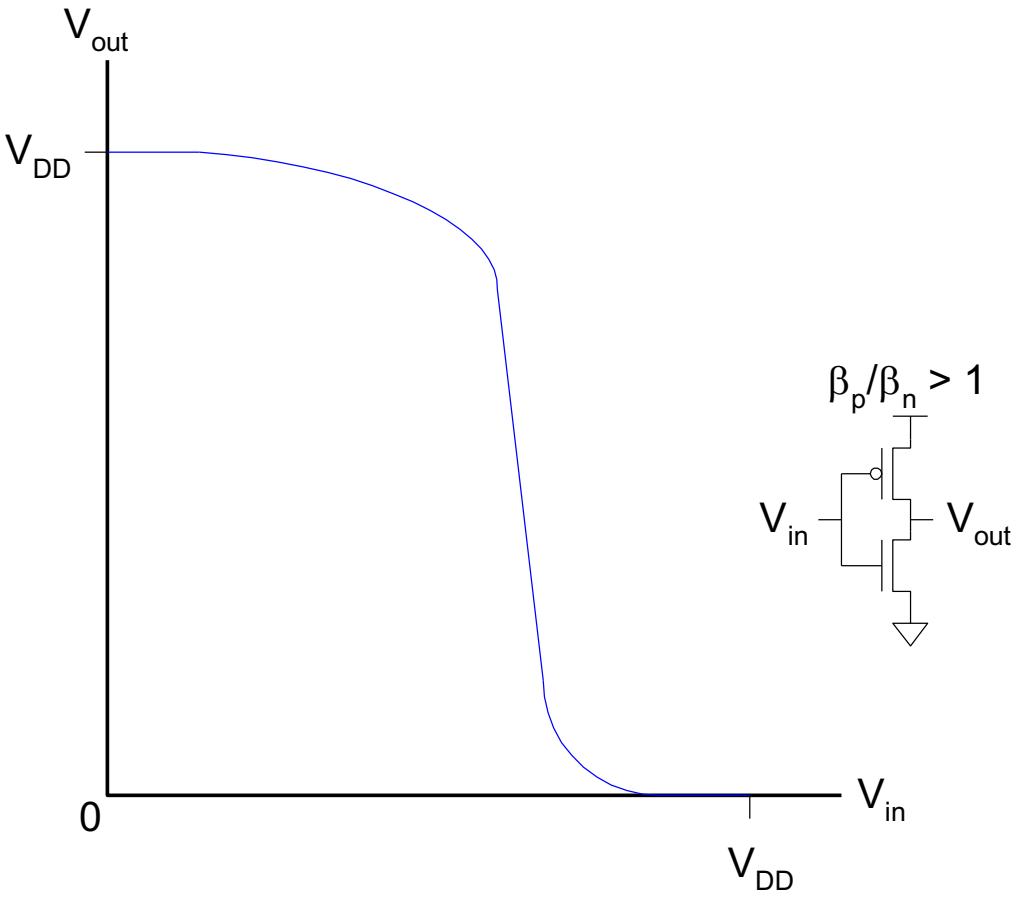
# Noise Margins

- How much noise can a gate input see before it does not recognize the input?

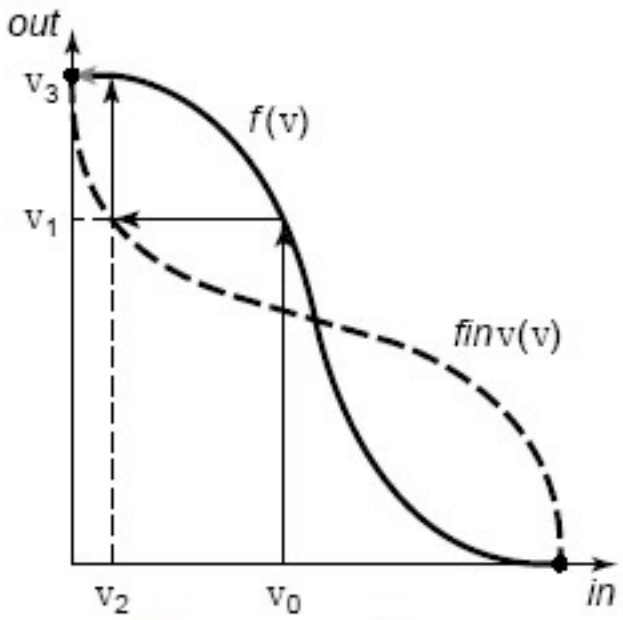


# Logic Level

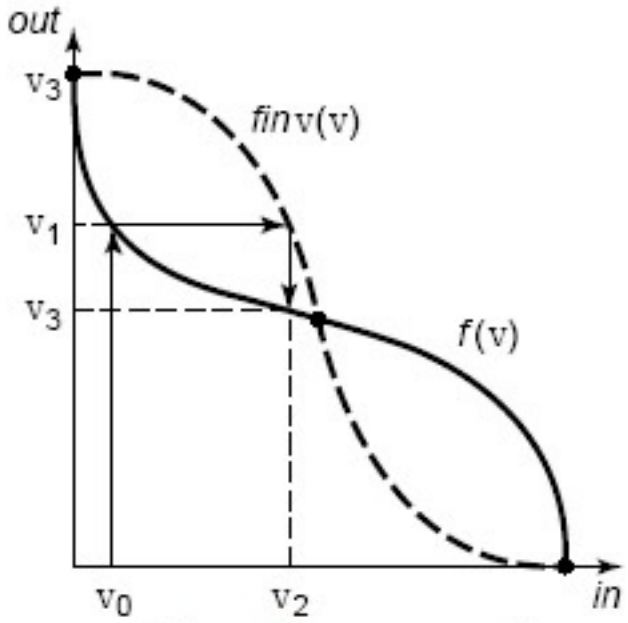
- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



# Regenerative

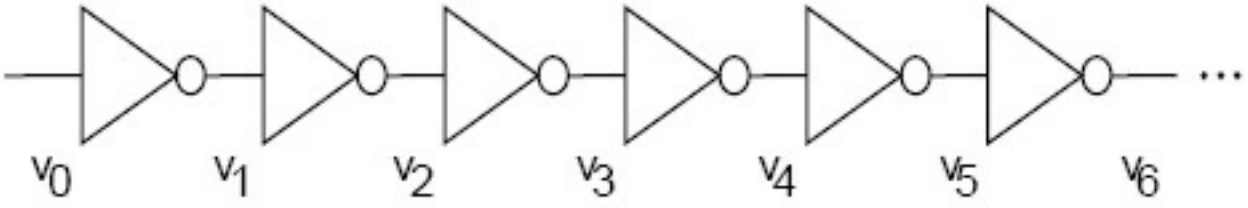


Regenerative

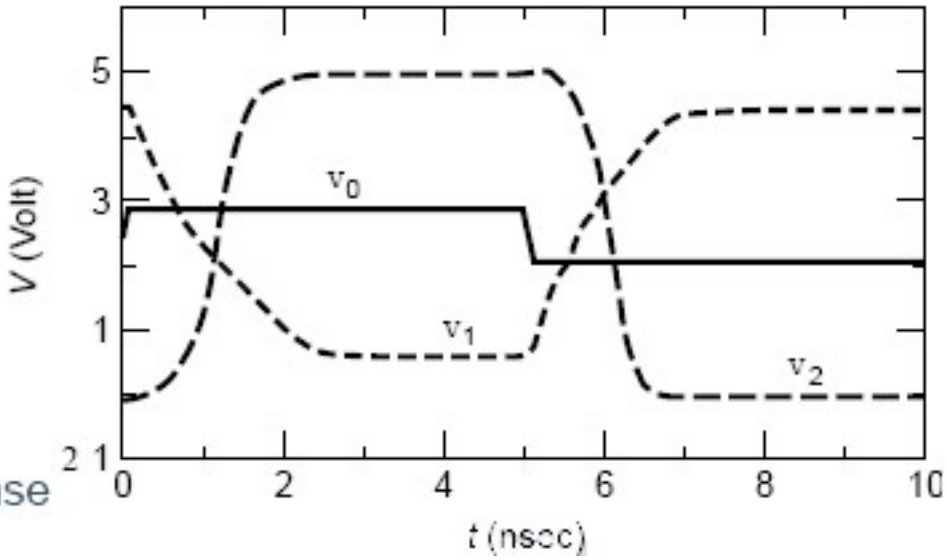


Non-Regenerative

# Regenerative Property



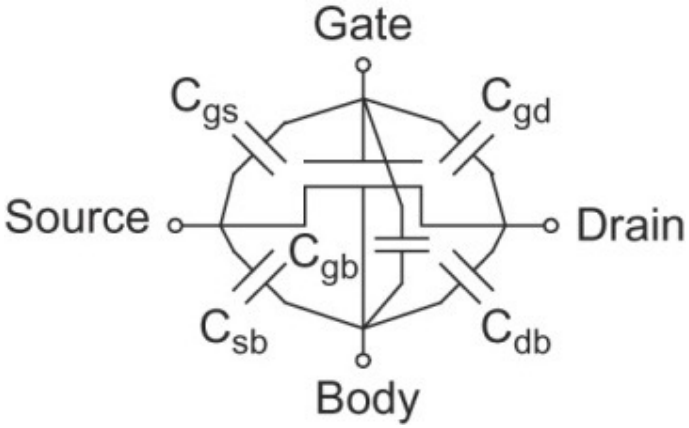

A chain of inverters



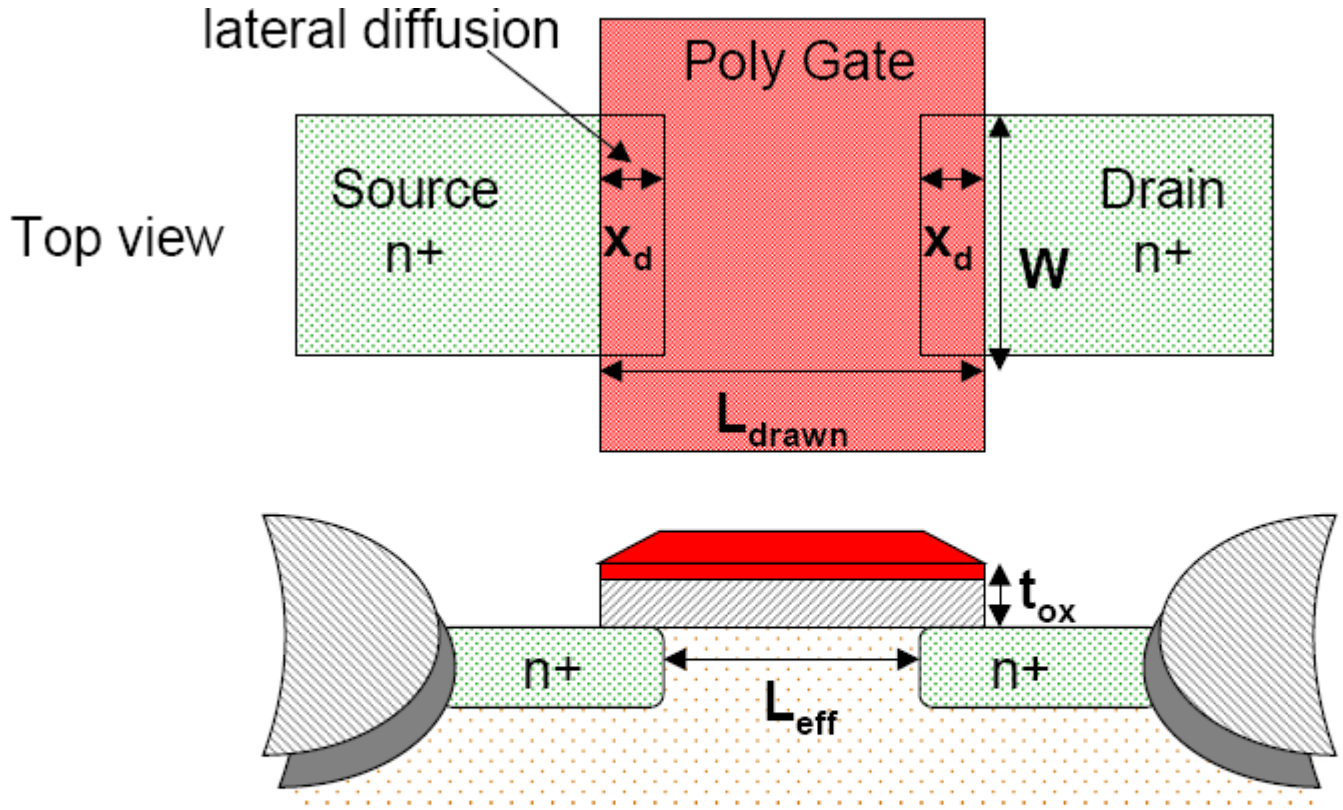

Simulated response

# Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
  - Gate capacitance
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called *diffusion capacitance* because it is associated with source/drain diffusion



# The Gate Capacitance



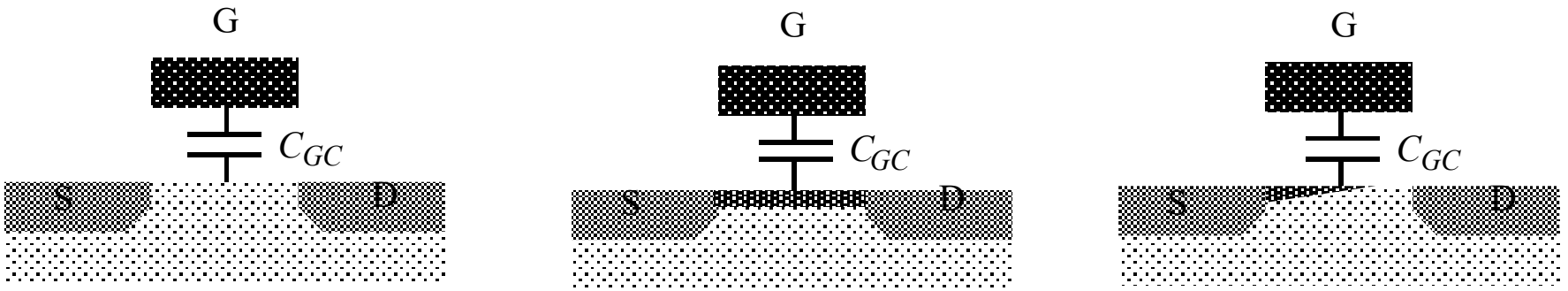

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

$=C_{permicron}*W$

$C_{permicron}$ = 2fF/um (>90nm)
or 1fF/um (<=90nm)

$= C_0$

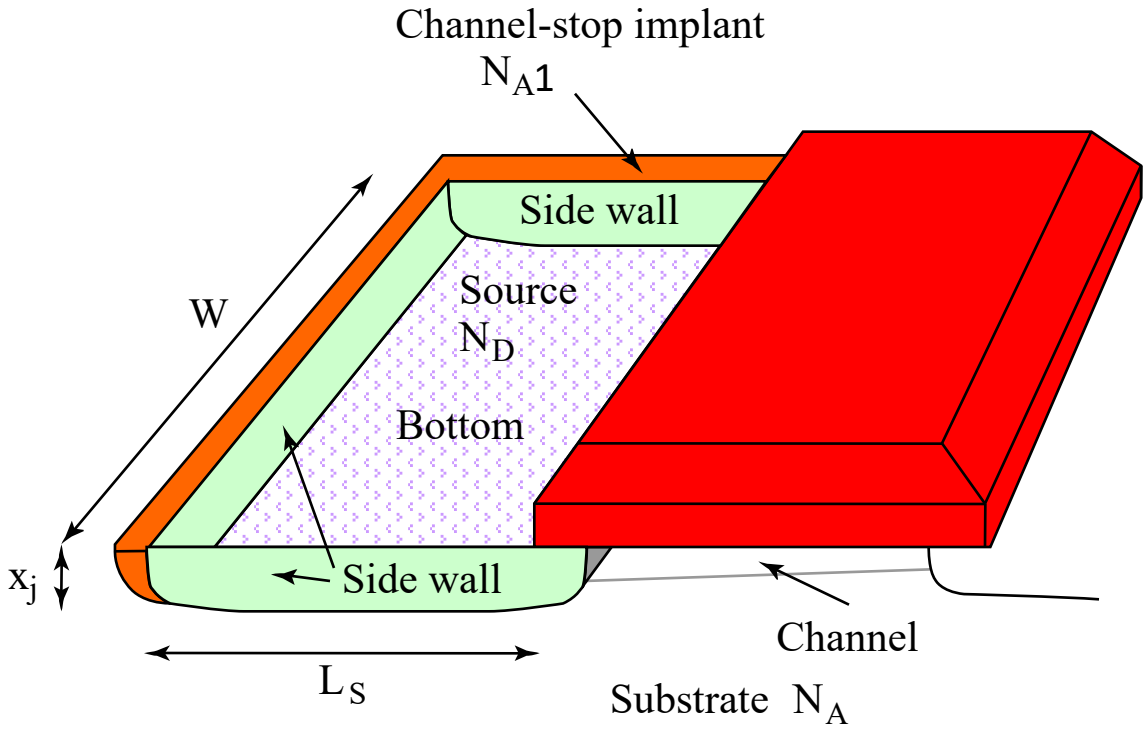
# Gate Capacitance with Operation Region




| Parameter | Cutoff | Linear | Saturation |
|---|---|---|---|
| $C_{gb}$ | $\leq C_0$ | 0 | 0 |
| $C_{gs}$ | 0 | $C_0/2$ | $2/3\ C_0$ |
| $C_{gd}$ | 0 | $C_0/2$ | 0 |
| $C_g = C_{gs} + C_{gd} + C_{gb}$ | $C_0$ | $C_0$ | $2/3\ C_0$ |

Most important regions in digital design: saturation and cut-off

# Diffusion Capacitance

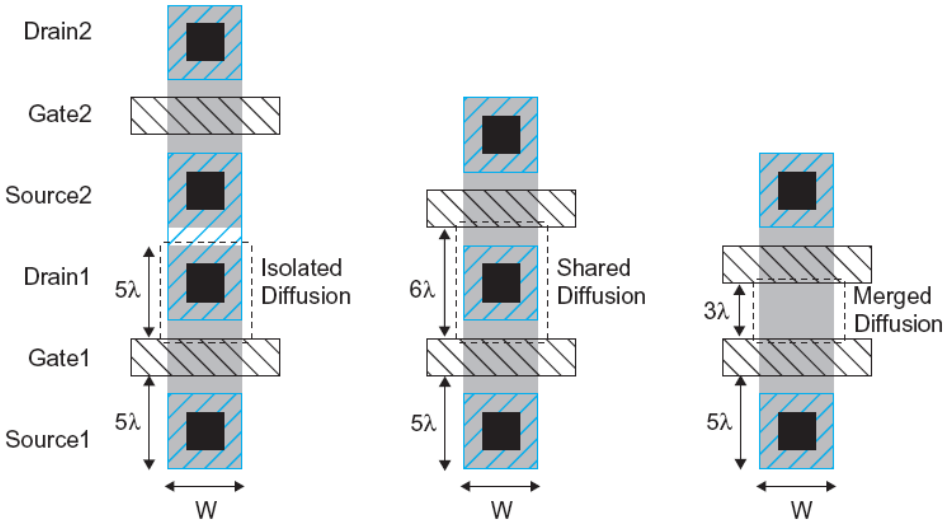



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

The junction (or diffusion) capacitance is from the reverse-biased source-body and drain-body pn junctions.

# Diffusion Capacitance

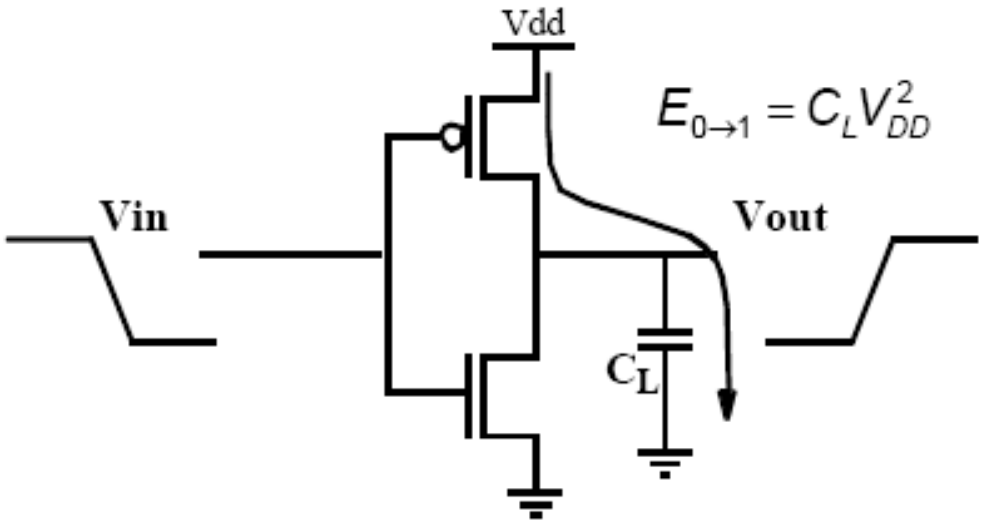
- $C_{sb}$, $C_{db}$
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to $C_g$ for contacted diff
  - ½ $C_g$ for uncontacted
  - Varies with process



# Where Does Power Go in CMOS?

- Switching power
  - Charging/Discharging capacitors
- Leakage power
  - Transistors are imperfect switches
  - Junction diodes
- Short-circuit power
  - Both pull-up and pull-down on during transition

# Dynamic Power Dissipation




$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

$$E_{0\to1} = \int_0^T P_{DD}(t)dt = V_{DD}\int_0^T i_{DD}(t)dt = V_{DD}\int_0^{V_{DD}} C_L\, dv_{out} = C_L V_{DD}^2$$

$$E_C = \int_0^T P_C(t)dt = \int_0^T v_{out}\, i_L(t)dt = \int_0^{V_{DD}} C_L v_{out}\, dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

- Not a function of transistor sizes!
- Need to reduce CL, Vdd, and *f* to reduce power.

# Activity and Power Transition

- Energy consumed in $N$ cycles, $E_N$,

$$\boldsymbol{E_N = C_L \times V_{DD}^2 \times n_{0\to1}}$$

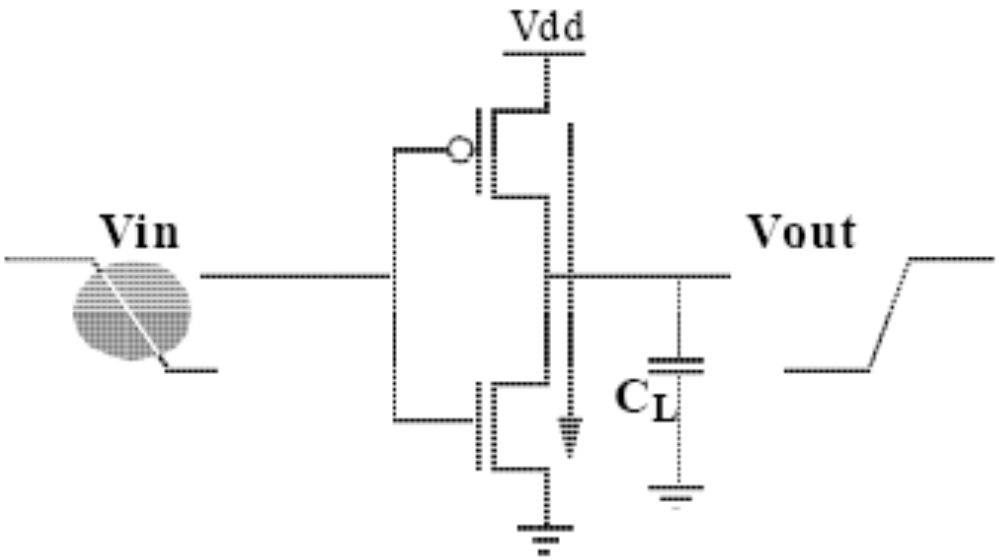
$n_{0\to1}$: number of 0→1 in $N$ cycles

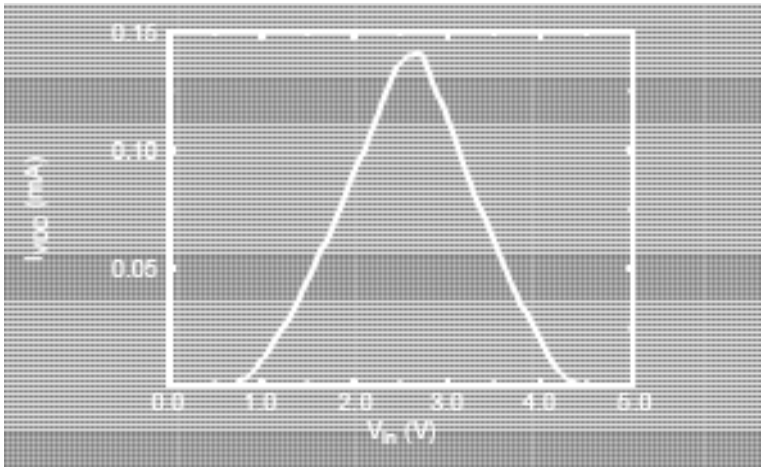
$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \left(\lim_{N\to\infty} \frac{n_{0\to1}}{N}\right) \cdot C_L \cdot {V_{DD}}^2 \cdot f$$

$$\alpha_{0\to1} = \lim_{N\to\infty} \frac{n_{0\to1}}{N}$$

$$\boldsymbol{P_{avg} = \alpha_{0\to1} \cdot C_L \cdot {V_{DD}}^2 \cdot f}$$

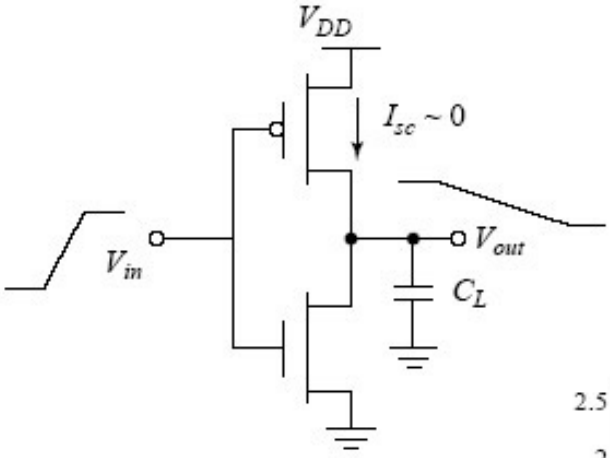
# Short Circuit



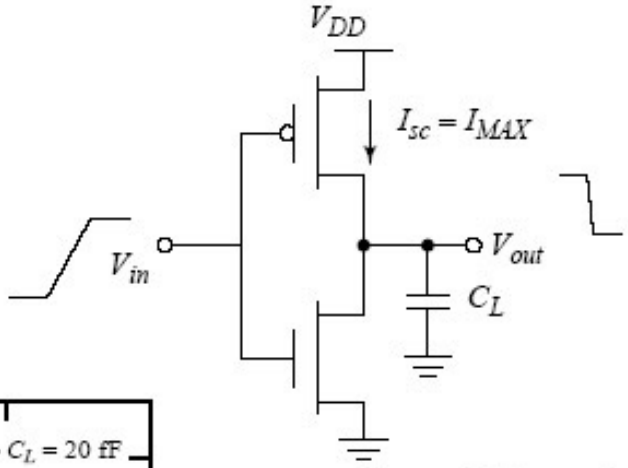



# Short Circuit Current

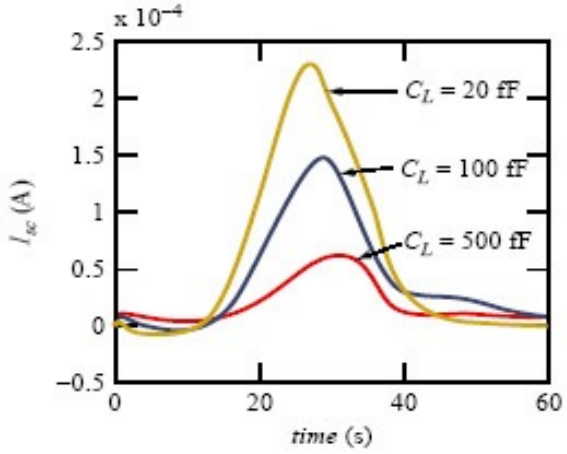
- Short circuit current is usually well controlled




Large load

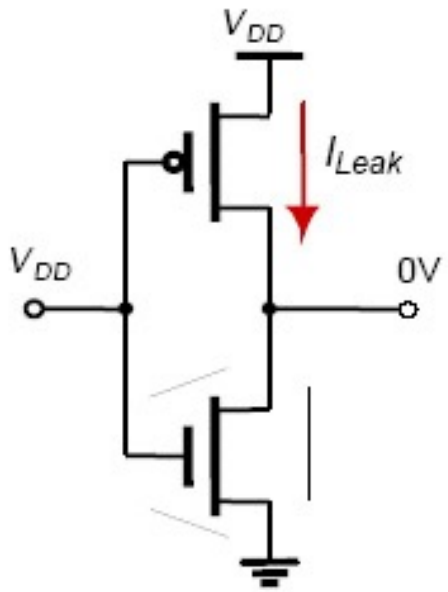



Small load

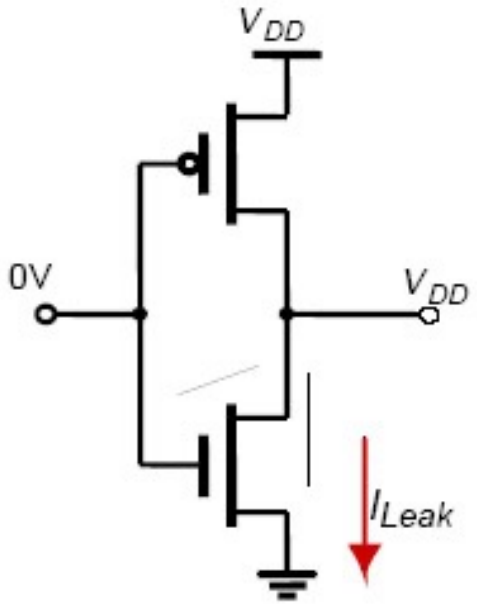


# Transistor Leakage

- Transistors that are supposed to be off-leak



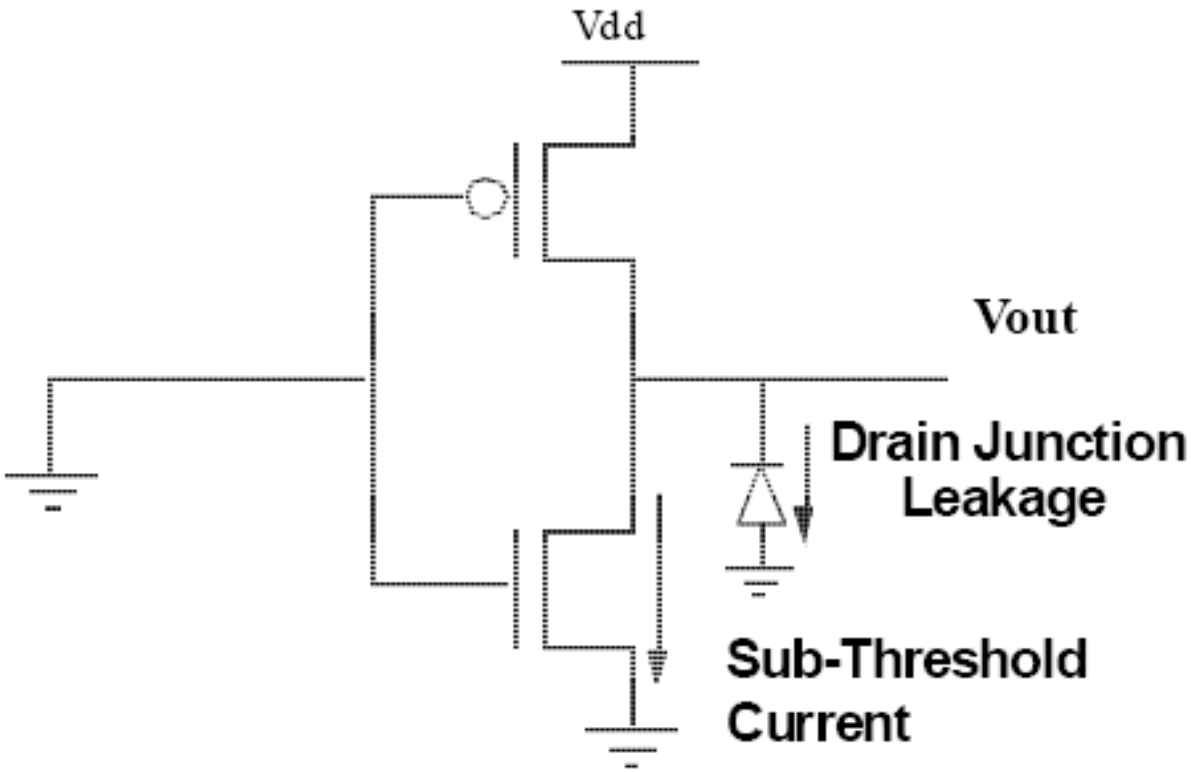

Input at $V_{DD}$



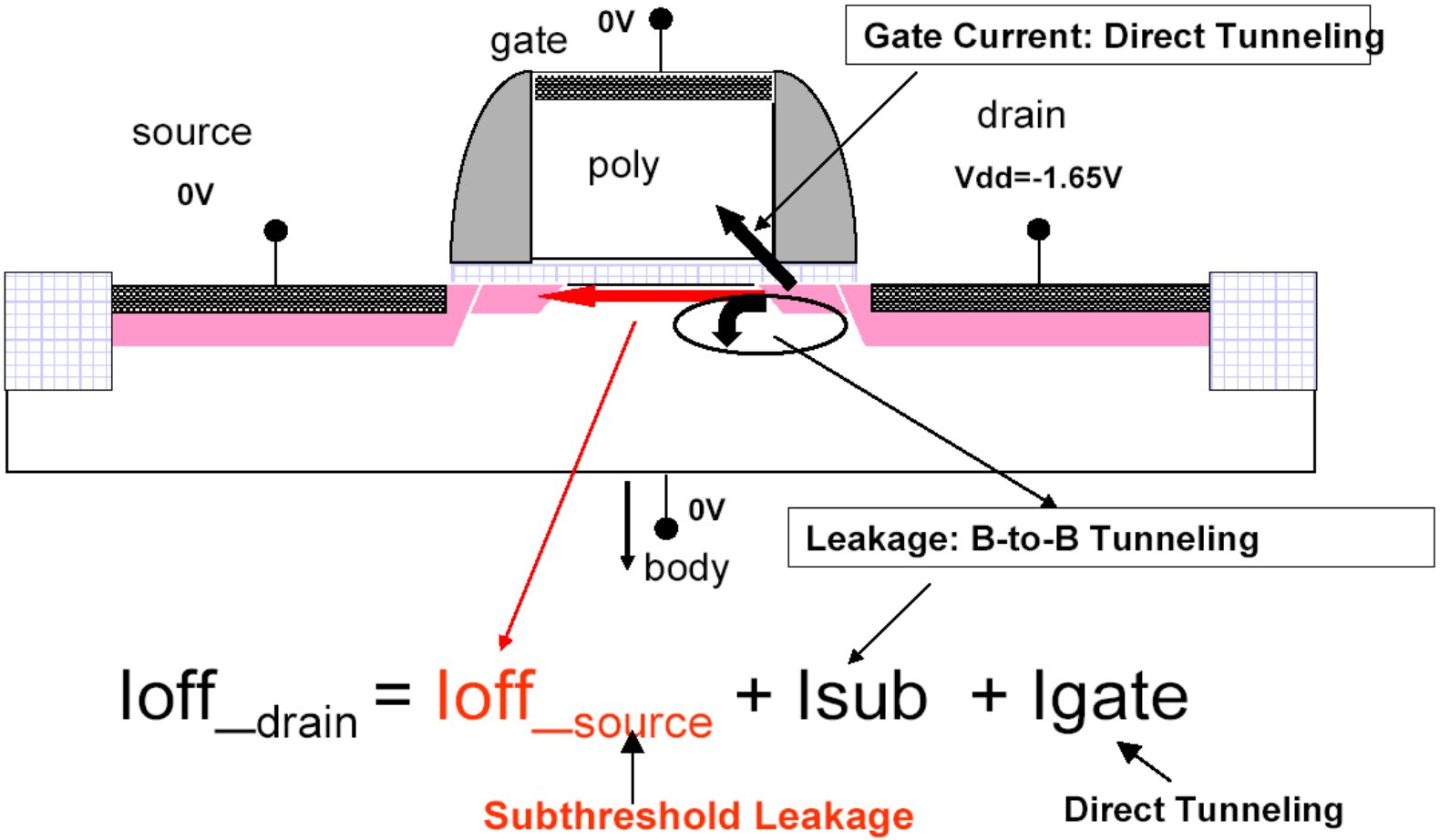

Input at 0

# Sub-threshold Leakage

- Sub-threshold current one of most compelling issues in low-energy circuit design!

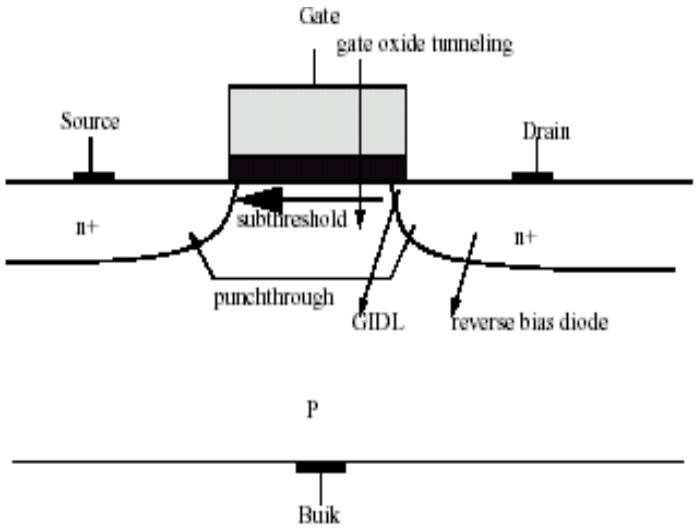


# Source of Leakage



# Leakage Sources for Static CMOS Transistors

- **PN reverse bias junction leakage - $I_B$**
  - Electron-hole pair generation in the depletion region
  - Band to band tunneling when the electric field approaches $10^6$V/cm
- **Subthreshold leakage - $I_s$**
  - Weak inversion current between source and drain
  - It increase exponentially with the reduction of the threshold voltage
  - SCE, DIBL make it even worse
- **Gate Induced Drain Leakage(GIDL) - $I_B$**
  - Occur at high electric field between drain and gate terminal
- **Punch-through - $I_D$**
  - Occur when the drain and source depletion approach each other
- **Gate Oxide Tunneling - $I_G$**
  - Due to the high electric field in the gate oxide- Direct tunnel since tox < 20A



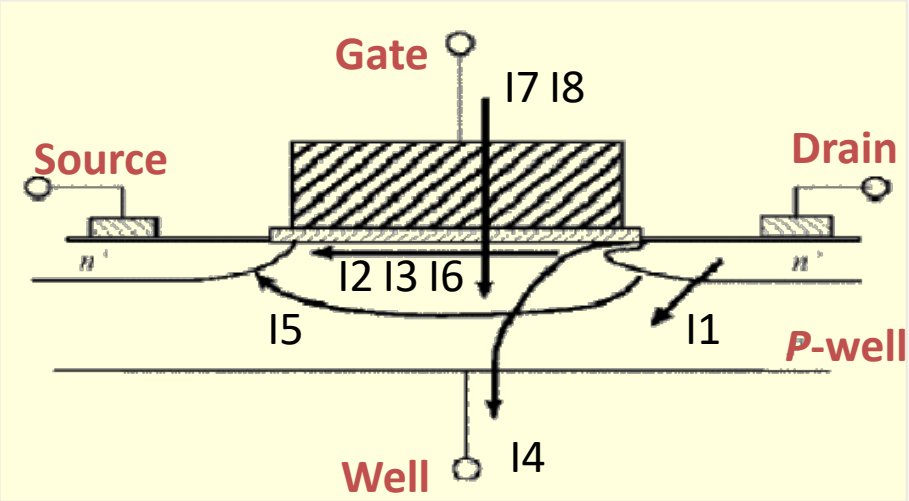

$I_{off} = I_B + I_S + I_G$ in normal operating voltage range

$I_B$ : be careful when back gate biased

$I_S$ : major contribution > 90%

$I_G$: can not be ignore from N90

# Leakage Currents of Nano-Scale Transistors




I1 : p-n Junction Reverse Bias Current

I2 : Weak Inversion

I3 : DIBL (Drain-Induced Barrier Lowering)

I4 : GIDL (Gate-Induced Drain Leakage)

I5 : Punchthrough

I6 : Narrow Width Effect

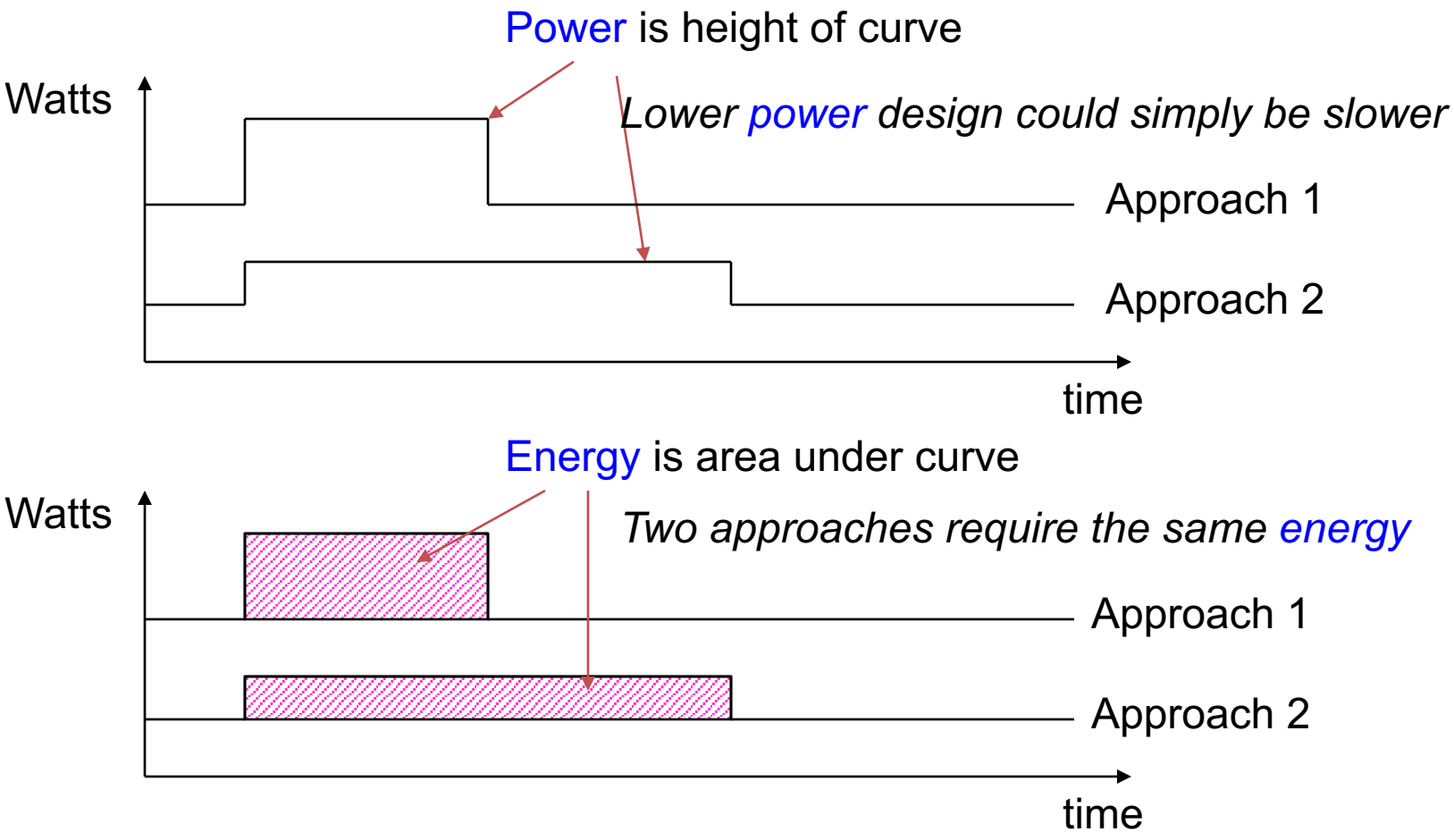
I7 : Gate Oxide Tunneling

I8 : Hot Carrier Injection

# Power and Energy Figures of Merit

- Power consumption in Watts
  - determines battery life in hours
- Peak power
  - determines power ground wiring designs
  - sets packaging limits
  - impacts signal noise margin and reliability analysis
- Energy efficiency in Joules
  - rate at which power is consumed over time
- Energy = power * delay
  - Joules = Watts * seconds
  - lower energy number means less power to perform a computation at the same frequency

# Power versus Energy



# CMOS Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\to1} + t_{sc} V_{DD} I_{peak} P_{0\to1} + V_{DD} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\to1} + t_{sc} V_{DD} I_{peak} f_{0\to1} + V_{DD} I_{leakage}$$

Dynamic power

Short-circuit power

Leakage power