Digital IC Design

Exercise 6
Clock Domain Crossing (CDC)

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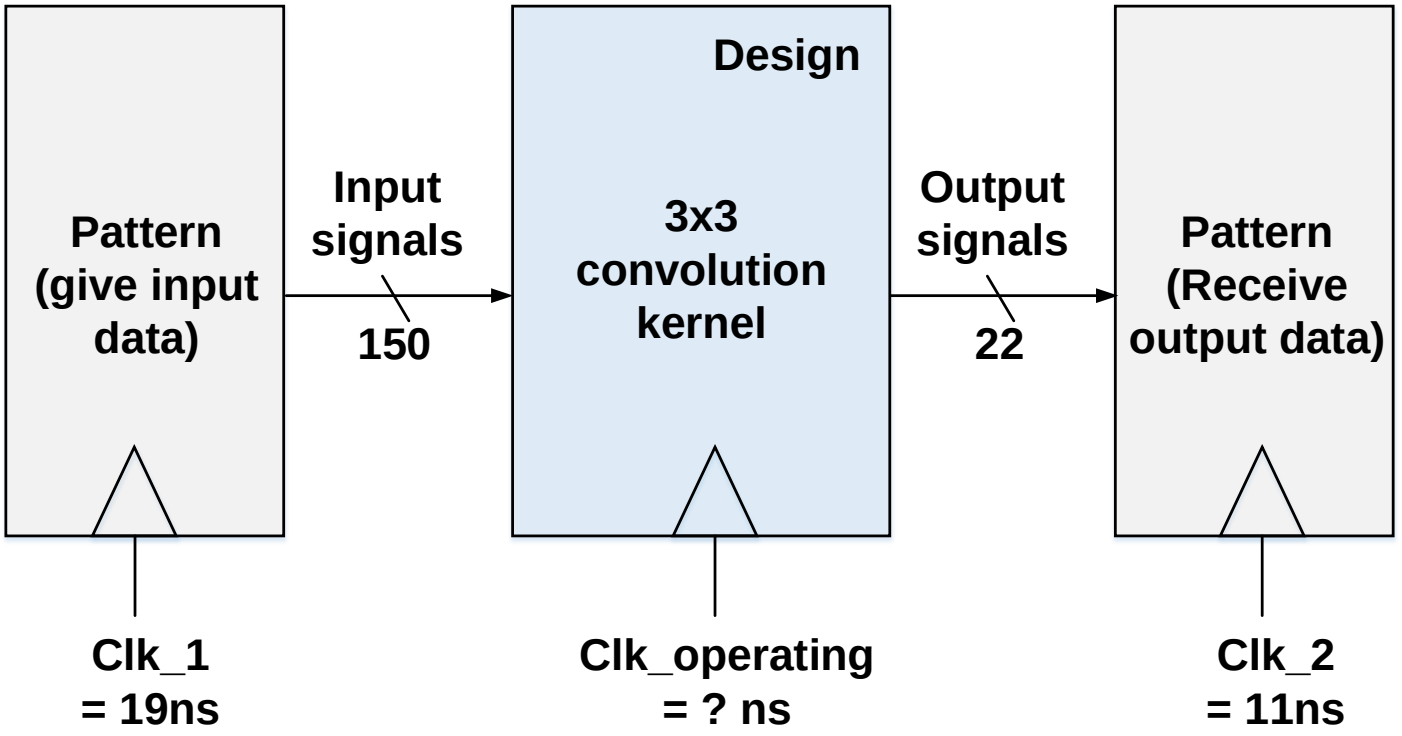
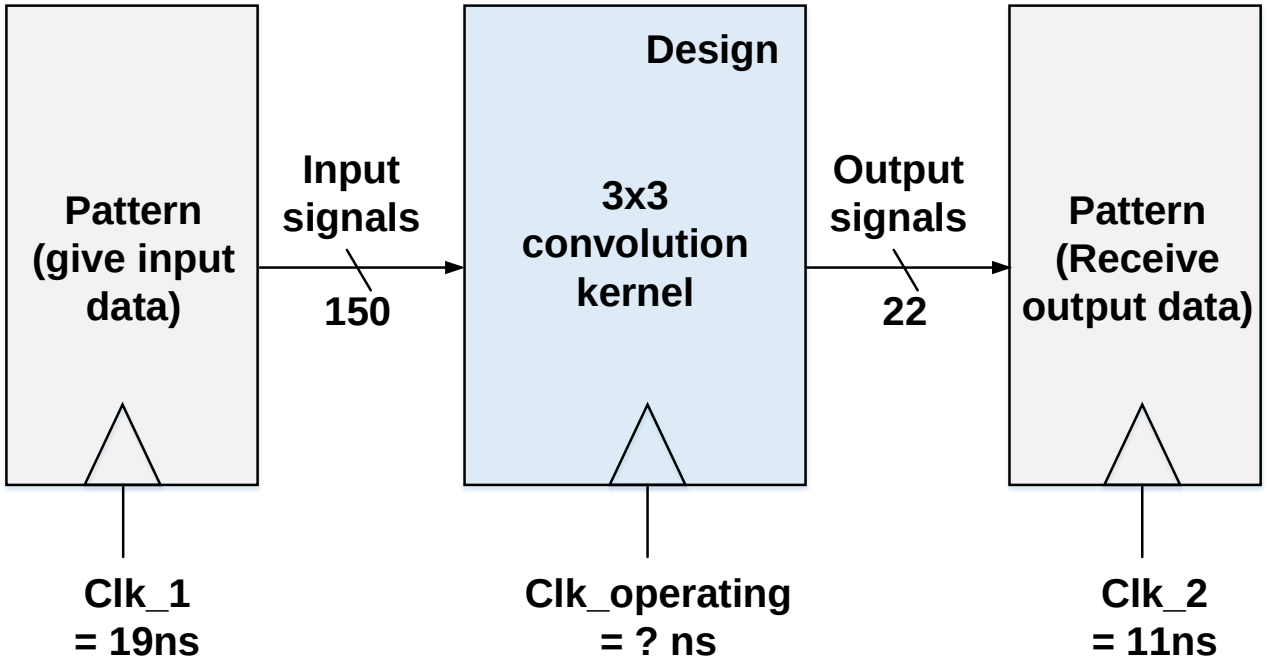
6-1 Clock Domain Crossing [60%]

- Design a 3x3 convolution kernel according to the following specifications
  - Input signals(cycle time = 19ns)
  - Output signals(cycle time = 11ns)

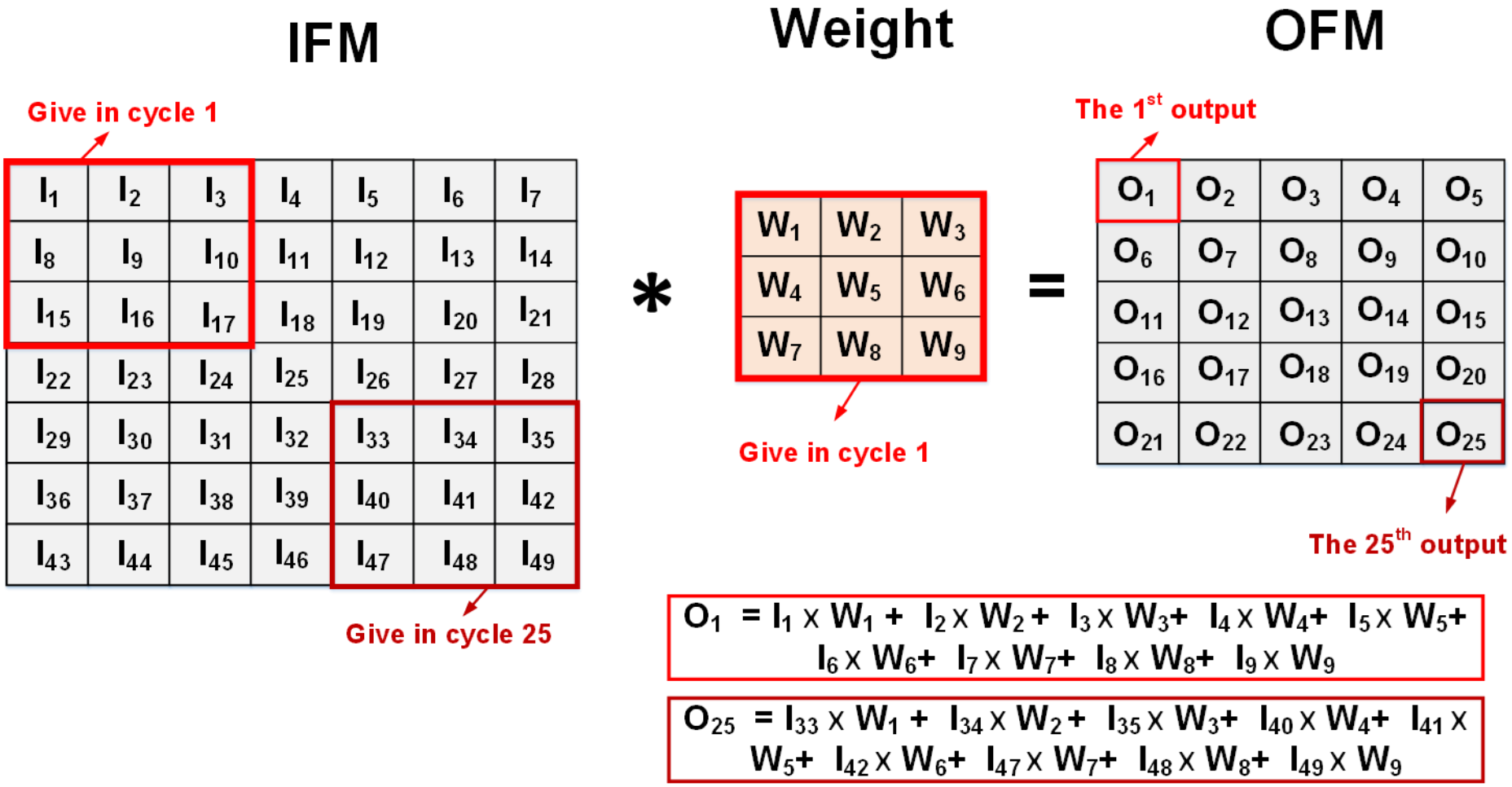


6-1 Clock Domain Crossing [60%]

- Design a 3x3 convolution kernel according to the following specifications
  - The cycle time of clk_operating is defined by yourself
  - Verify the design in gate level simulation using the pattern provided by TA.



3x3 Convolution (Parallel input)



$$O_1 = I_1 \times W_1 + I_2 \times W_2 + I_3 \times W_3 + I_4 \times W_4 + I_5 \times W_5 + I_6 \times W_6 + I_7 \times W_7 + I_8 \times W_8 + I_9 \times W_9$$

$$O_{25} = I_{33} \times W_1 + I_{34} \times W_2 + I_{35} \times W_3 + I_{40} \times W_4 + I_{41} \times W_5 + I_{42} \times W_6 + I_{47} \times W_7 + I_{48} \times W_8 + I_{49} \times W_9$$

Specifications for 3x3 convolution kernel

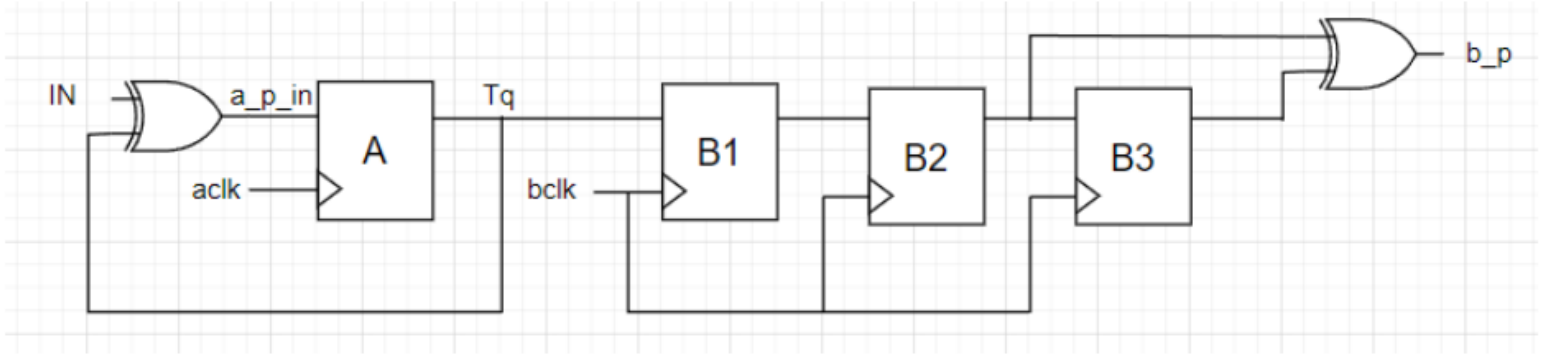
- Signals:

Input signals	Bit width	Description
Clk_1	1	Positive edge trigger clock, cycle time is **19ns**
Clk_2	1	Positive edge trigger clock, cycle time is **11ns**
Clk_operating	1	Positive edge trigger clock, cycle time is **? ns (define by yourself)**
rst_n	1	Asynchronous active-low reset.
in_valid	1	When High, **In_IFMs** are valid
Weight_valid	1	When High, **In_Weights** are valid
In_IFM_1-9	8	Input feature map **(9 signals), give in 25 cycles, cycle time is 19ns**
In_Weight_1-9	8	Weights **(9 signals), give in one cycle, cycle time is 19ns**

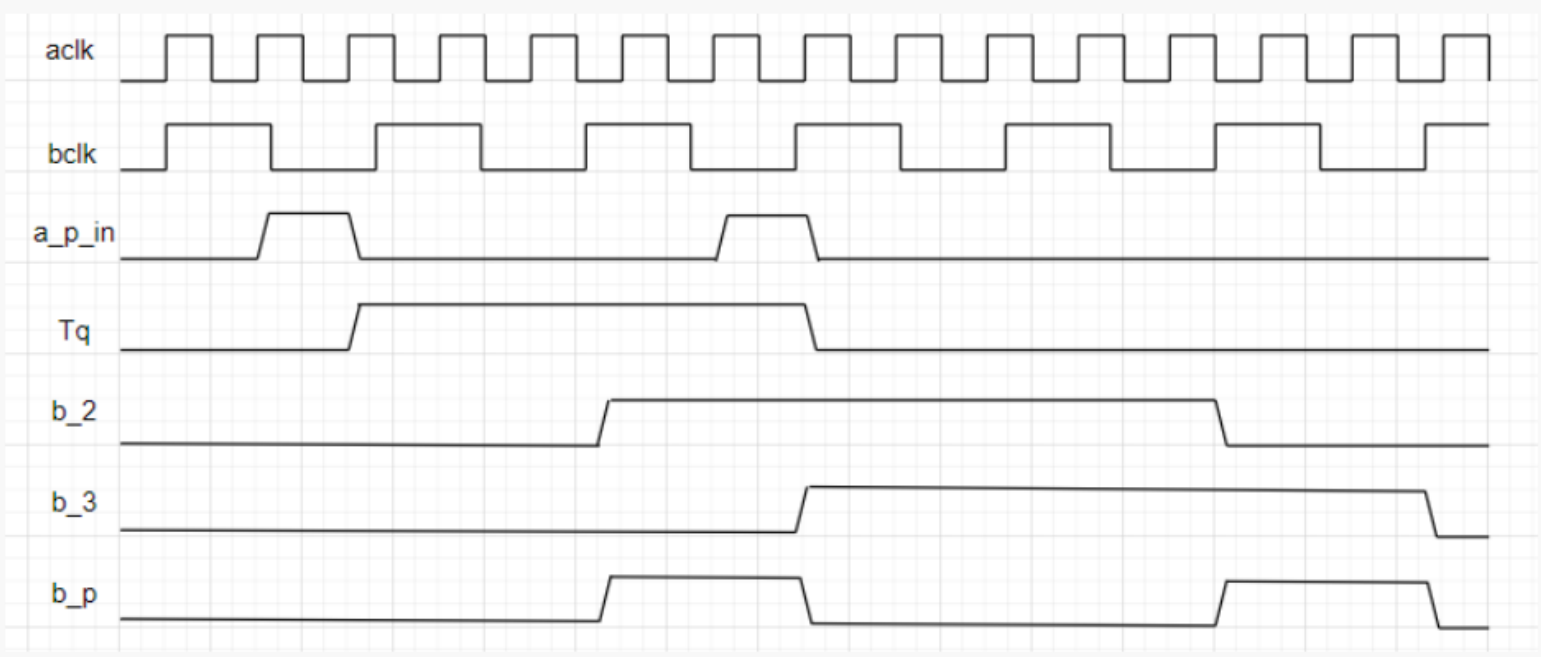
Output signals	Bit width	Description
Out_valid	1	High when out is valid, then Patten will check Out_OFM, **cycle time is 11ns**
Out_OFM	21	The answers of the 3x3 convolution, **cycle time is 11ns**

- Settings:
  - **In_IFMs & In_Weights should be received by registers.**
  - **The output ports should be set as registers.**

Example of Synchronizer



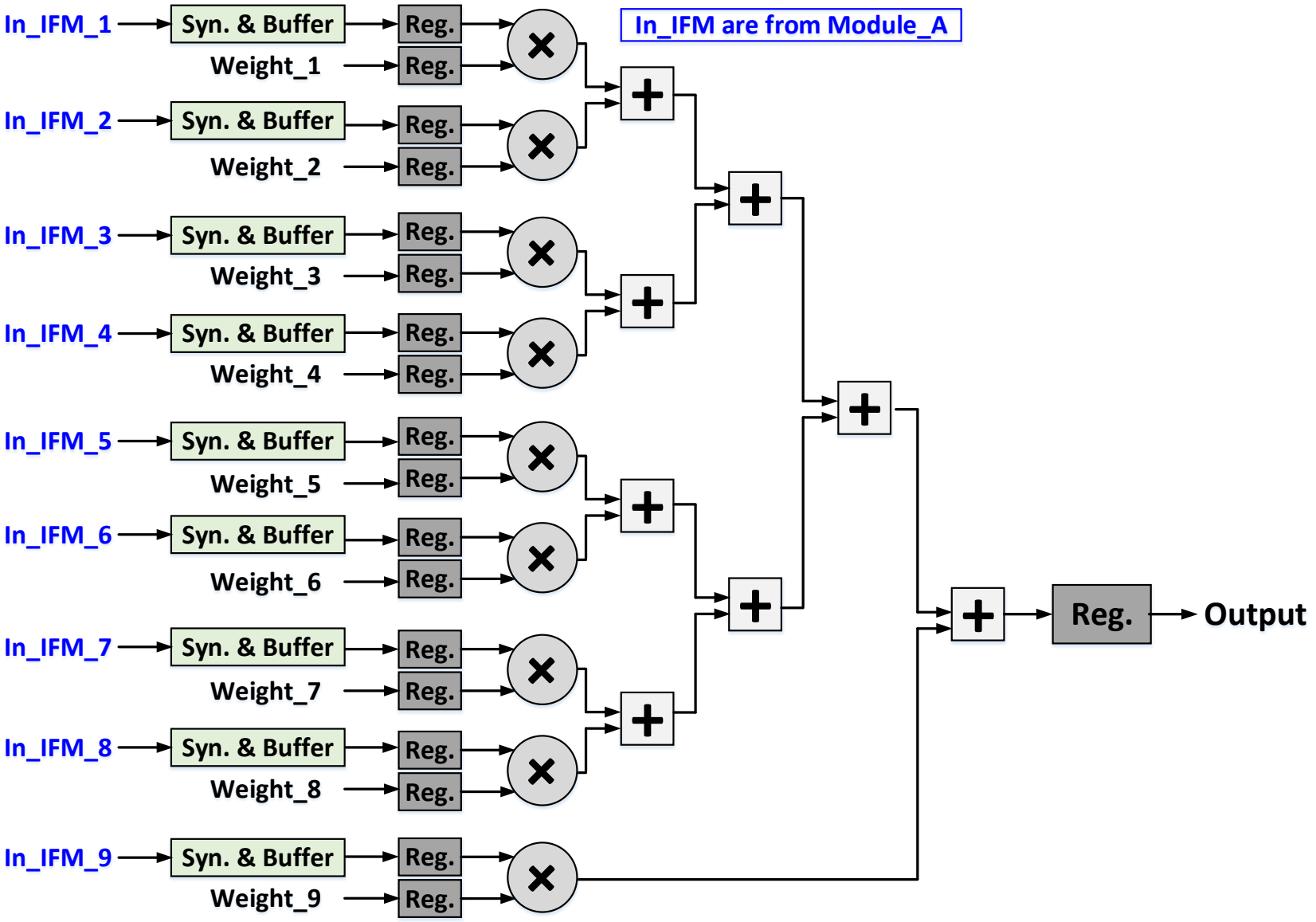
Pulse synchronizer using XOR



6-2 Limitation of average bandwidth [40%]

- Inference the CNN model, some preprocessing of input image are required before doing the convolution. A CNN inference processor is consisted by two modules, Module_A and Module_B, and the information is as follows:
  - The Module_A is used to preprocess input images, and the Module_A will output preprocessed data to Module_B then do the 3x3 convolution.
  - Module_B is a 3x3 convolution kernel, which is consisted by nine 8bit-multipliers with an adder tree, and the cycle time of the kernel is 9ns.
    - The nine 8bit weight has been stored in Module_B.
- In order to ensure that module_B can correctly receive data from module_A for convolution, what is the limitation on the average output bandwidth of module_A?
  - The buffer size of module_B is not infinite

Block diagram of Module_B



Submission of Exerice-6

- Please upload the following files
  - Due day: PM 11:55 on 01/08
  - Naming rule:
    - Ex_6_student_ID.tar(.rar / .zip)
      - 3x3_Convolution_CDC.v
      - **Operating_cycle_time.txt (e.g. ?ns.txt)**
      - Report.pdf