Digital IC Design

Lecture 10:
Variability & Reliability for IC Design

黃柏蒼 **Po-Tsang (Bug) Huang**
bughuang@nycu.edu.tw

International College of Semiconductor Technology
National Chiao Tung Yang Ming University

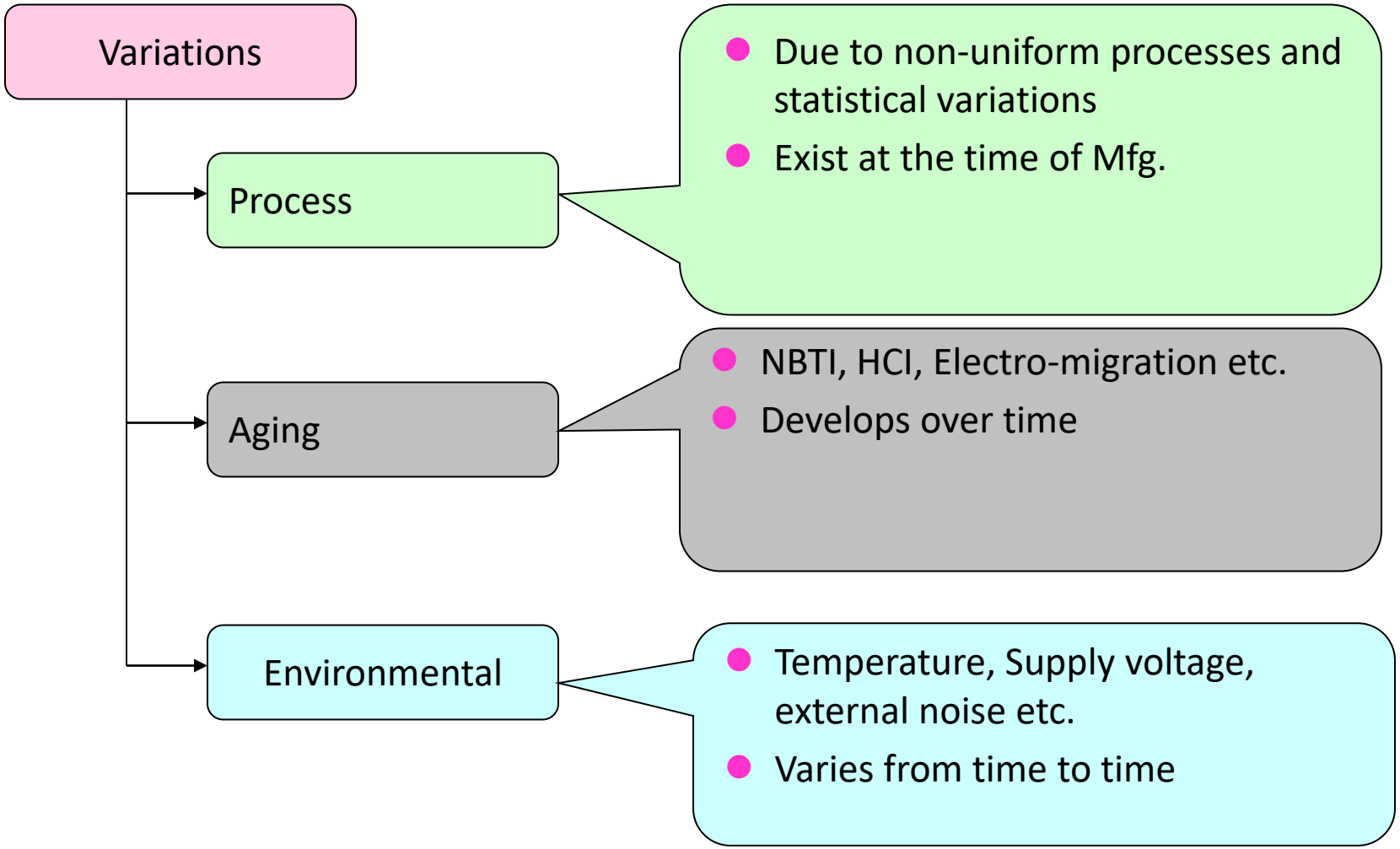
國立陽明交通大學
NATIONAL YANG MING CHIAO TUNG UNIVERSITY

Variability/Reliability Sources

- *Physical (Reliability)*
  - **Changes in characteristics of devices and wires.**
  - **Caused by IC manufacturing process & wear-out (electromigration).**
  - **Time scale: 10^{9}sec (years)**

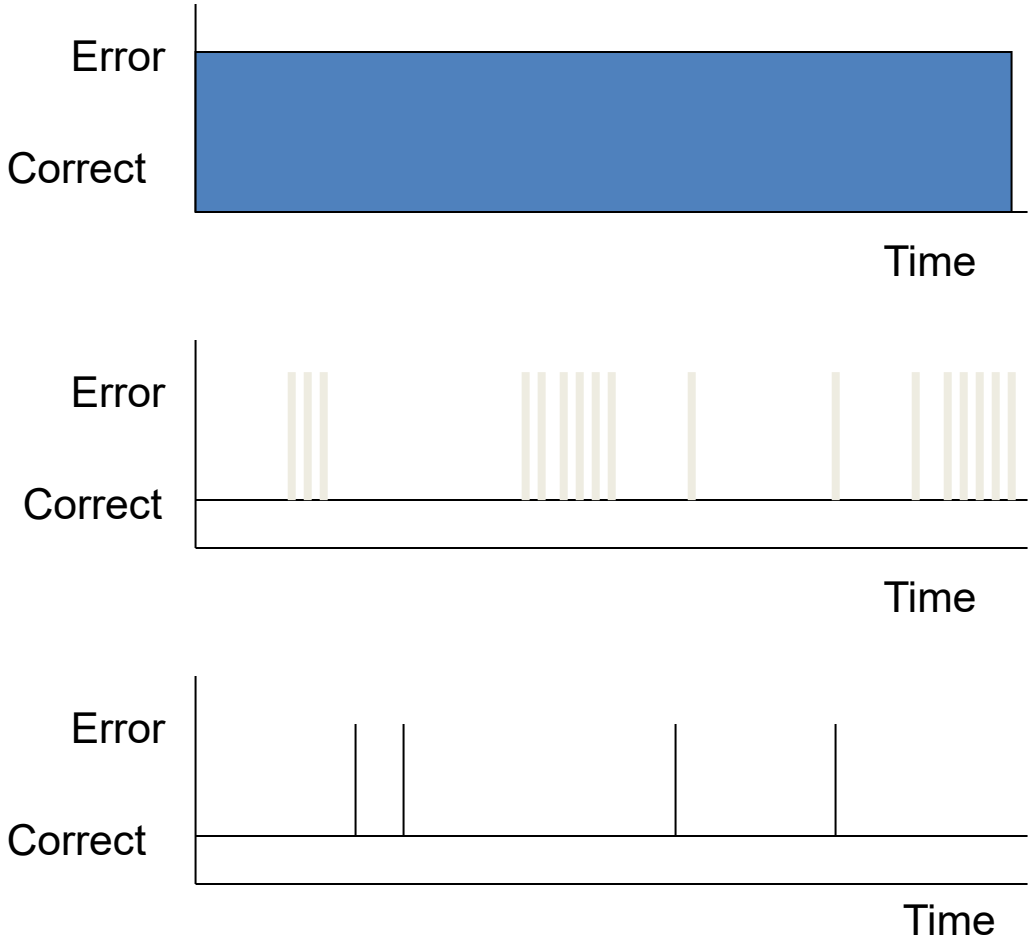
- *Environmental (Variability)*
  - **Changes in VDD, Temperature, local coupling.**
  - **Caused by the specifics of the design implementation.**
  - **Time scale: 10^{-6} to 10^{-9} sec (clock tick)**

Cause of Variations

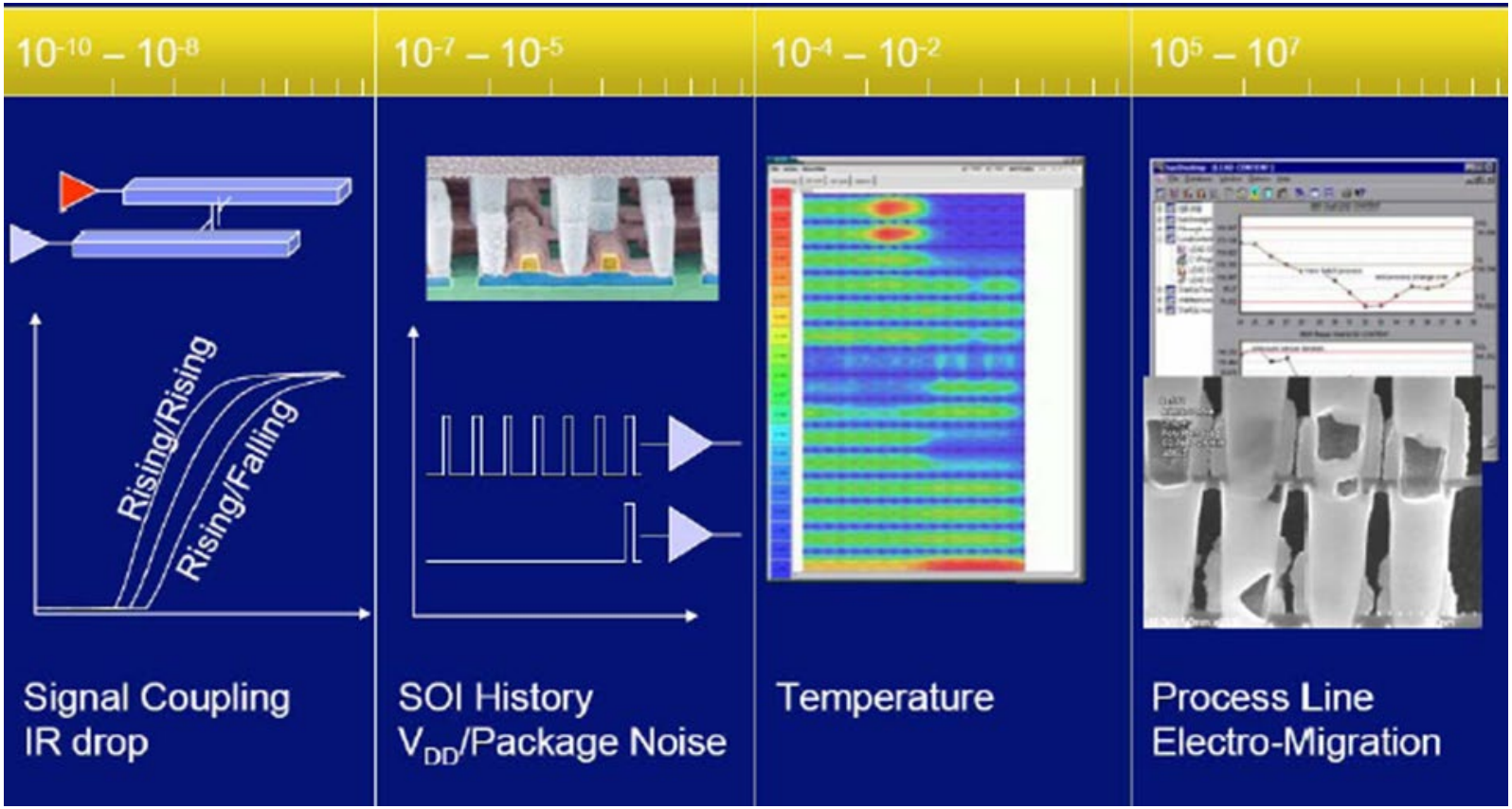


Types of Errors

- Hard Error
  - Broken connection, short circuit, large parameter variation
- Intermittent Error
  - Bursty occurrence
  - Marginal circuit
    - Breaking connection
    - Parameter Variation
- Soft Error
  - Random occurrence
  - Radiation induced
  - Marginal circuit + noise

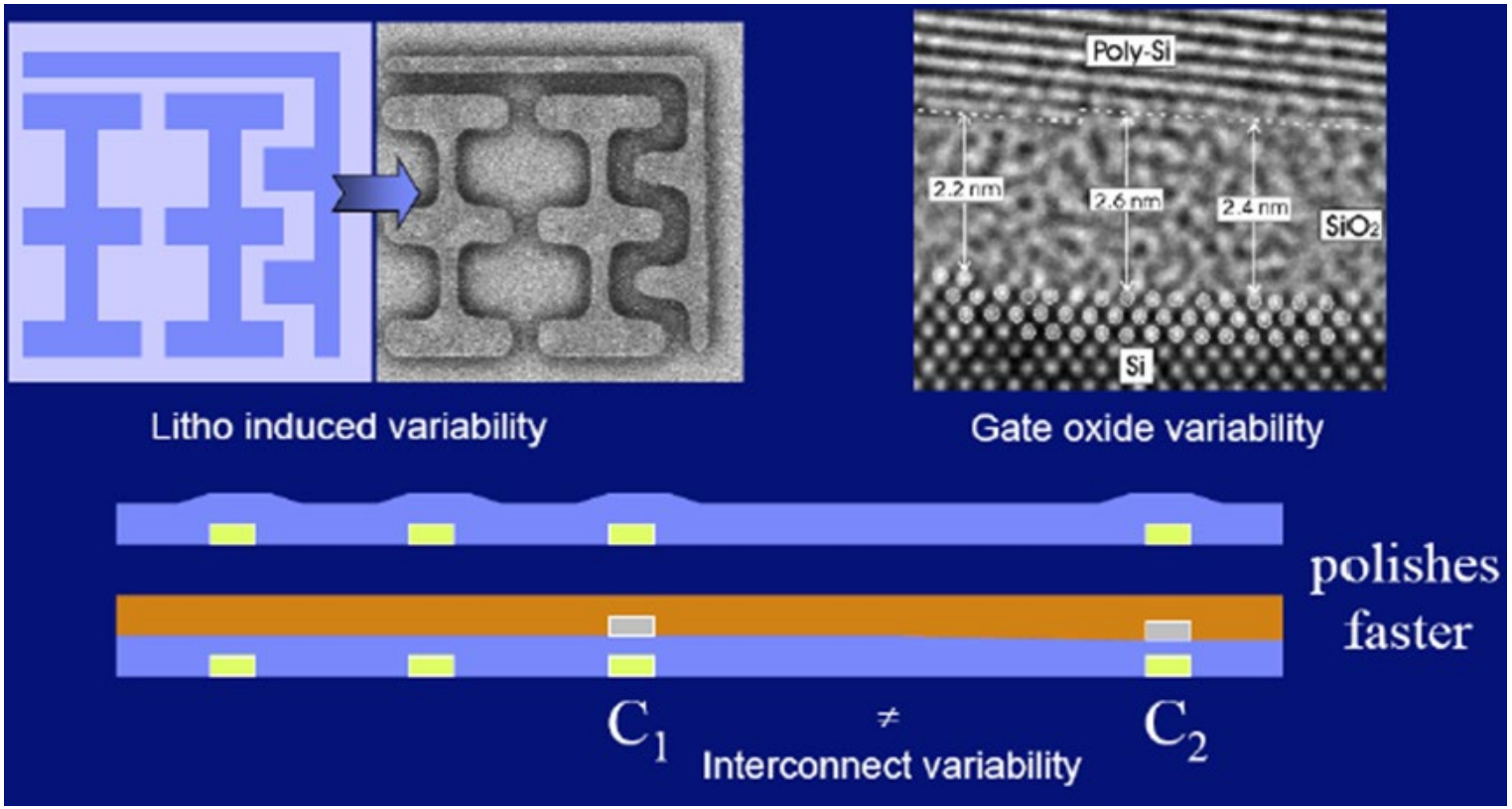


Variability Time Scale

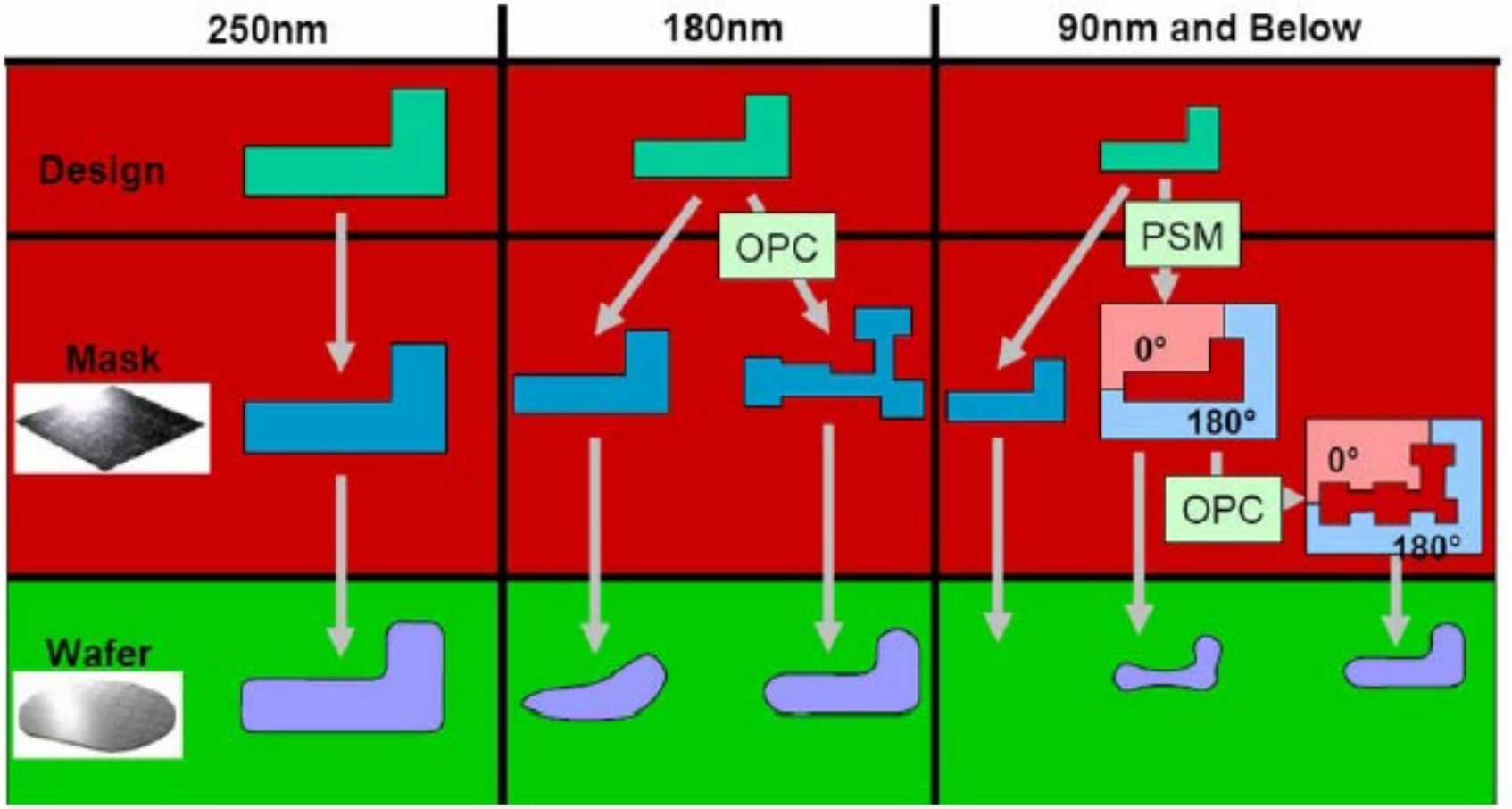


Is Variability for Real?

- Variability ≠ Statisitcis
- Most of the variability is systematic
- The key question is how much is known at design time!!!



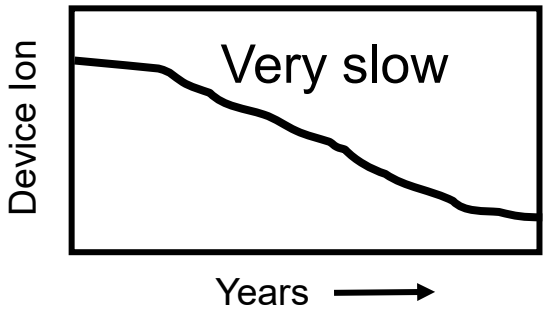
Achieving Sub-Wavelength Resolution



P, V, T Variations

Process

- Die-to-die variation
- Within-die variation
- Static for each die



Time dependent

Degradation

Aging

NBTI

Voltage

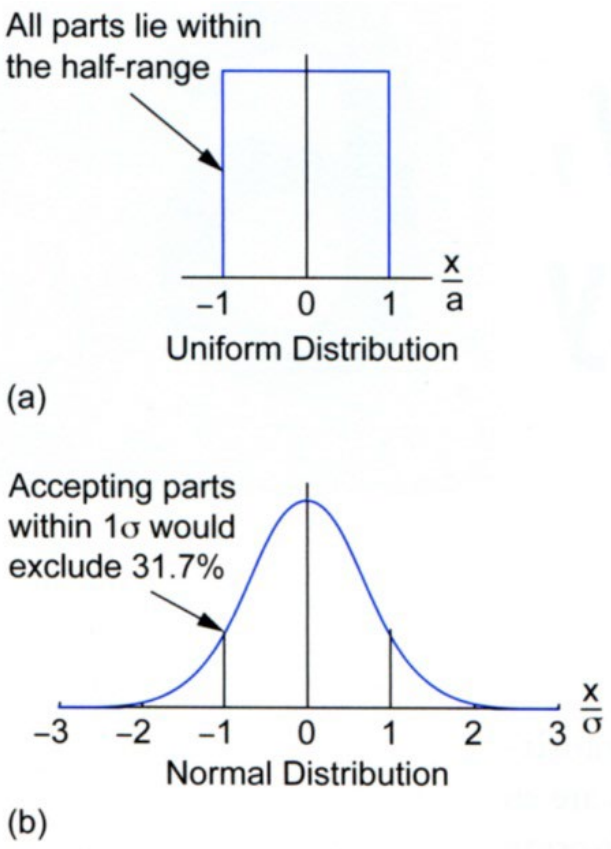
- Chip activity change
- Current delivery—RLC
- Dynamic: ns to 10-100us
- Within-die variation

Temperature

- Activity & ambient change
- Dynamic: 100-1000us
- Within-die variation

PVT Variation

- Three sources of variation: two environmental and one manufacturing
  - Process (P) variation
  - Supply voltage (V)
  - Operating temperature (T)
- Variation modeling
  - Uniform distribution
  - Normal distribution
    - 2~3σ for commercial CMOS
    - 5~7 σ for memory



Sources of Variability

Process	Circuit Operation	Simulation Tools
Channel Length	Temperature	Timing Analysis
Channel Width	Supply Voltage	RC Extraction
Threshold Voltage	Aging (NBTI)	Cell Modeling I-V Curves
Overlap Capacitance	Cross-Coupling Capacitance	Circuit Simulations
Nesting Effects	Multiple Input Switching	Process Files
Interconnect		Transistor Models

Process Variation

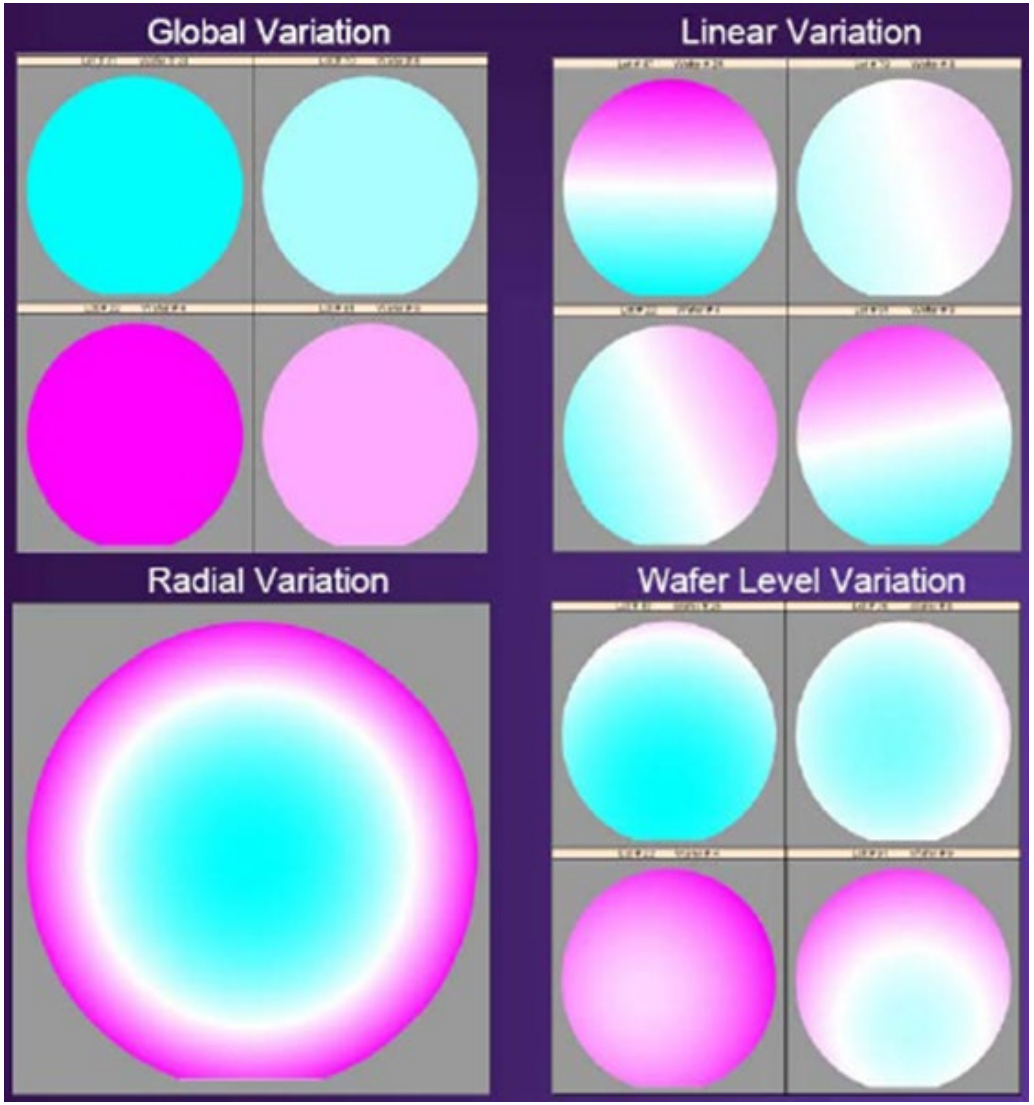
- **Control of minimum features does not track feature scaling**
  - Relative device/interconnect variations increase
- **Sources :**
  - Random dopant fluctuations
  - Feature size, oxide thickness variations
- **Effects:**
  - Speed
  - Power, primary leakage
  - Yield

Process Variation

- For devices
  - Channel length (L)
    - Optics or etching variation
  - Threshold voltage (Vth)
    - Doping variation
- For interconnect
  - Line width and spacing
  - Metal and dielectric thickness
  - Contact resistance

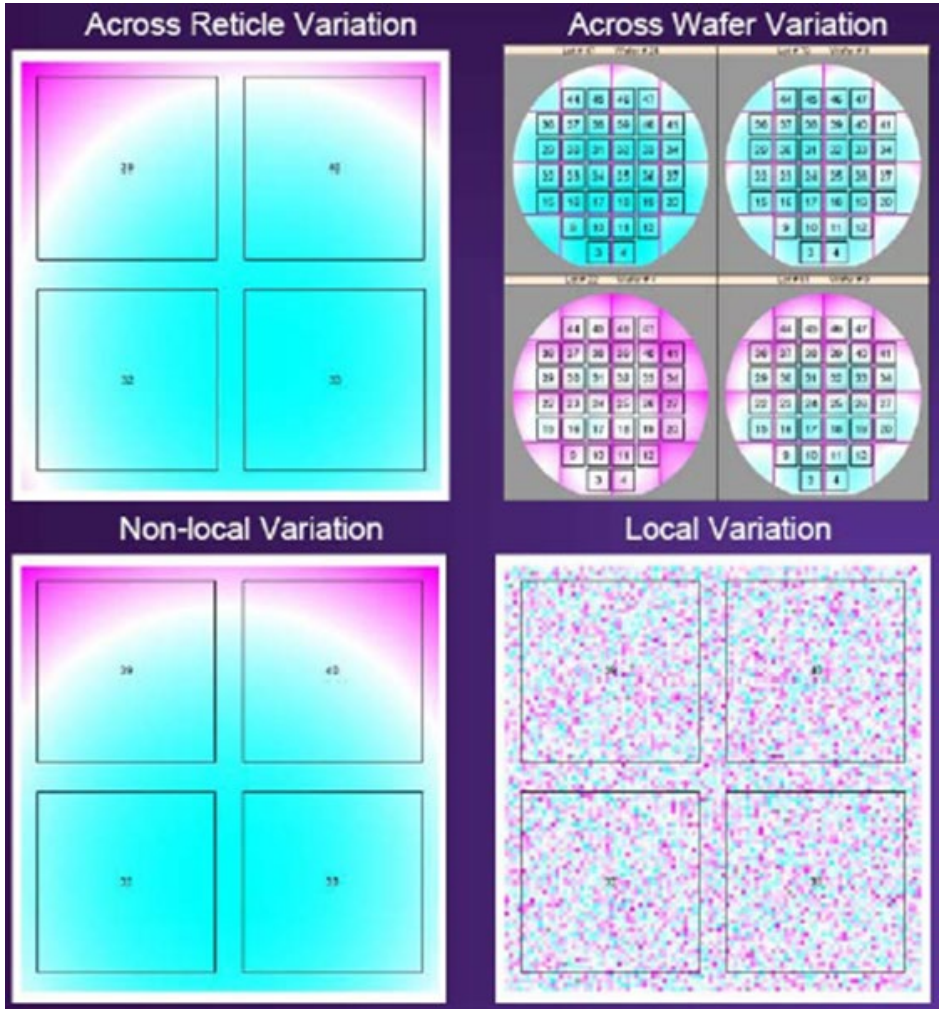
Variation Component (Wafer)

- Global variation comes from Fab, Lot, Wafer processes
- Linear variation is due to materials and gas flow
- Radial variation is due to thermal and spin process
- Wafer level variation is the sum of global, linear, and radial variation
- Affects mainly single-ended circuit performance measures like switching speed, gain, dynamic power etc.



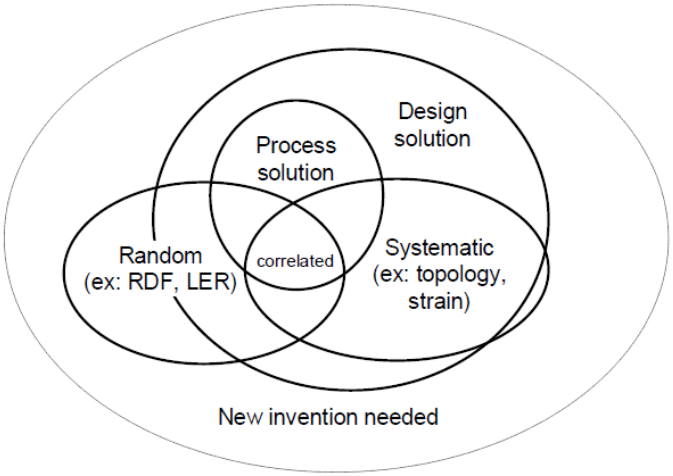
Variation Components (Reticle, Local)

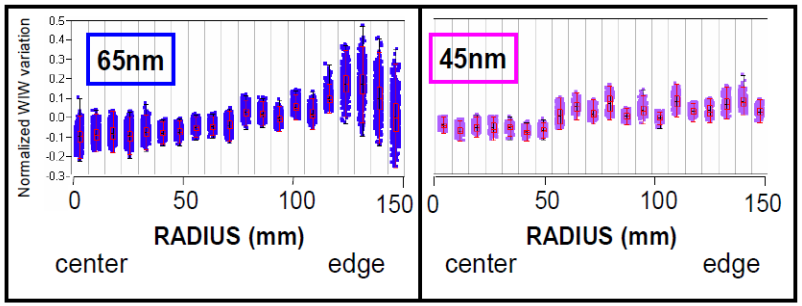
- Reticle variation is due to optical process
- Local Variation comes from totally random microscopic processes. It affects mainly differential circuits performance measures like differential amplifier offset voltage, current mirrors, DACs, etc.
- Becoming important for digital design.

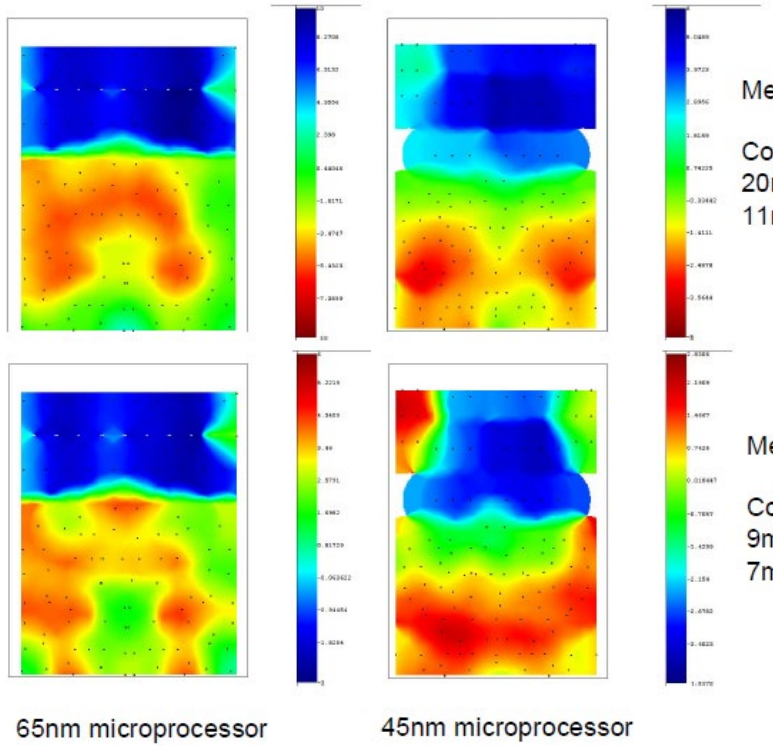


Increasing Process Variation

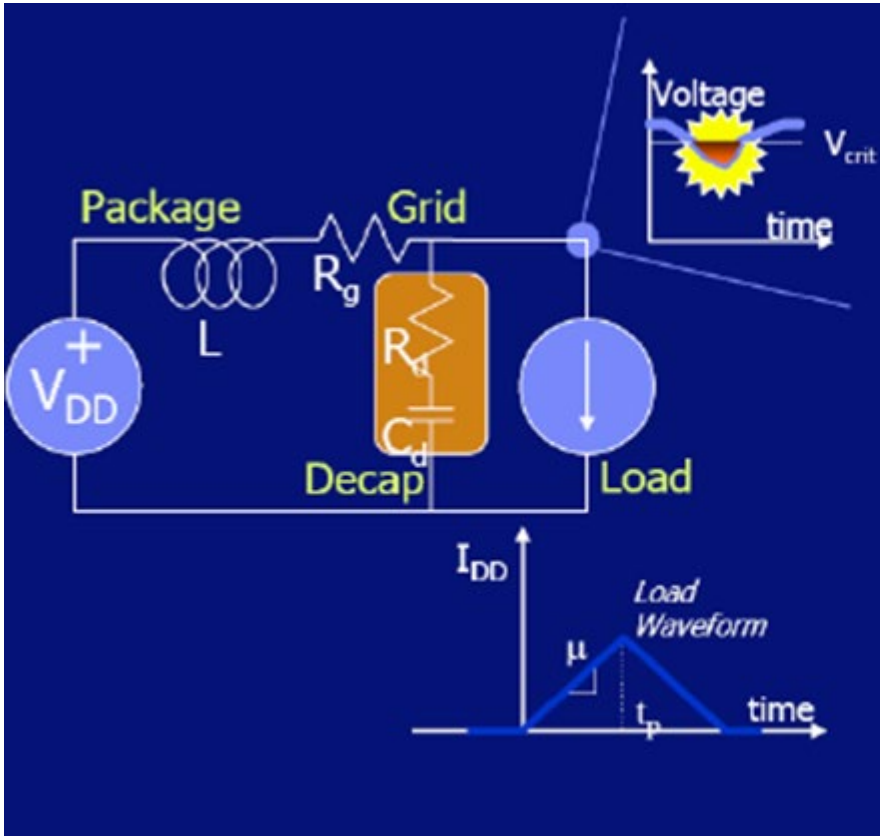
- With-In-Wafer (WIW) variation
- With-IN-Die (WID)

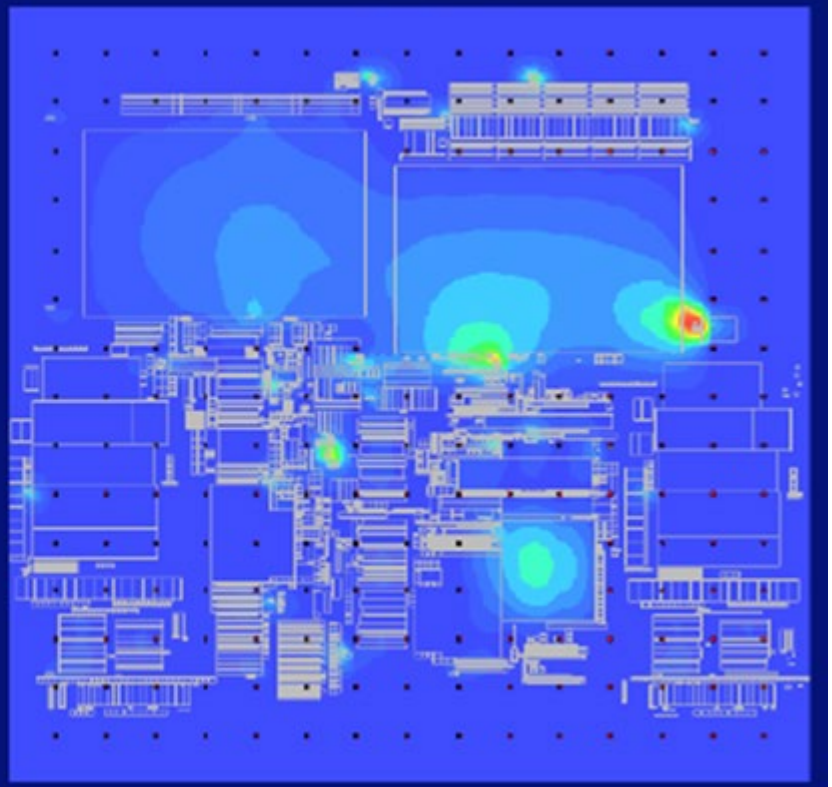






Environmental Variation: Power Supply

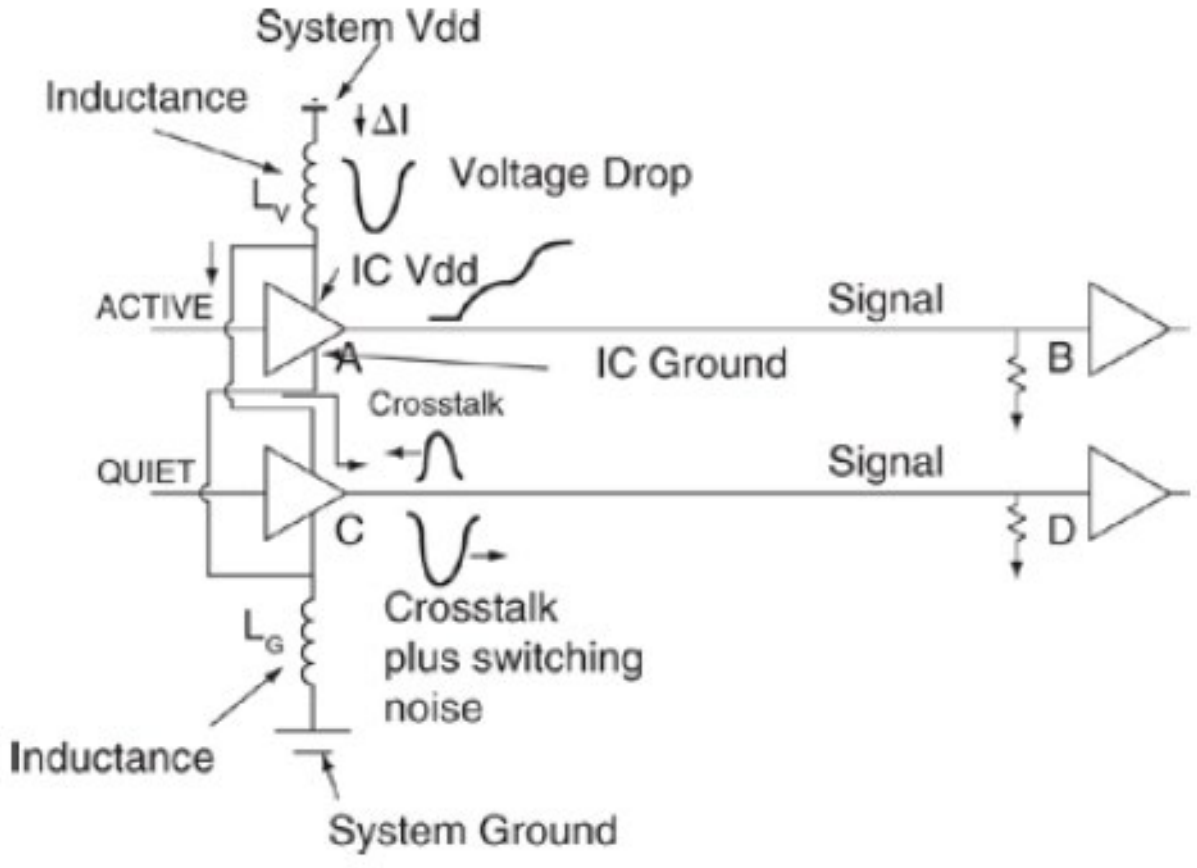




$$\text{VDD Noise} \approx \underbrace{\mu\, t_p\, R_g}_{\text{DC}} + \underbrace{\mu L}_{\text{Package}} + \underbrace{\mu\, R^2_g\, C_d\,(1 - e^{-t_p/\tau})}_{\text{Decap}} \sim \text{Same}$$

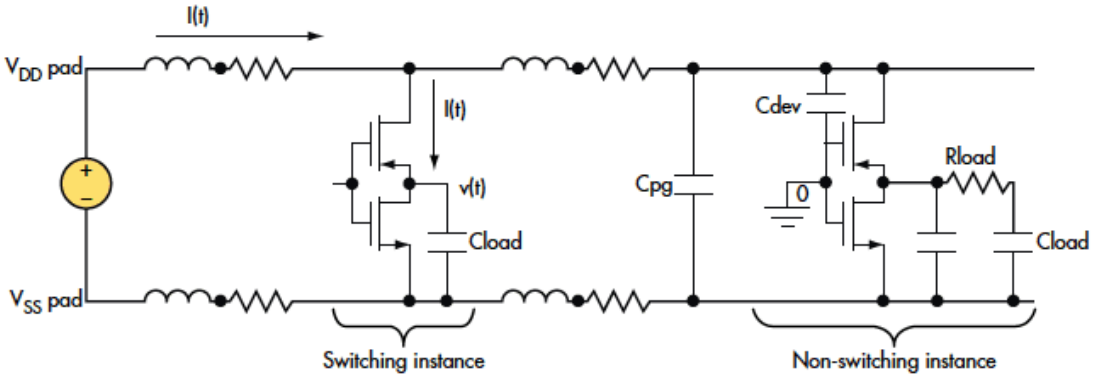
Power Supply Noises

- Delta I noise
- Simultaneous switching noise (SSN)
- IR Drop

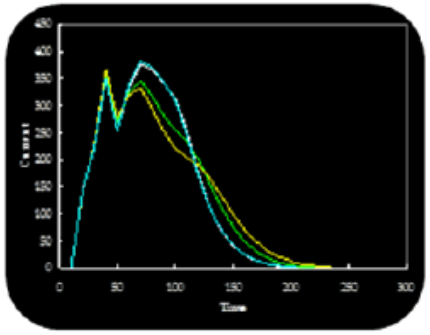


Simultaneous switching noise (SSN)

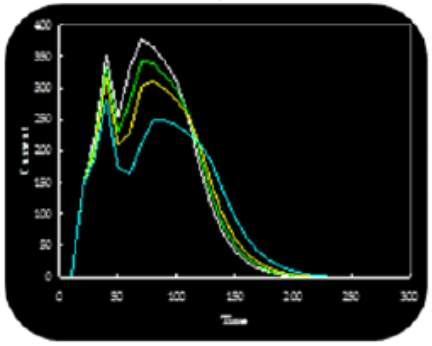
- Time-varying current sources
  - Voltage source
  - Load
  - Input slew for each logic gate



Output: 1:1



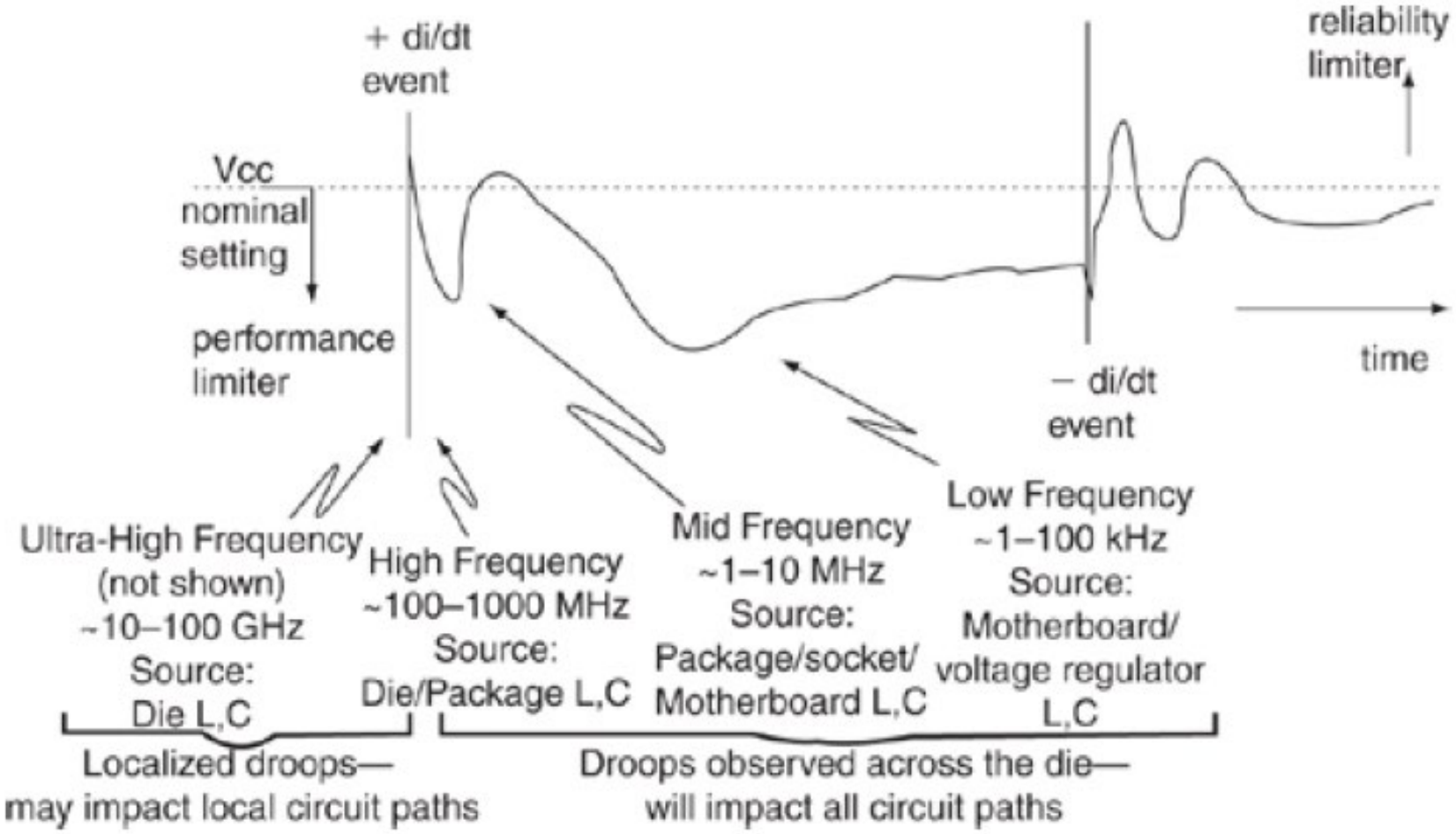
Transistor current versus load



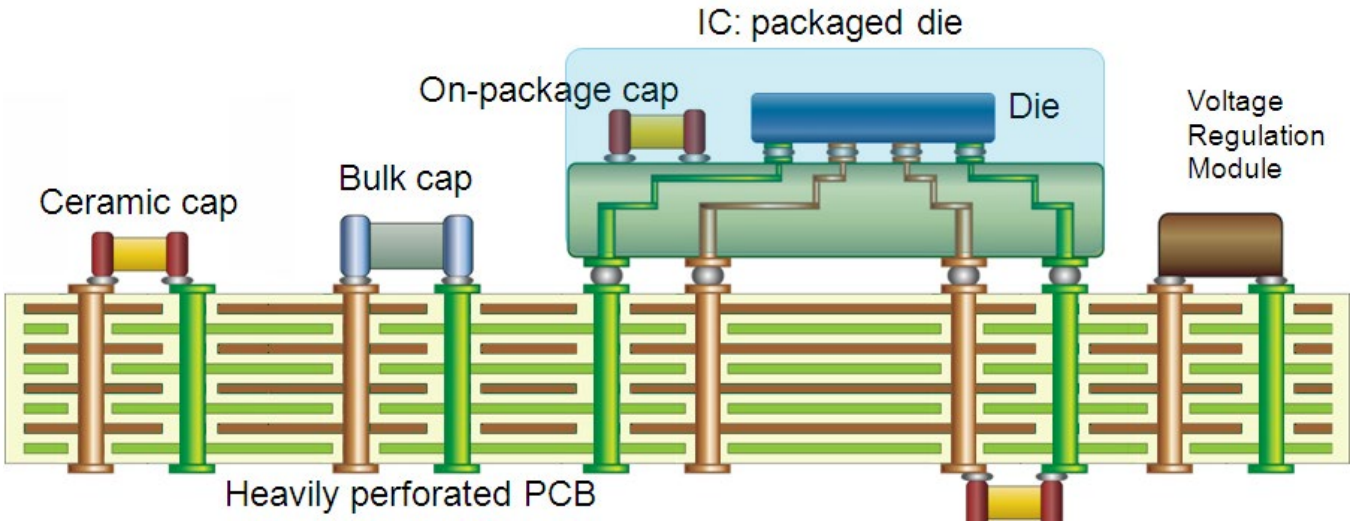
Transistor current versus V_{DD}

Delta I Noise

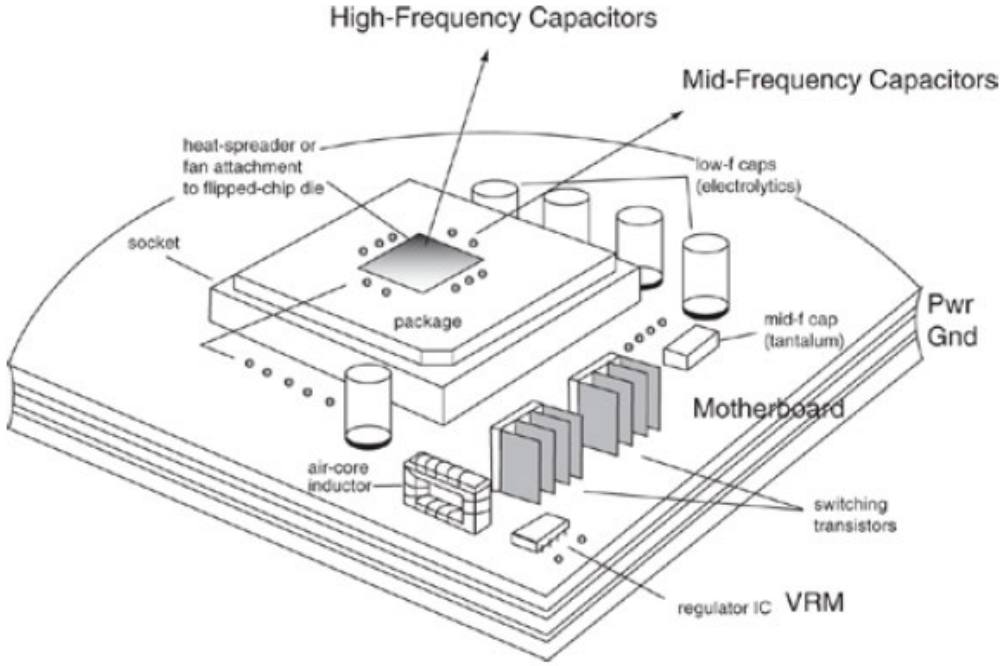
- Different noise frequencies by different inductance



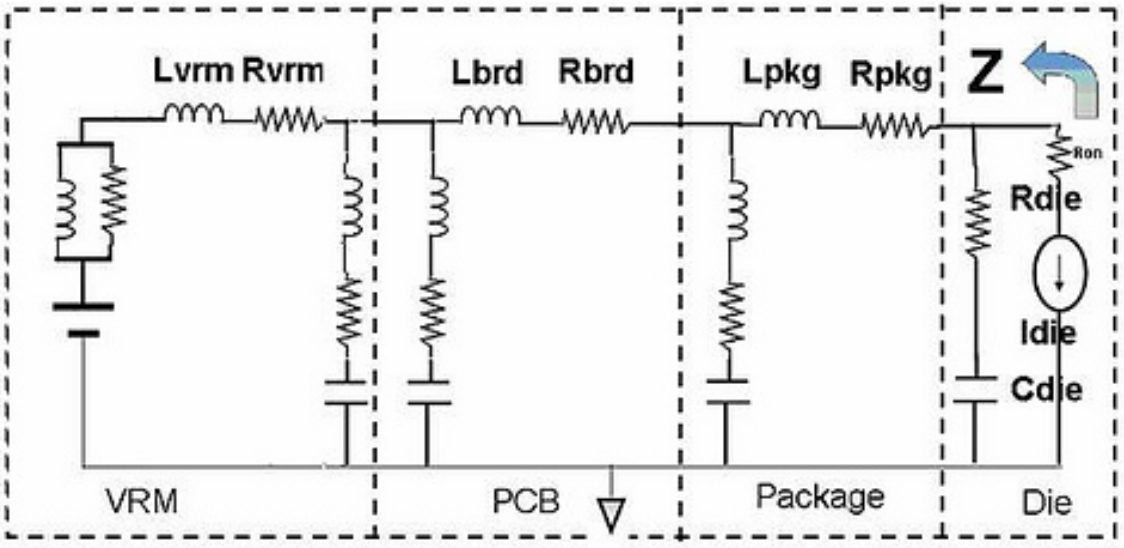
Delta I Noise Suppression

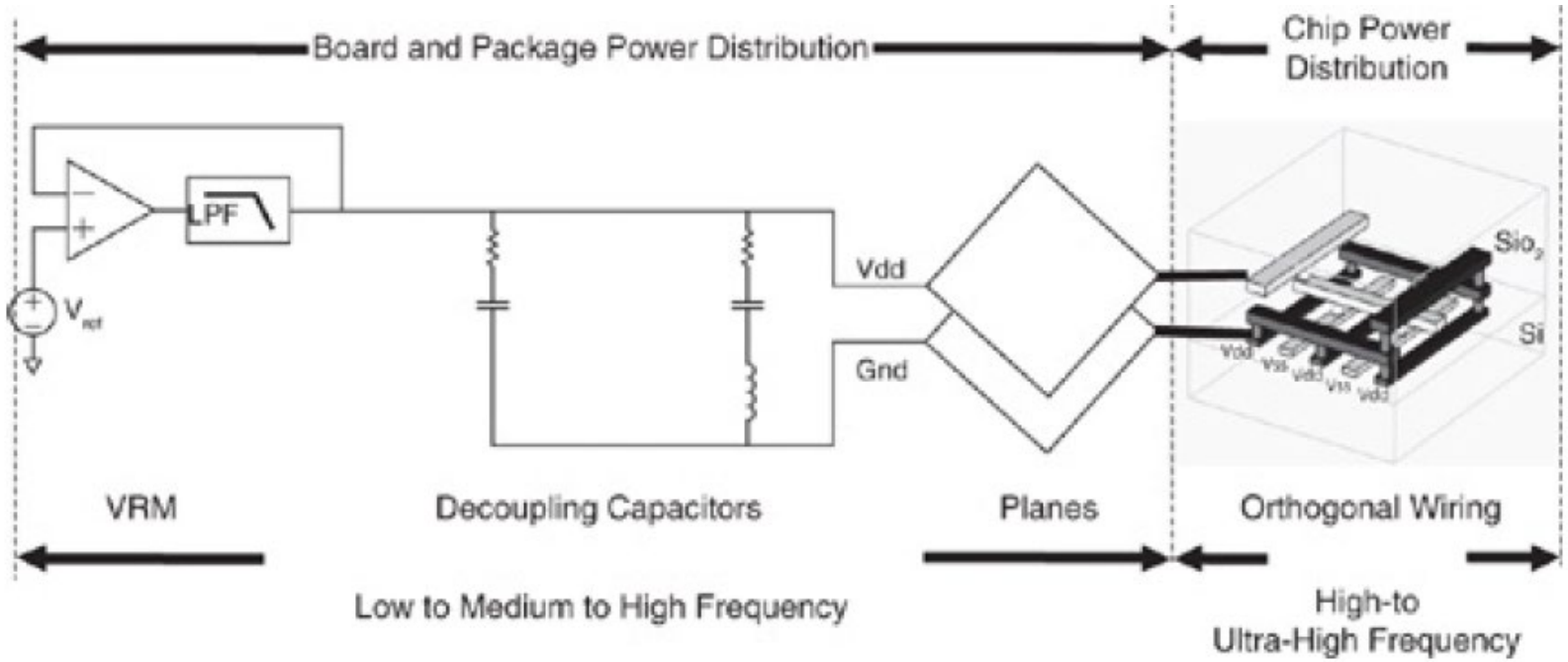


- Smaller Z for 5% voltage drop
- DECAP for noise suppression

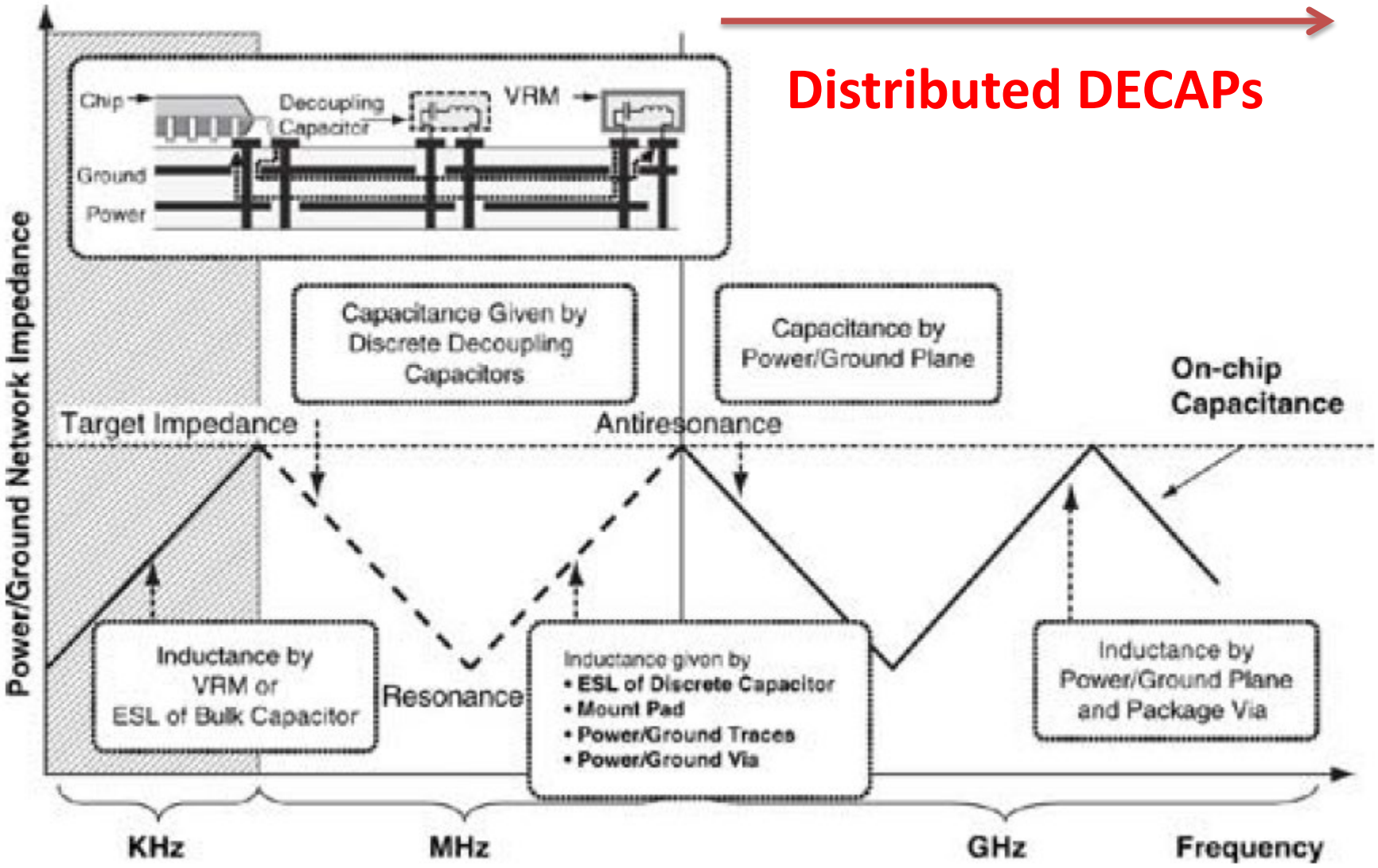


Power Deliver Network



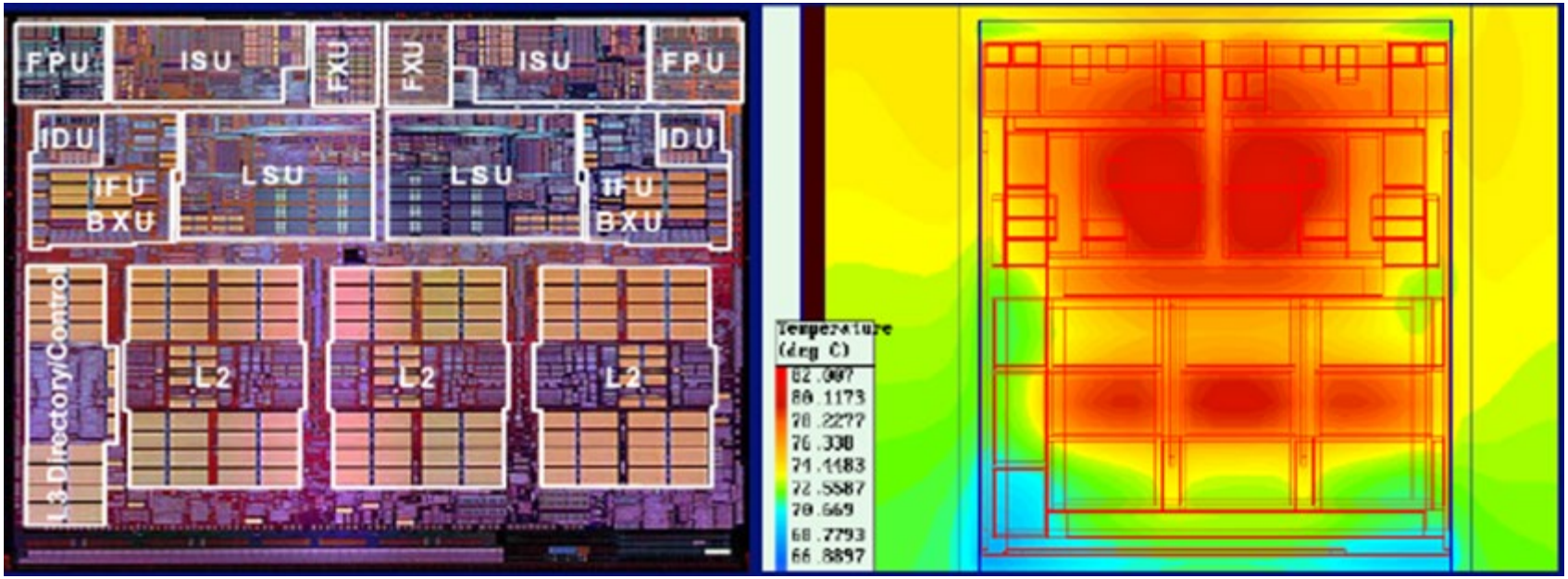


Impendence on Power Network



Environmental Variation: Thermal

- Thermal varies with-in the chip



Chip Floorplan

Chip Thermal Profile

Power 4 Server Chip: 2 CPU on a chip

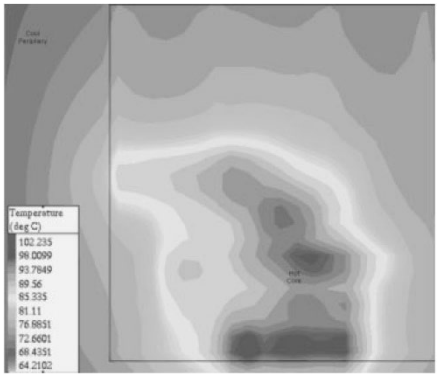
- **The CPUs can be much hotter than the caches**

Temperature Variation

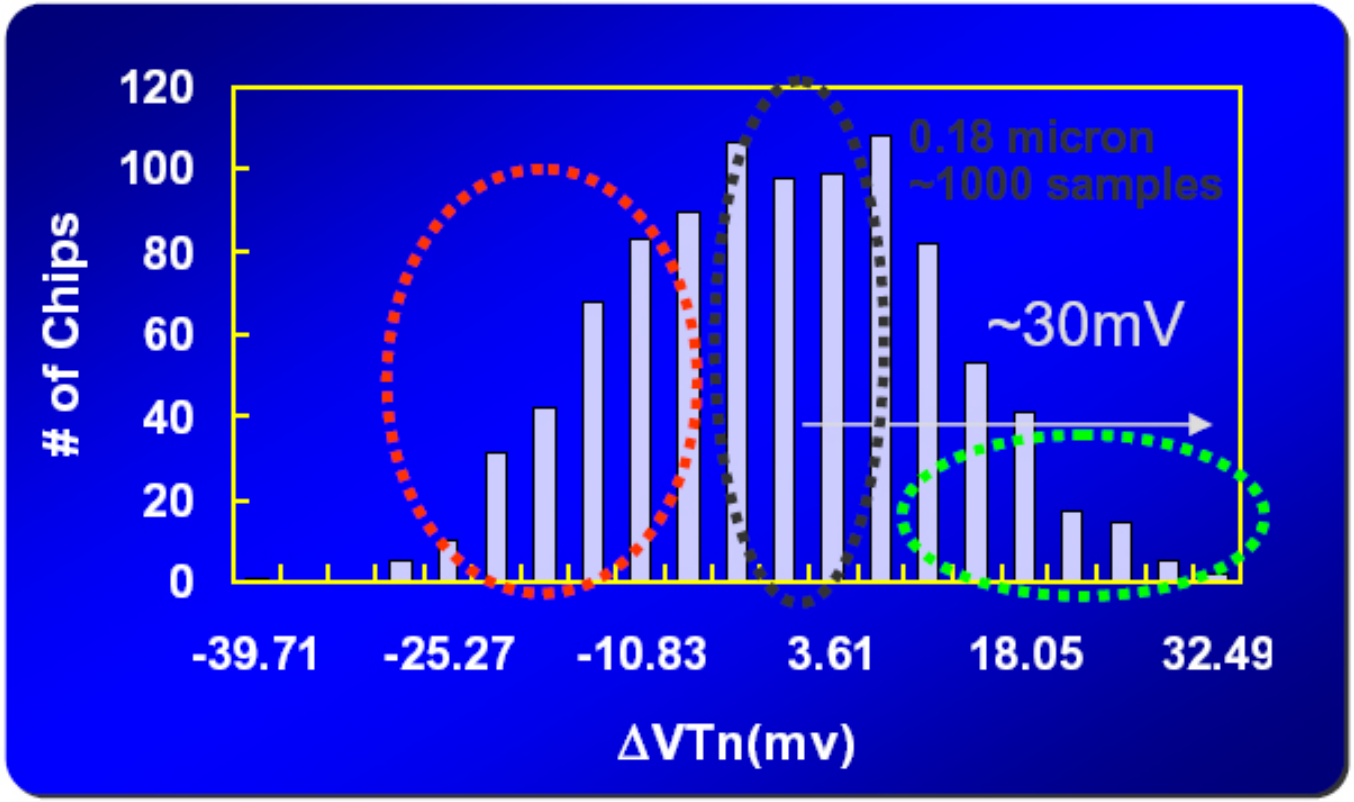
- Temperature
- Ambient temperature range

Standard	Minimum	Maximum
Commercial	0 °C	70 °C
Industrial	−40 °C	85 °C
Military	−55 °C	125 °C

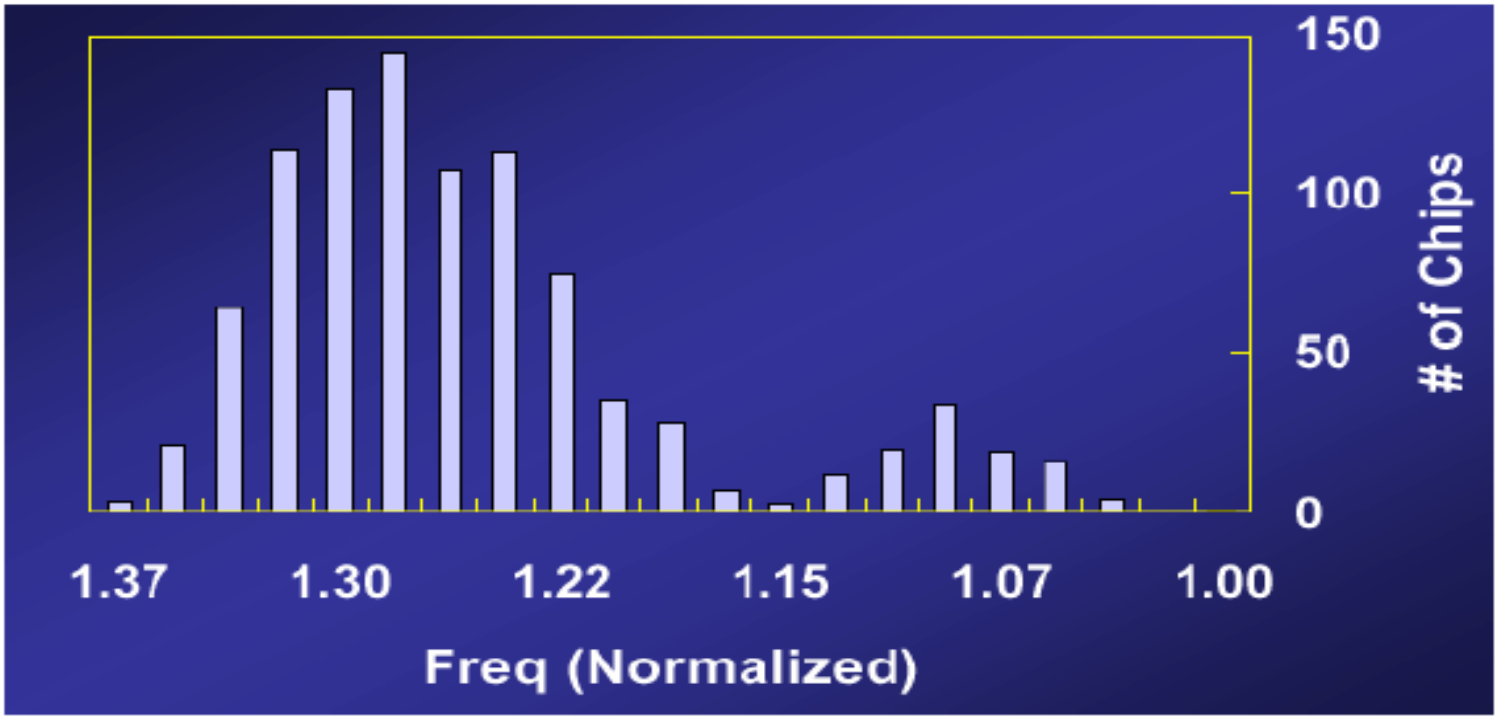
- Variation depending on power density



Vt Distribution

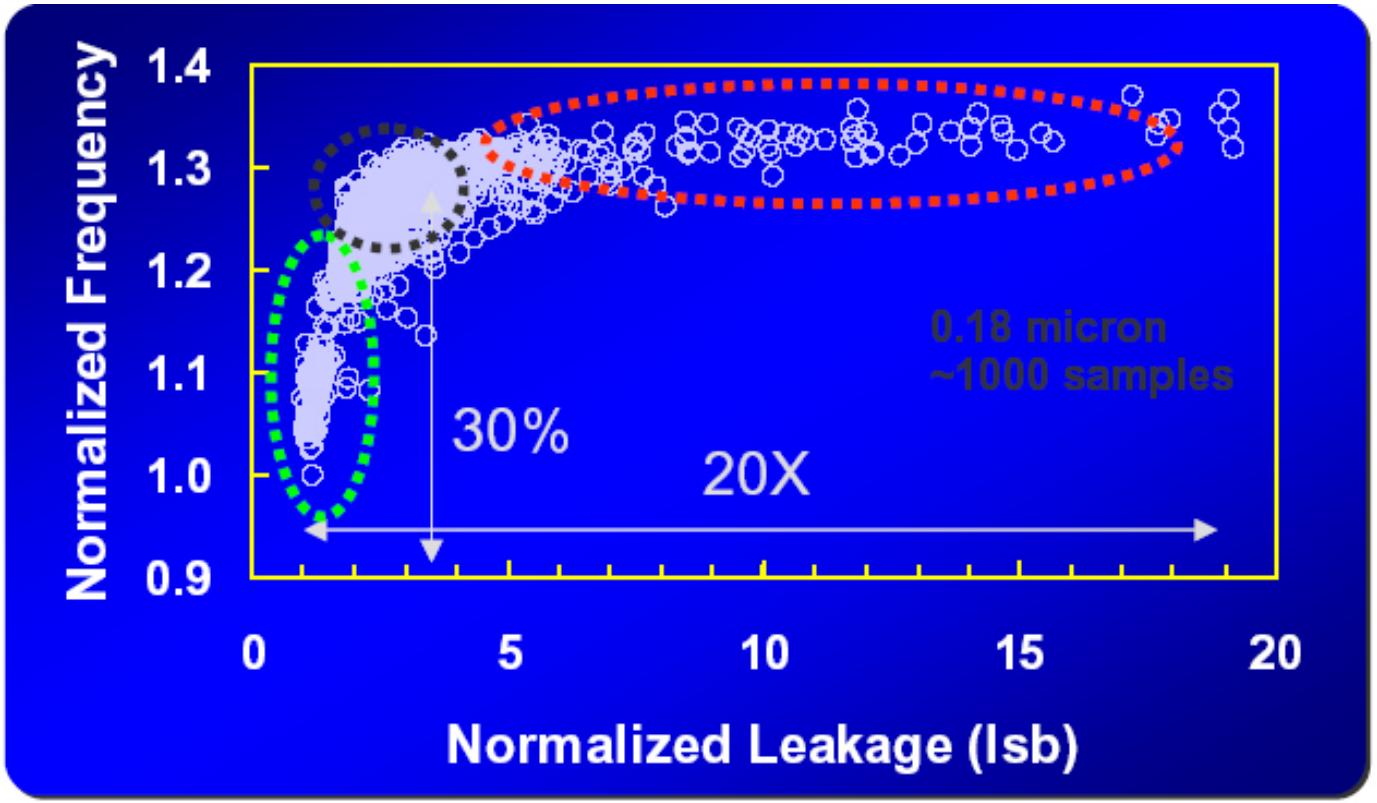


Causes Larger Frequency Distribution



Courtesy Intel

Frequency & SD Leakage



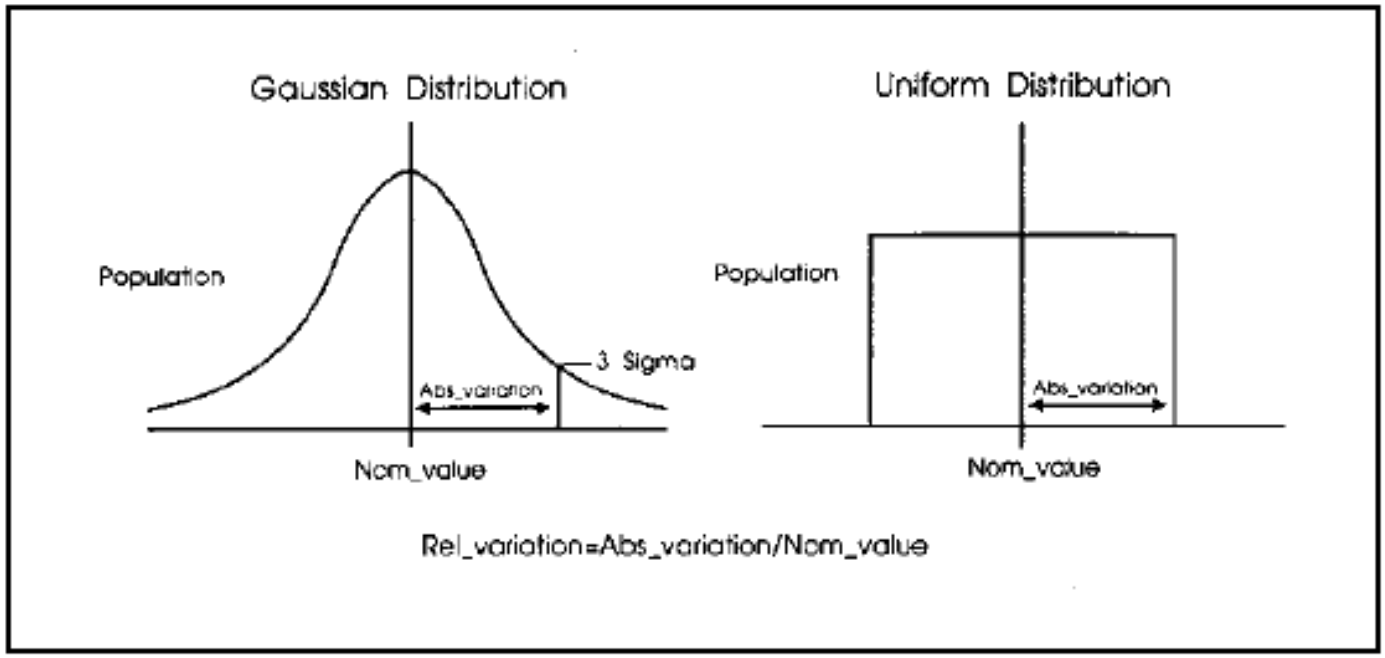
Low Freq
Low Isb

High Freq
Medium Isb

High Freq
High Isb

Monte Carlo Simulation

- Monte Carlo analysis uses a random number generator to create the following types of functions:
  - Gaussian Parameter Distribution
  - Uniform Parameter Distribution
  - Random Limit Parameter Distribution



Corner Cases

- Typical (TT)
- Fast PMOS Fast NMOS (FF)
- Slow PMOS Slow NMOS (SS)
- Fast PMOS Slow NMOS (FPSN)
- Slow PMOS Fast NMOS (SPFN)
- Digital timing analysis
  - Best Case
    - -25 ℃ / 1.1V / FF corner
  - Worst Case
    - 125℃ / 0.9V / SS corner

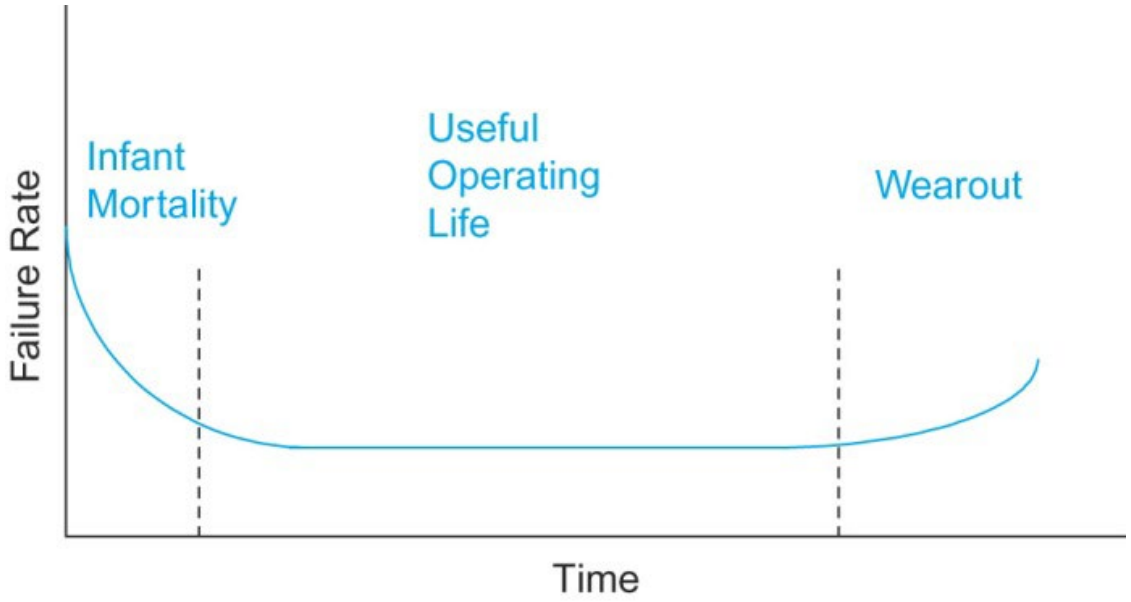
Timing Margins for Multi-Corner Multi-Mode

- The setup and hold times must be analyzed simultaneously for different combinations of library models, voltages, and interconnect (RC) corners.

	Single Core Design			Core + 1 Island				Core + 2 Islands				
	Lib	Core	RC	Lib	Core	Vdd1	RC	Lib	Core	Vdd1	Vdd2	RC
Setup1	Max	1.2	Max	Max	1.2	0.9	Max	Max	1.2	0.9	0.9	Max
Setup2	Max	1.2	Min	Max	1.2	0.9	Min	Max	1.2	0.9	0.9	Min
Hold1	Min	1.8	Min	Min	1.8	1.5	Min	Min	1.8	1.5	1.5	Min
Hold2	Min	1.8	Max	Min	1.8	1.5	Max	Min	1.8	1.5	1.5	Max
Setup1	—	—	—	Max	1.2	0	Max	Max	1.2	0	1.2	Max
Setup2	—	—	—	Max	1.2	0	Min	Max	1.2	0	1.2	Min
Hold1	—	—	—	Min	1.8	0	Min	Min	1.8	0	1.8	Min
Hold2	—	—	—	Min	1.8	0	Max	Min	1.8	0	1.8	Max
Setup1	—	—	—	—	—	—	—	Max	1.2	0.9	1.2	Max
Setup2	—	—	—	—	—	—	—	Max	1.2	0.9	1.2	Min
Hold1	—	—	—	—	—	—	—	Min	1.8	1.5	1.8	Min
Hold2	—	—	—	—	—	—	—	Min	1.8	1.5	1.8	Max
Setup1	—	—	—	—	—	—	—	Max	1.2	0	0.9	Max
Setup2	—	—	—	—	—	—	—	Max	1.2	0	0.9	Min
Hold1	—	—	—	—	—	—	—	Min	1.8	0	1.5	Min
Hold2	—	—	—	—	—	—	—	Min	1.8	0	1.5	Max

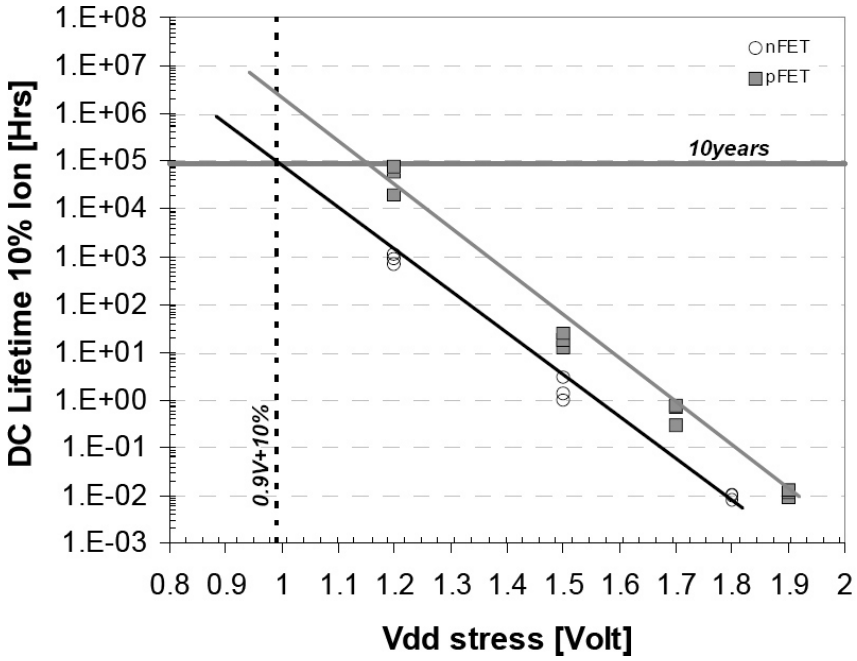
Reliability

- Characterizing reliability
  - Mean time between failures (MTBF)
    - # of devices x hours of operation / number of failures
  - Failures in time (FIT)
    - # of failures / thousand hours / million devices



Accelerated Lifetime Testing

- Expected reliability typically exceeds 10 years
- But products come to market in 1-2 years
- Accelerated lifetime testing required to predict adequate long-term reliability
  - Wear out display exponential relationship to V / T



For gate oxide

Reliability

- Hard errors caused by:
  - Electromigration, depending on current density J
  - Self-heating, limiting RMS J in bi-directional lines
  - Hot carriers, injected into the gate oxide
  - Latchup, low-resistance between VDD and GND
  - Overvoltage failure, from electrostatic discharge (ESD), oxide breakdown, punchthrough
- Soft errors:
  - cause systems to crash or lose data, often found in memory devices (in DRAM)

Hard Errors

- Fail permanently
- Oxide wearout
  - Hot carriers
  - Negative bias temperature instability
  - Time-dependent dielectric breakdown
- Interconnect wearout
  - Electromigration
  - Self-heating

Hot Carriers

- Electric fields across channel impart high energies to some carriers
  - These "hot" carriers may be blasted into the gate oxide where they become trapped
  - Accumulation of charge in oxide **causes shift in V_t over time**
  - Eventually V_t shifts too far for devices to operate correctly
- **Choose V_{DD}** to achieve reasonable product lifetime
  - Worst problems for inverters and NORs with slow input risetime and long propagation delays

NBTI

- *Negative bias temperature instability*
- Electric field applied across oxide forms dangling bonds called traps at Si-SiO_2 interface
- Accumulation of traps causes V_t shift
- Most pronounced for pMOS transistors with strong negative bias ($V_g = 0$, $V_s = V_{DD}$) at high temperature

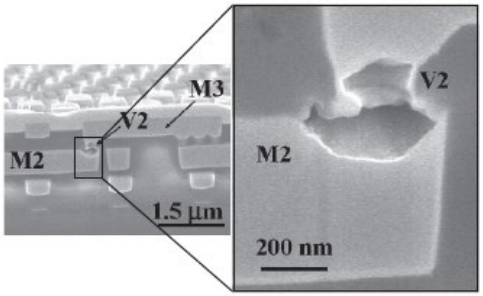
$$\Delta V_t = k e^{\frac{E_{ox}}{E_0}} t^{0.25} \qquad E_{ox} = V_{DD}/t_{ox}$$

TDDB

- *Time-dependent dielectric breakdown*
  - Gradual increase in gate leakage when an electric field is applied across an oxide
  - a.k.a *stress-induced leakage current*
- For 10-year life at 125 C, keep E_{ox} below ~0.7 V/nm

Electromigration

- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density J_{dc} (current / area)
  - Exponential dependence on temperature
  - Black's Equation: $$MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^{\ n}}$$
  - Typical limits: $J_{dc} < 1 - 2$ mA / μm^2



[Christiansen06]

Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability

$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 dt}{T}}$$

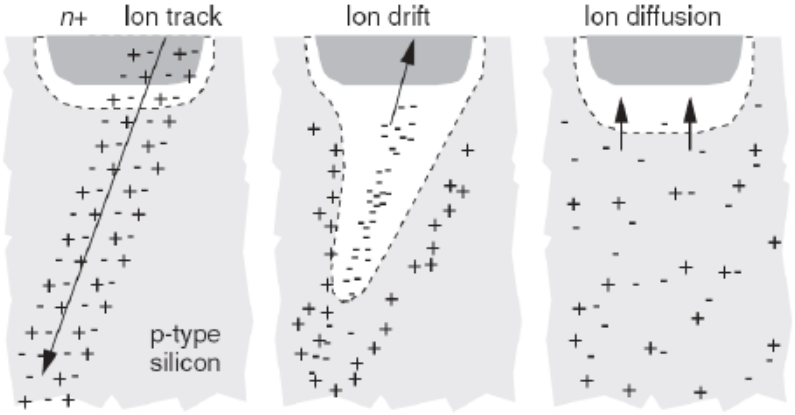
  - Typical limits: $J_{rms} < 15$ mA / μm^2

Overvoltage Failure

- High voltages can blow out tiny transistors
- *Electrostatic discharge* (ESD)
  - kilovolts from static electricity when the package pins are handled
- *Oxide breakdown*
  - In a 65 nm process, $V_g \approx 3$ V causes *arcing* through thin gate oxides
- *Punchthrough*
  - High V_{ds} causes depletion region between source and drain to touch, leading to high current flow and destructive overheating

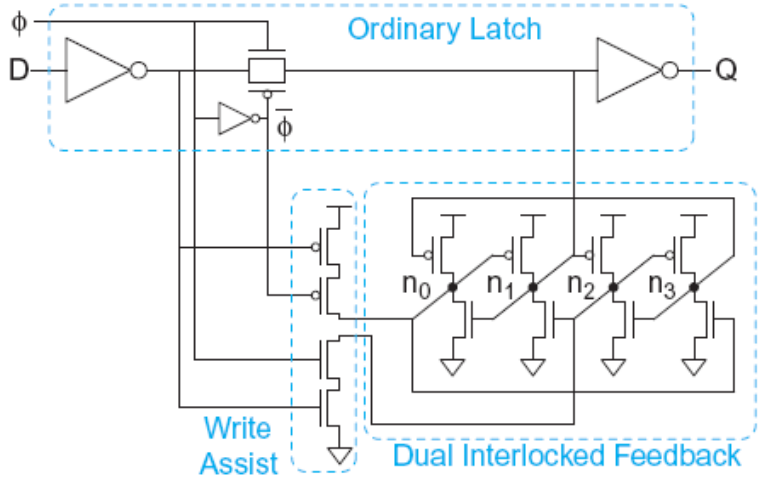
Soft Errors

- In 1970's, DRAMs were observed to randomly flip bits
  - Ultimately linked to alpha particles and cosmic ray neutrons
- Collisions with atoms create electron-hole pairs in substrate
  - These carriers are collected on p-n junctions, disturbing the voltage



Radiation Hardening

- Radiation hardening reduces soft errors
  - Increase node capacitance to minimize impact of collected charge
  - Or use redundancy
  - E.g. *dual-interlocked cell*



- Error-correcting codes
  - Correct for soft errors that do occur