Digital IC Design

Lec 4-2:

Combinational Circuits – Logic Families

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Logic Family

- **Static CMOS**
  - Complementary CMOS logic
  - **Pass Transistor Logic**
  - **Ratioed circuits**
    - **Pseudo-nMOS Logic**
  - **CVSL (Cascode voltage switch logic)**
- Dynamic Logic

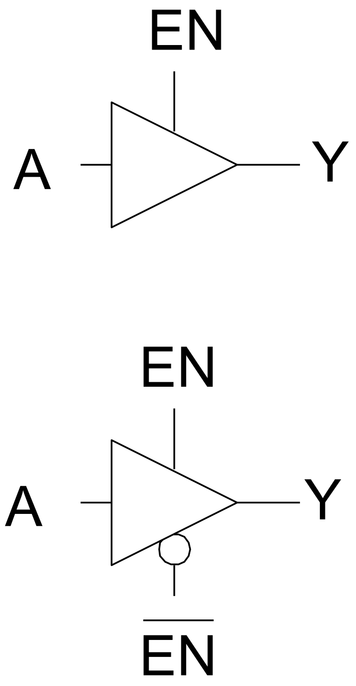
Review of Static CMOS

- Number of transistor of a logic is ***2N*** where N is number of inputs
- Capacitance loading of each input is the gate capacitance of one PMOS and one NMOS
- ***No DC*** current if there is no logic change
- ***Rail-to-rail voltage swing, restoring and ratioless design***
- Most ***robust*** logic style and used in standard cell

Tristates

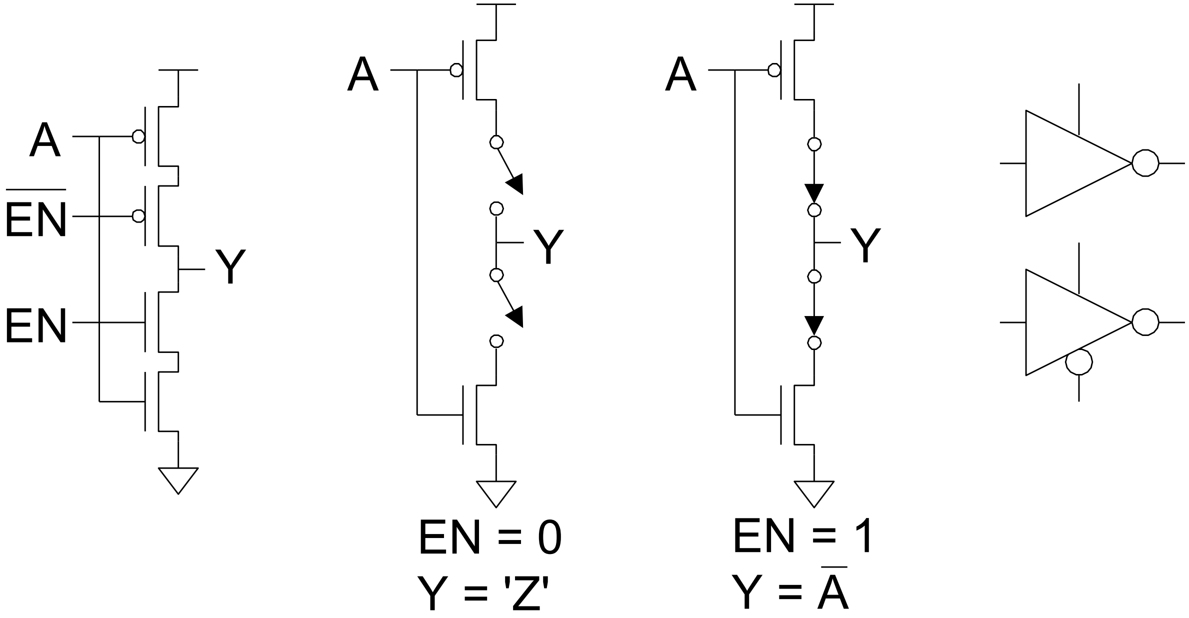
- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



Tristate Inverter

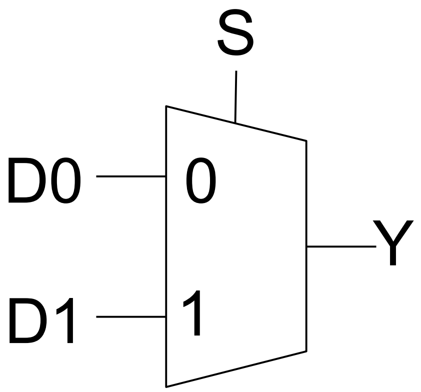
- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output



Multiplexers

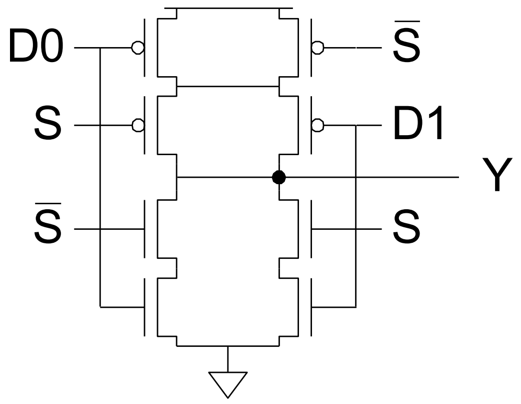
- 2:1 multiplexer chooses between two inputs

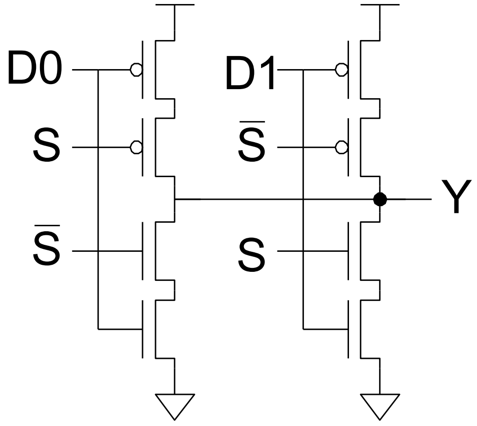
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

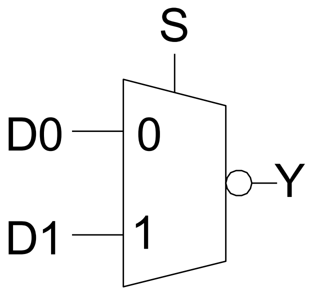


Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter

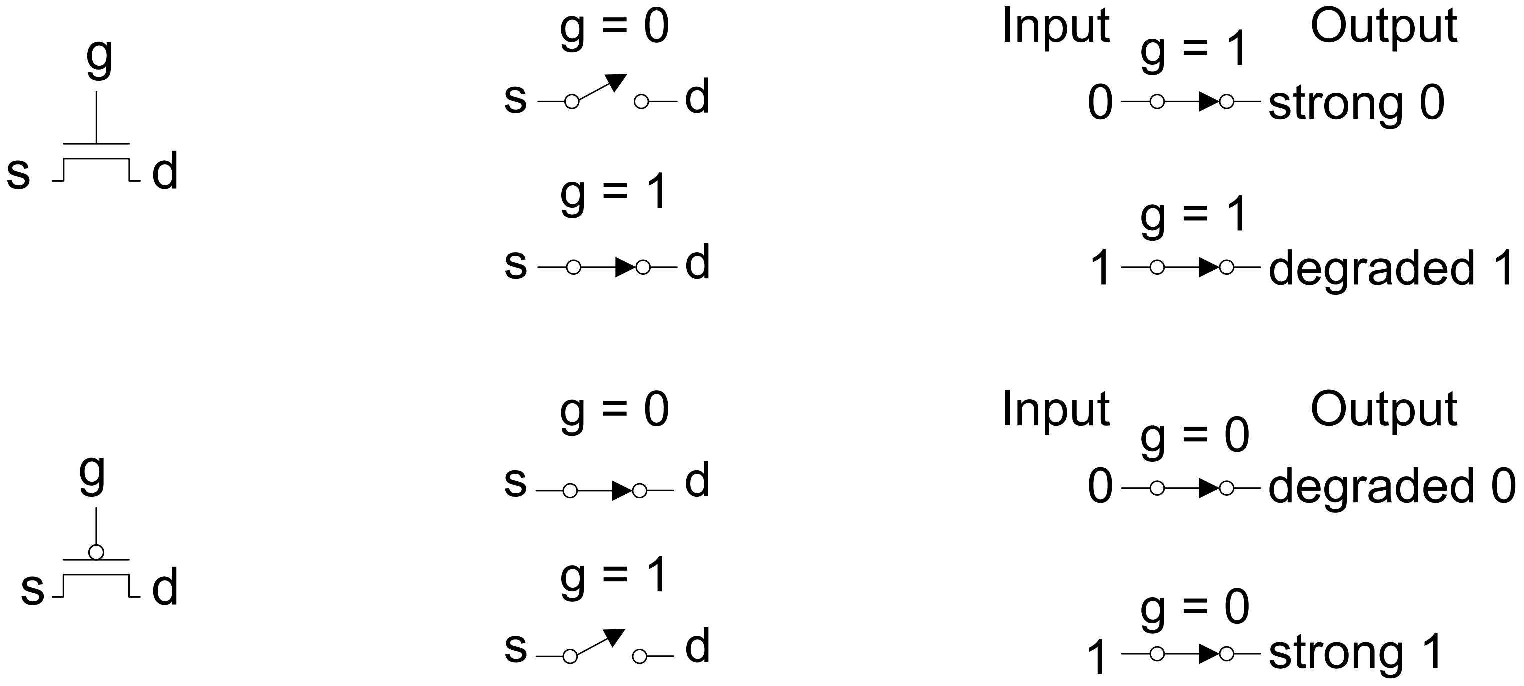






Pass Transistors

- Transistors can be used as switches



g
s d

g = 0
s d

g = 1
s d

Input g = 1 Output
0 strong 0

g = 1
1 degraded 1

g
s d

g = 0
s d

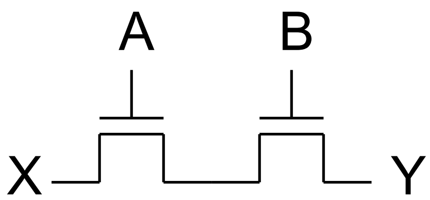
g = 1
s d

Input g = 0 Output
0 degraded 0

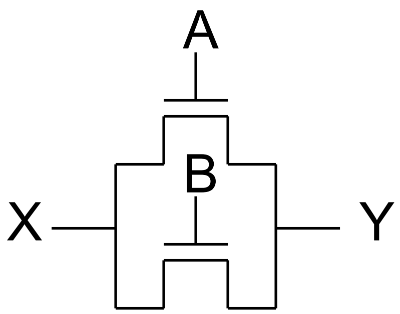
g = 0
1 strong 1

NMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



X = Y if A and B

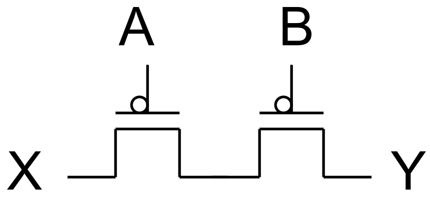


X = Y if A or B

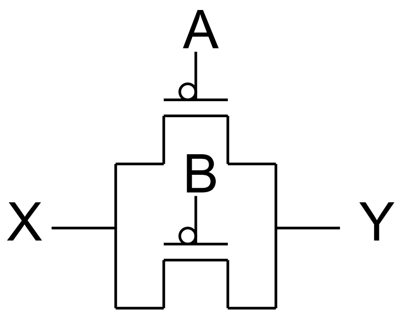
- Remember - NMOS transistors pass a strong 0 but a weak 1

PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low



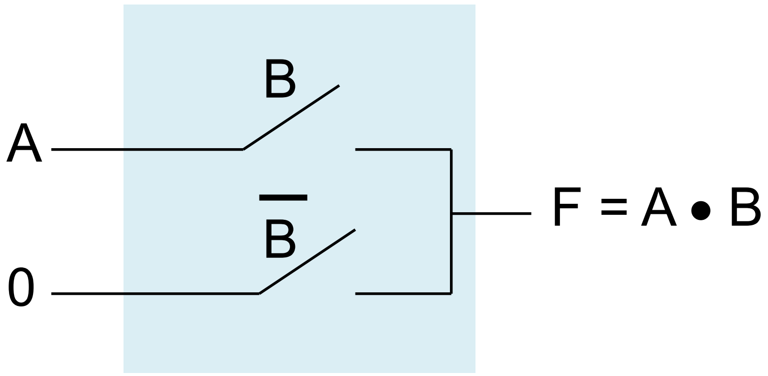
X = Y if $\overline{A}$ and $\overline{B}$ = $\overline{A + B}$

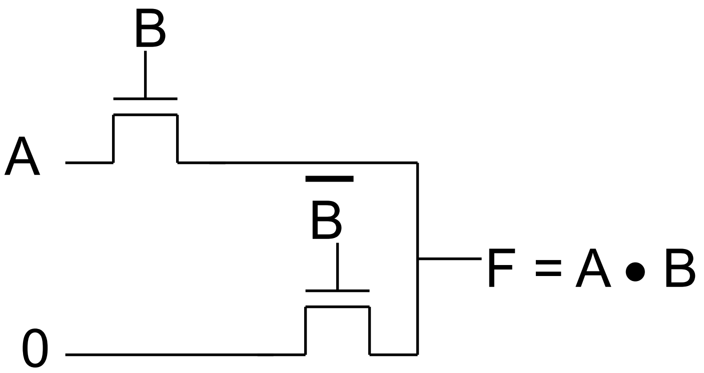


X = Y if $\overline{A}$ or $\overline{B}$ = $\overline{A \bullet B}$

- Remember - PMOS transistors pass a strong 1 but a weak 0

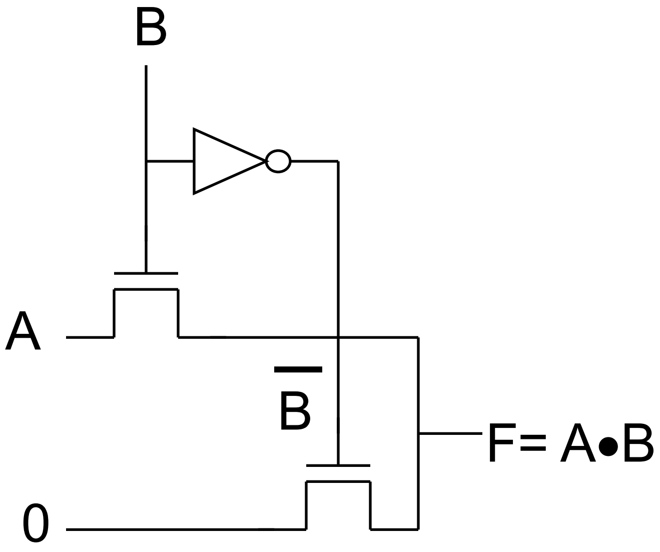
Pass Transistor (PT) Logic

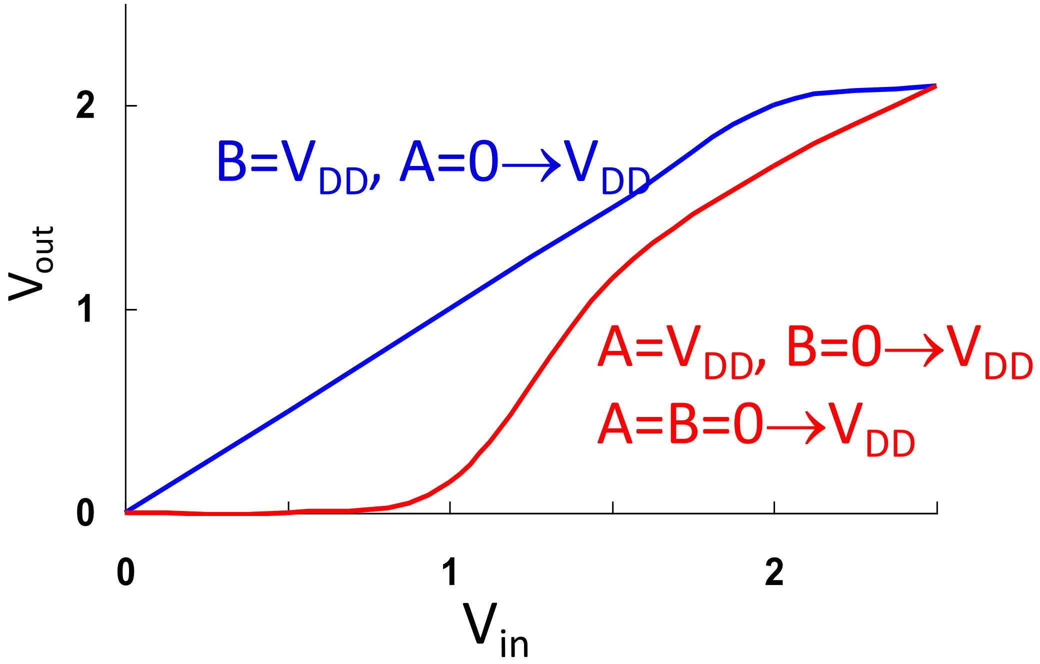




- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

VTC of Pass Transistor AND Gate

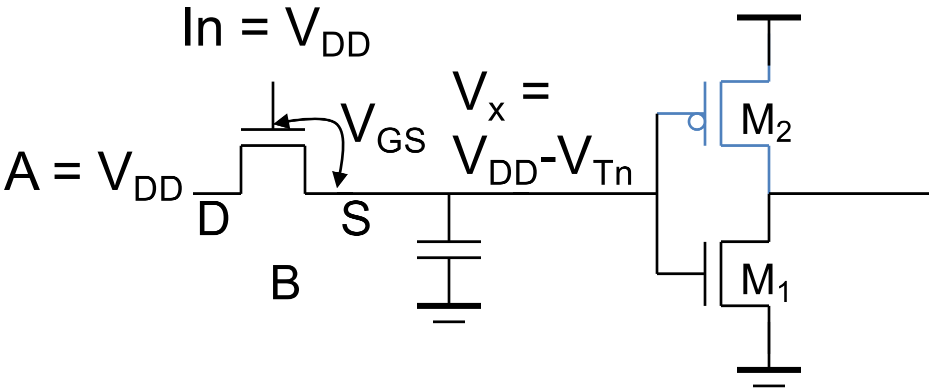




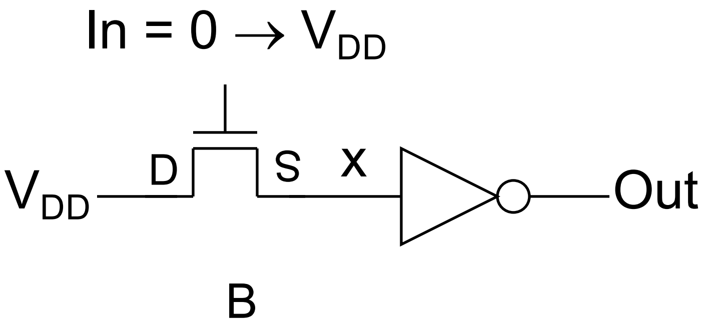
- Pure PT logic is not **regenerative** - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

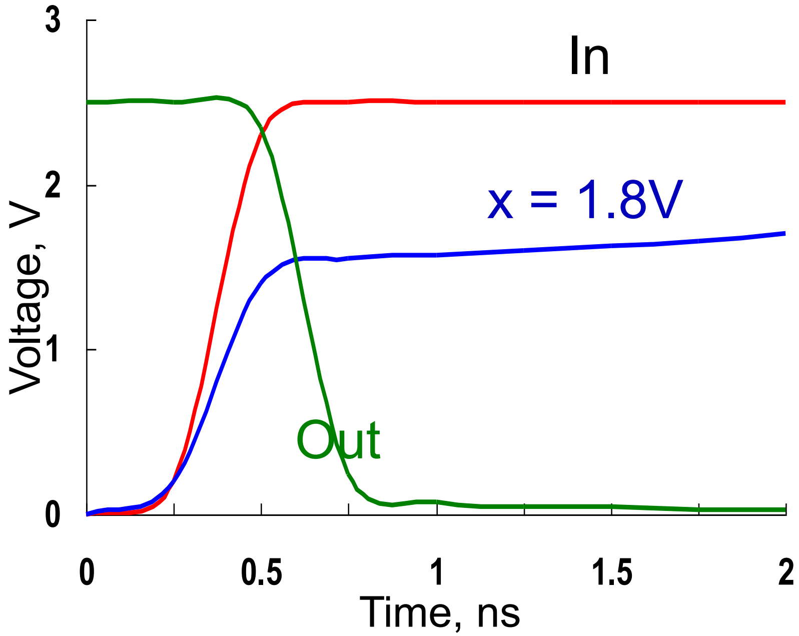
NMOS Only PT Driving an Inverter

- V_x does not pull up to V_{DD}, but $V_{DD} – V_{Tn}$
  - Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
  - Notice V_{Tn} increases for pass transistor due to body effect (V_{SB})



Voltage Swing of PT Driving an Inverter

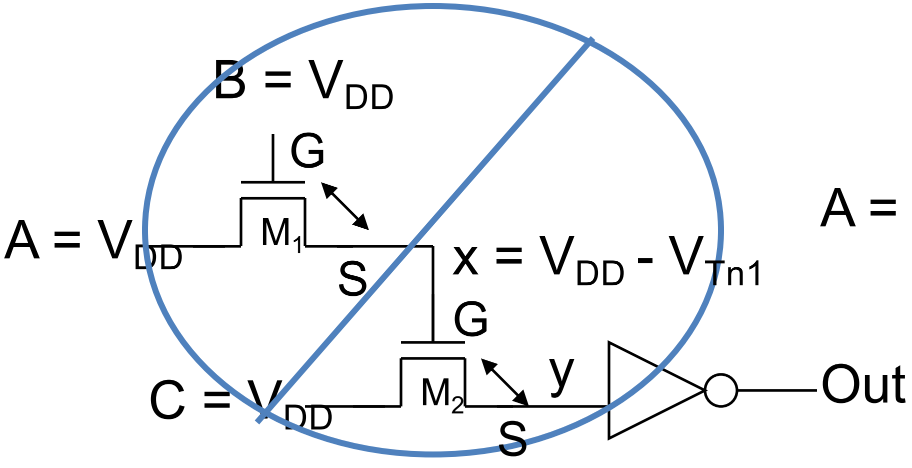


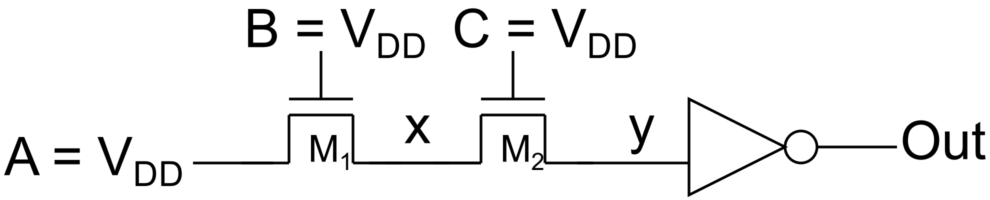


- Body effect – large V_{SB} at x - when pulling high (B is tied to GND and S charged up close to V_{DD})
- So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{(|2\phi_f| + V_x)} - \sqrt{|2\phi_f|}))$$

Cascaded NMOS Only PTs



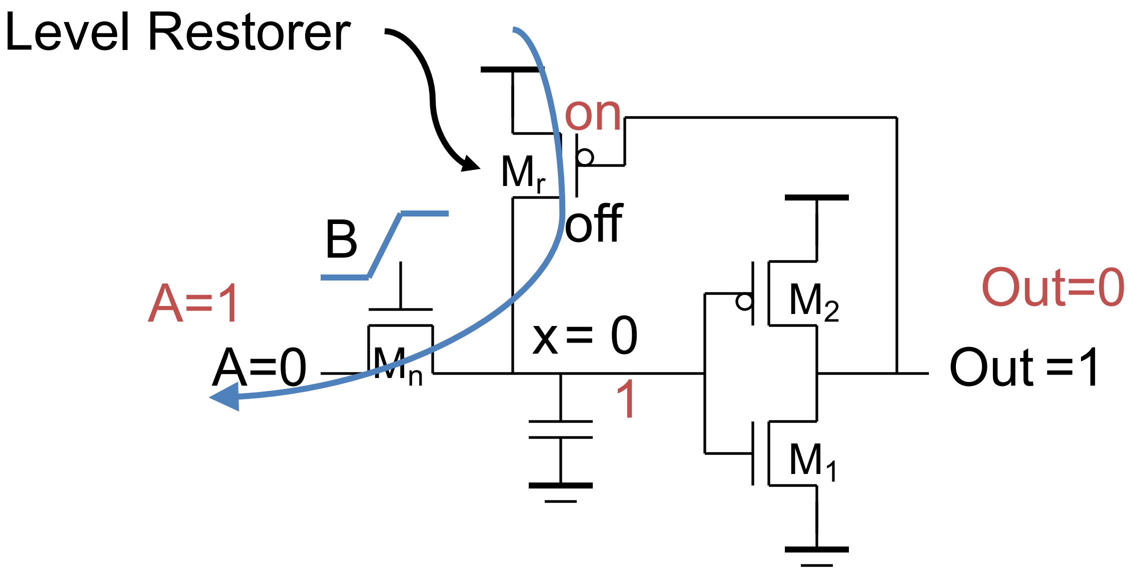


Swing on y = V_{DD} - V_{Tn1} - V_{Tn2}

Swing on y = V_{DD} - V_{Tn1}

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

Solution 1: Level Restorer

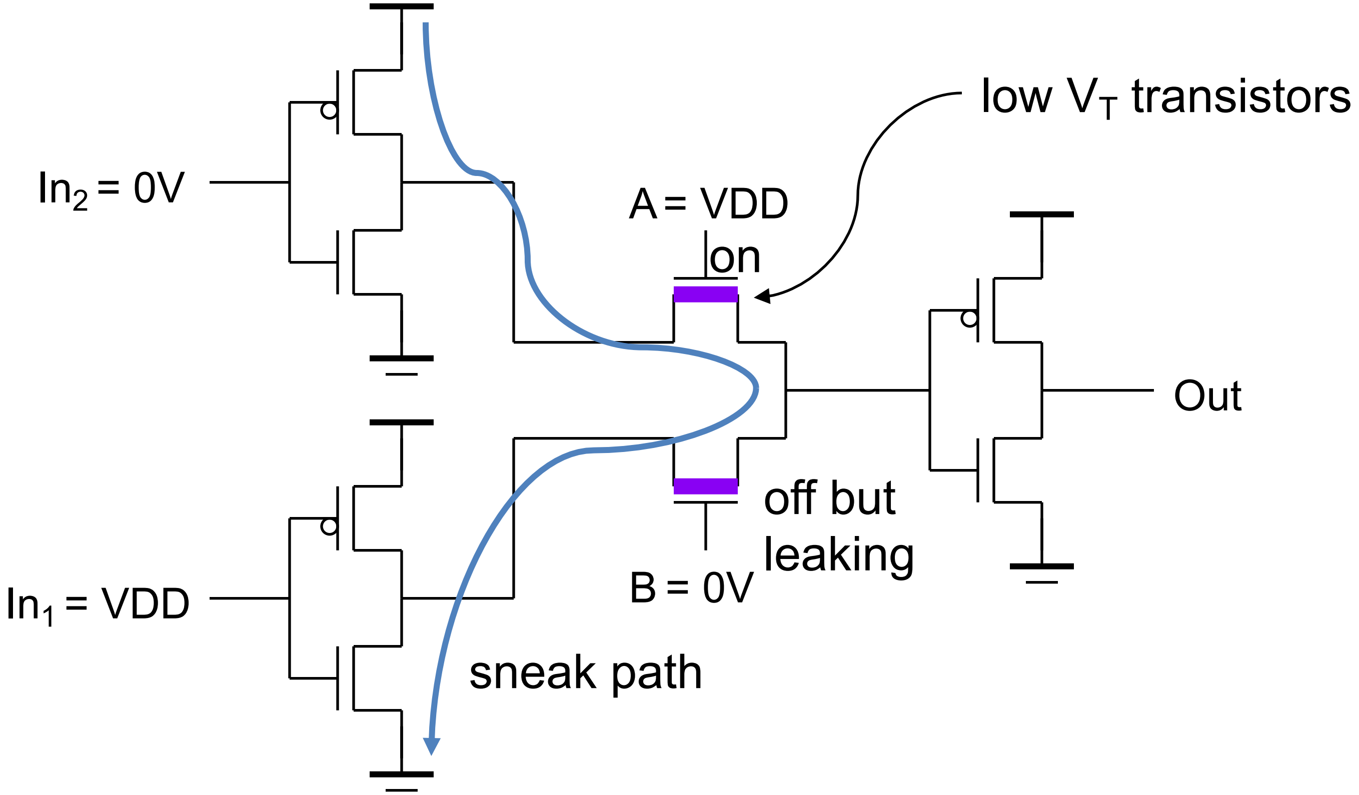


- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when A is high

For correct operation M_r must be sized correctly (ratioed)

Solution 2: Multiple V_T Transistors

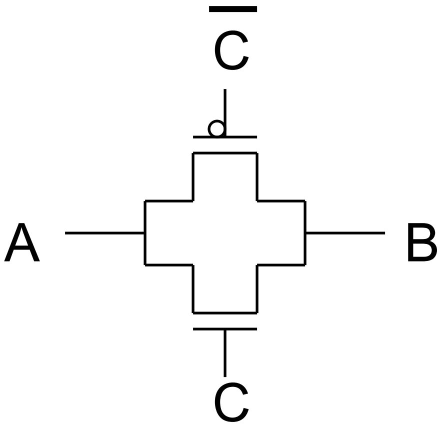
- Technology solution: Use (near) zero V_T devices for the NMOS PTs to eliminate *most* of the threshold drop (body effect still in force preventing full swing to V_{DD})

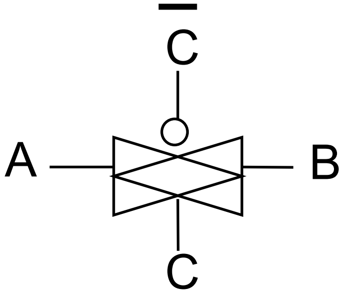


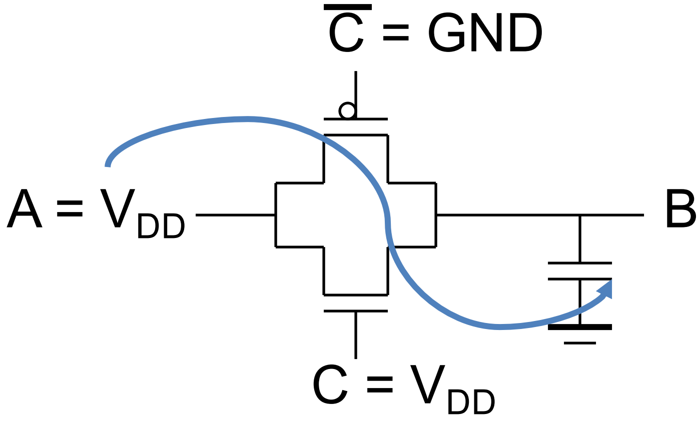
- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if V_{GS} is below V_T)

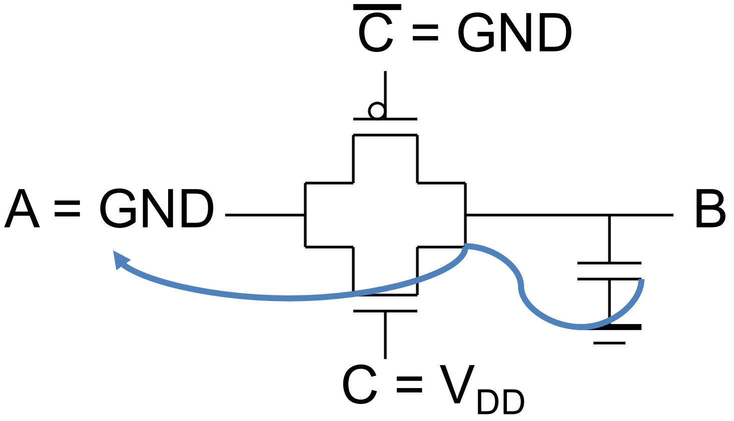
Solution 3: Transmission Gates (TGs)

- Most widely used solution





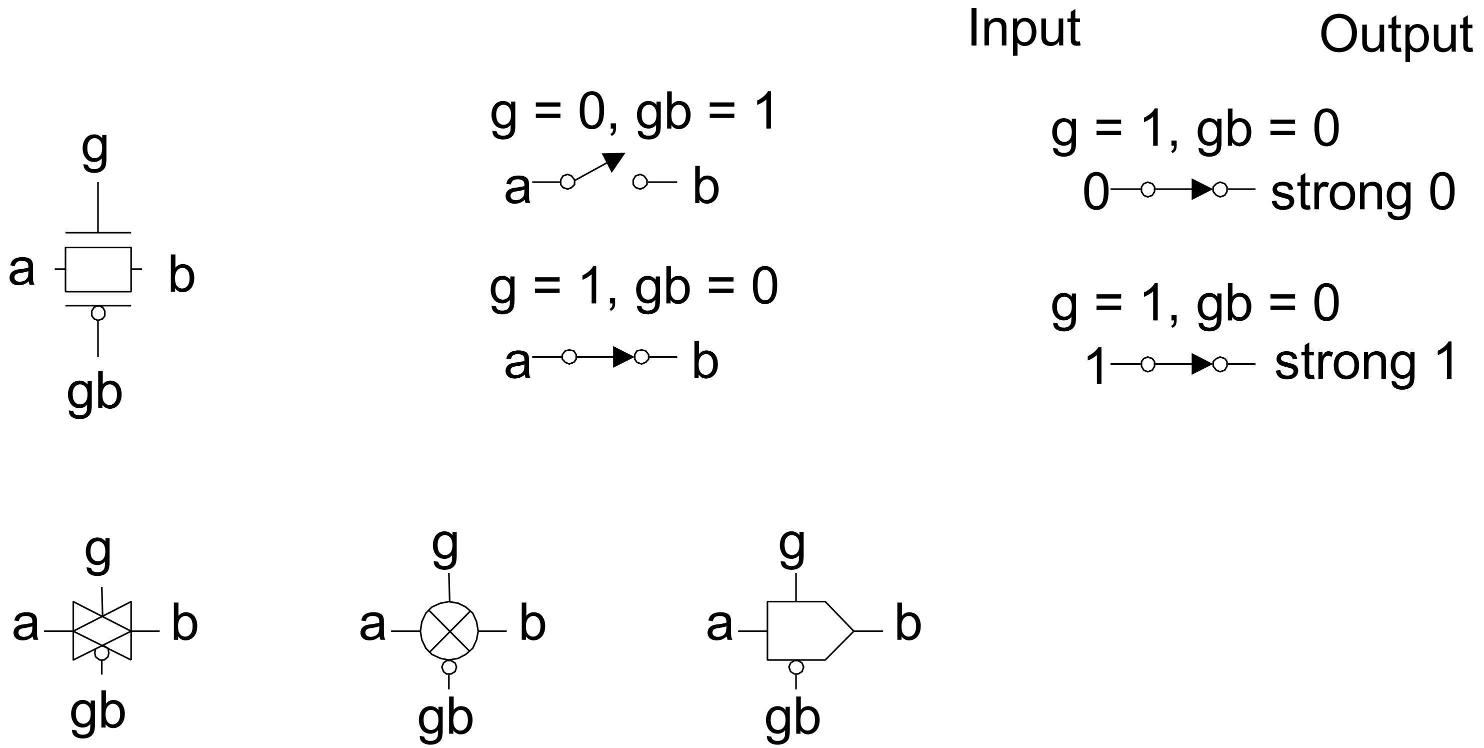




- Full swing *bidirectional* switch controlled by the gate signal C, A = B if C = 1

Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well



Input

Output

g = 0, gb = 1

g = 1, gb = 0

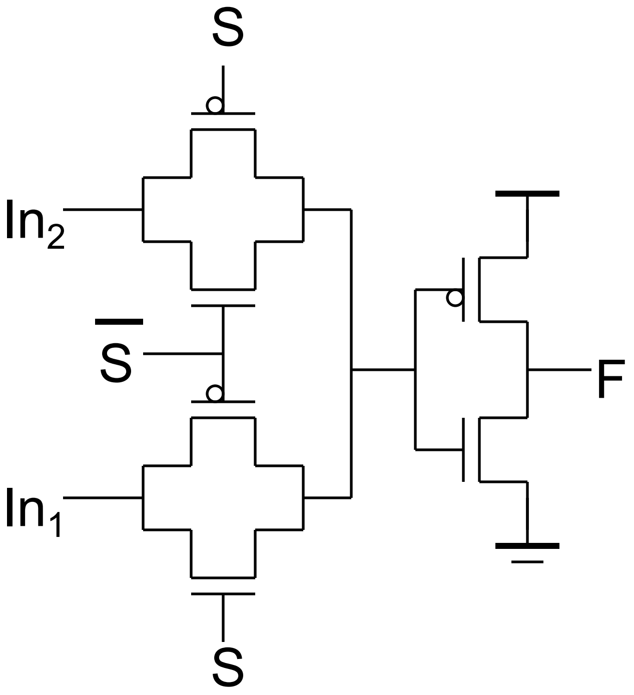
g = 1, gb = 0

strong 0

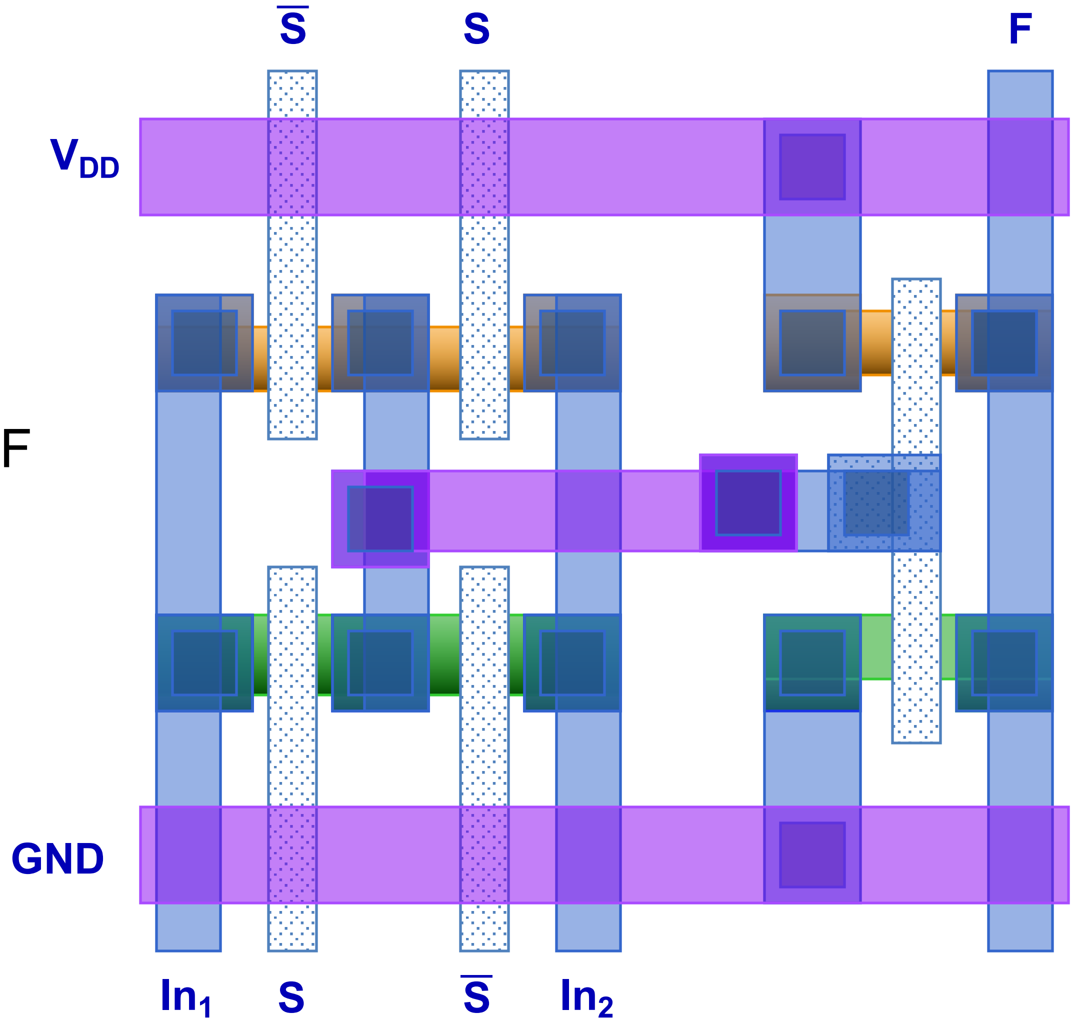
g = 1, gb = 0

strong 1

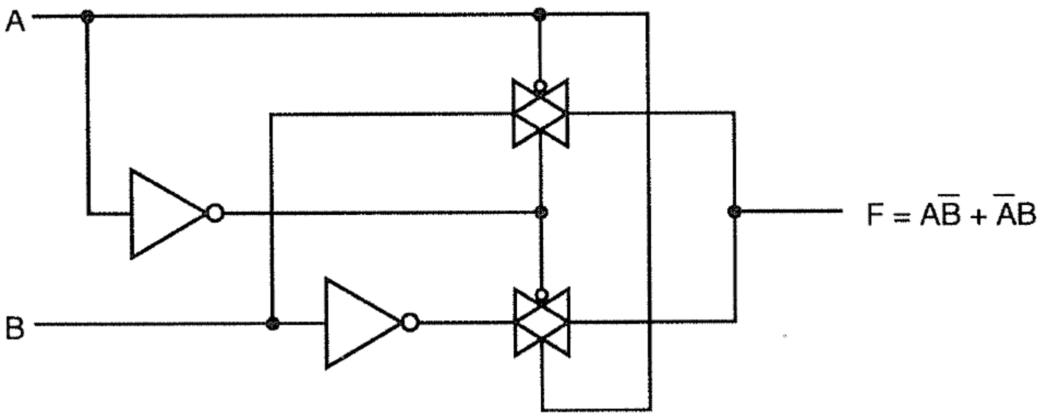
TG Multiplexer

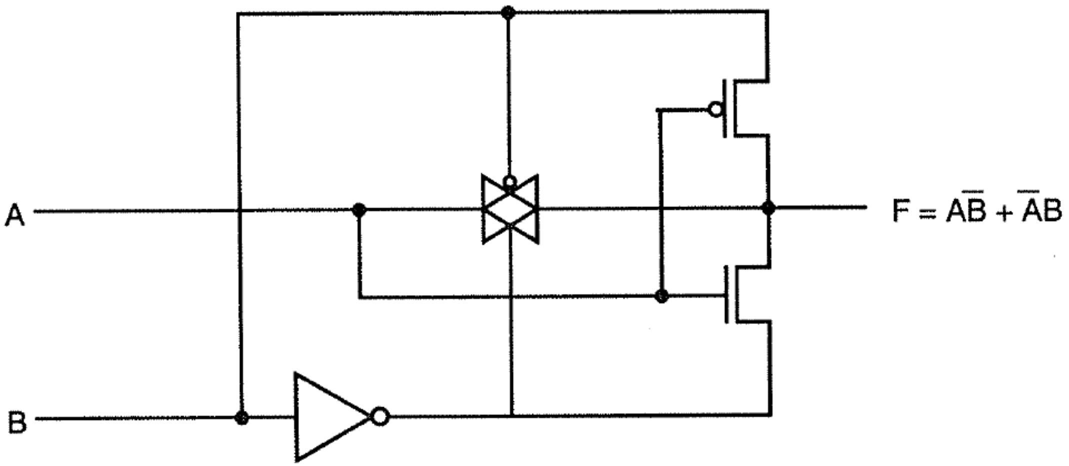


$$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$$

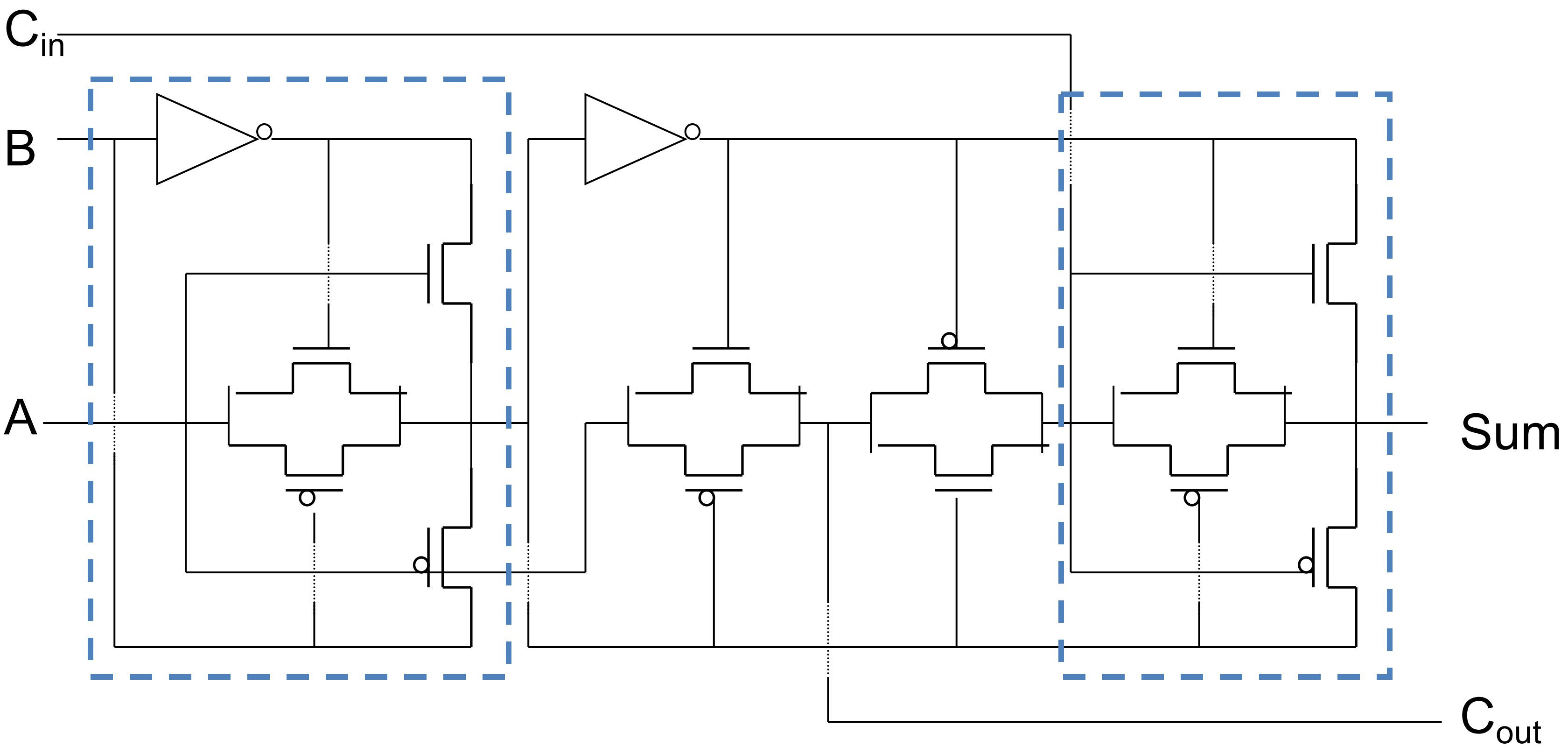


TG-Based XOR function

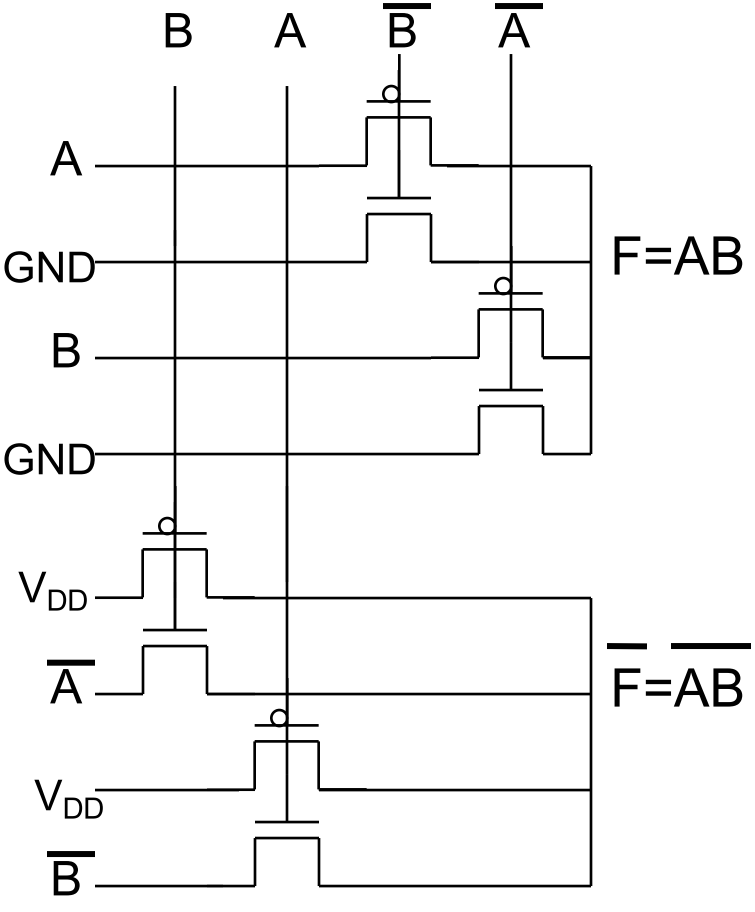




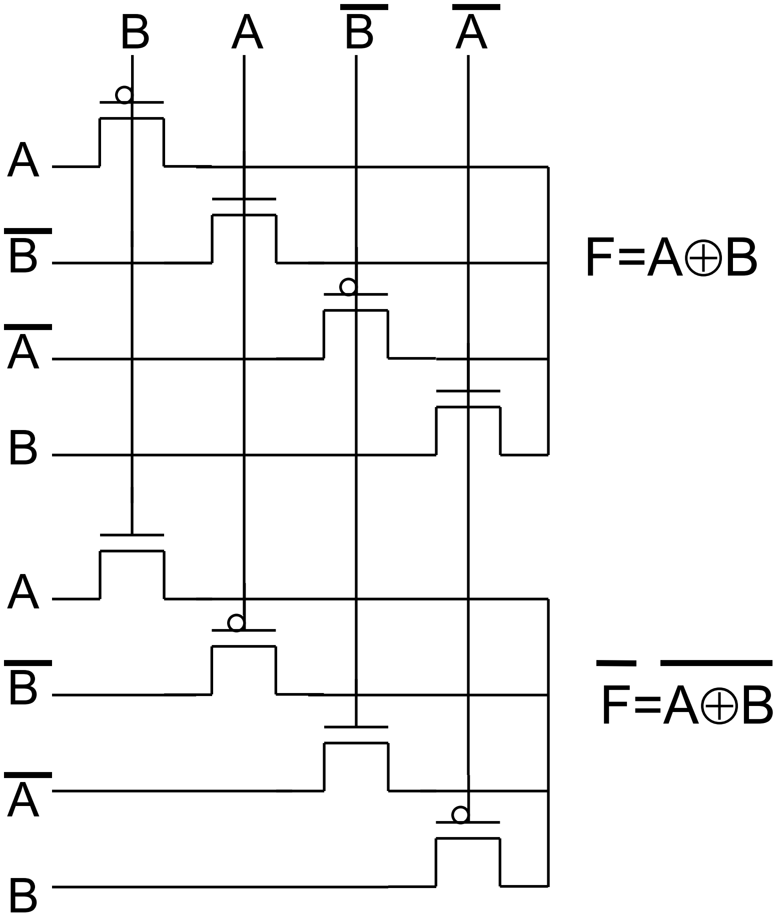
TG Full Adder



Differential TG Logic (DPL)



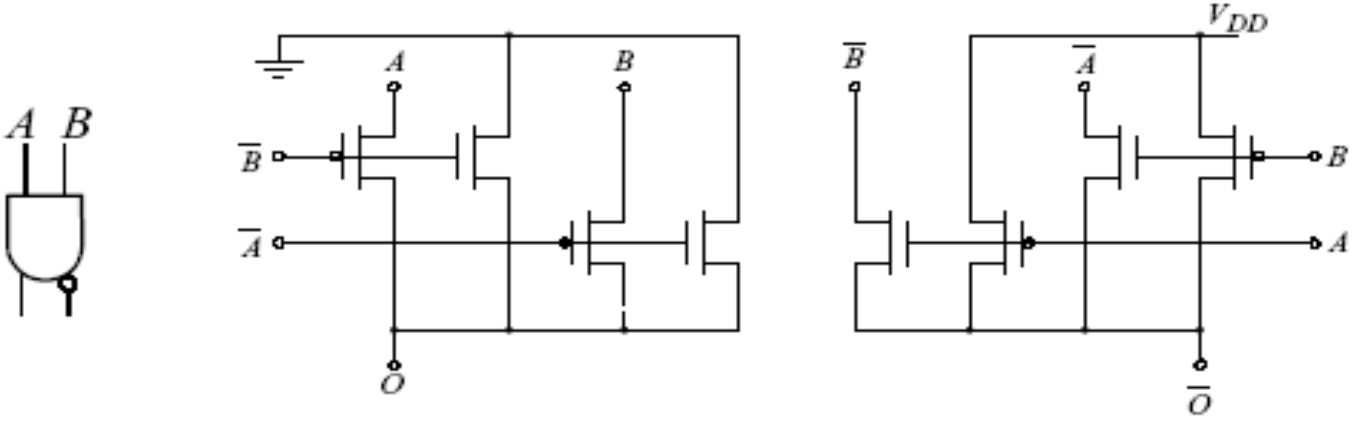
AND/NAND



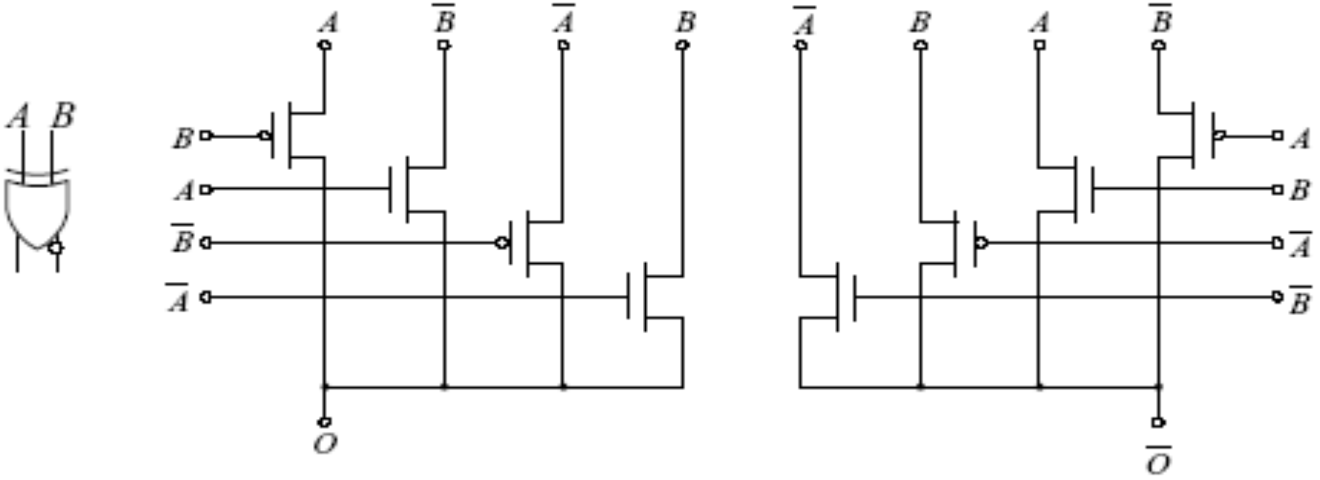
XOR/XNOR

Double Pass-Transistor Logic (DPL)

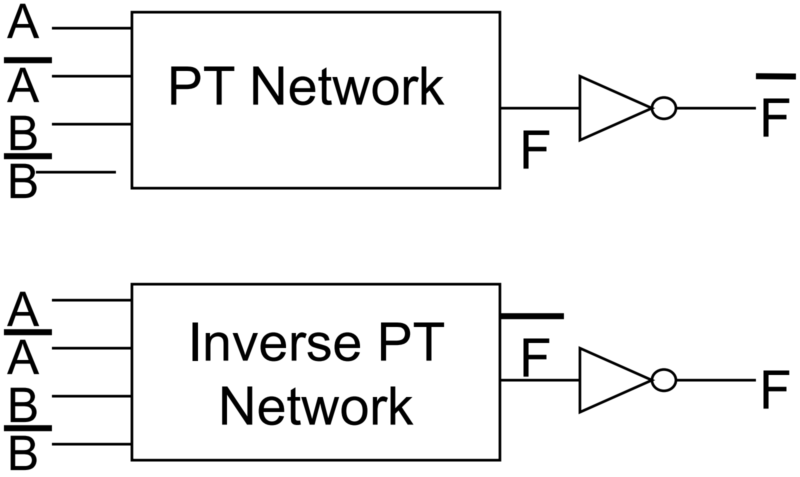
AND/NAND

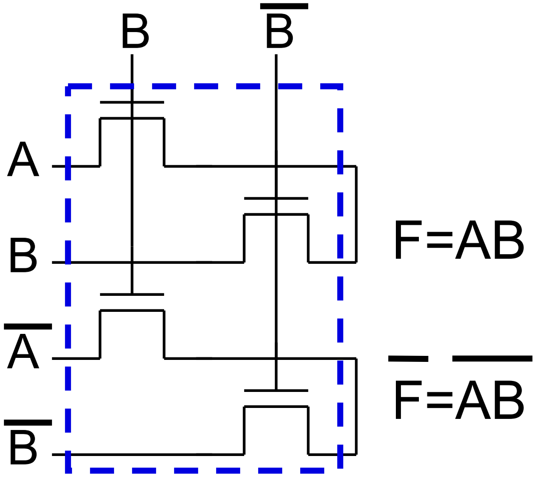


XOR/XNOR

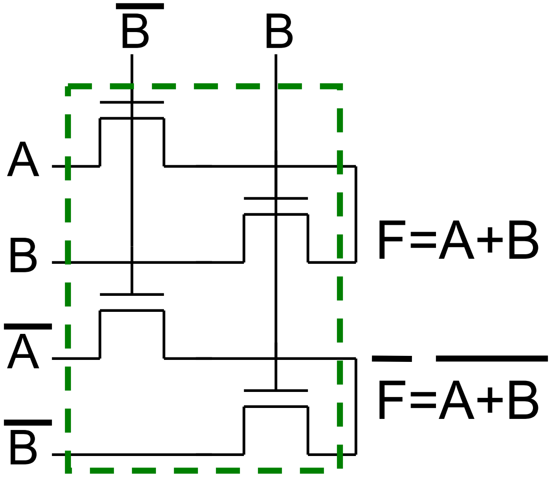


Differential/Complemental PT Logic (CPL)

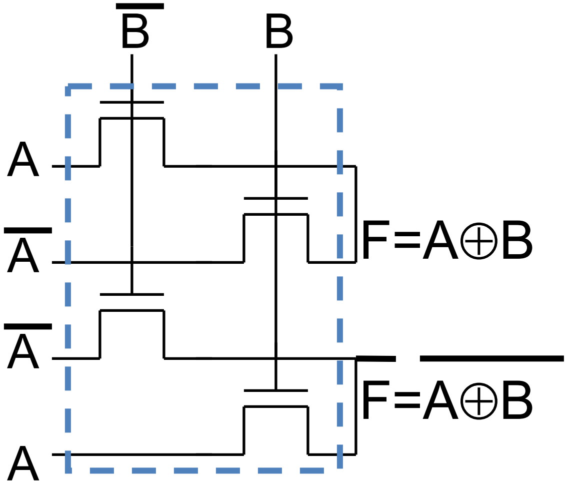




AND/NAND

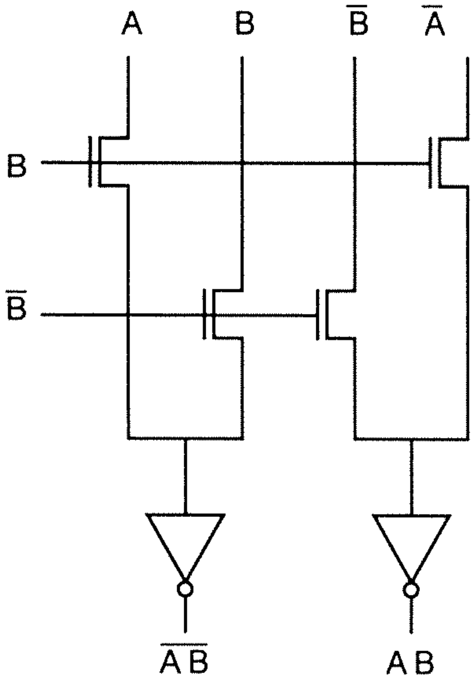


OR/NOR

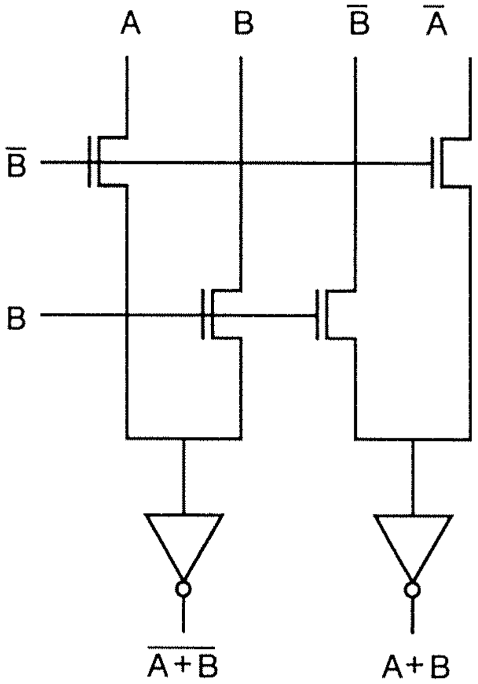


XOR/XNOR

CPL NAND2/NOR2 gates



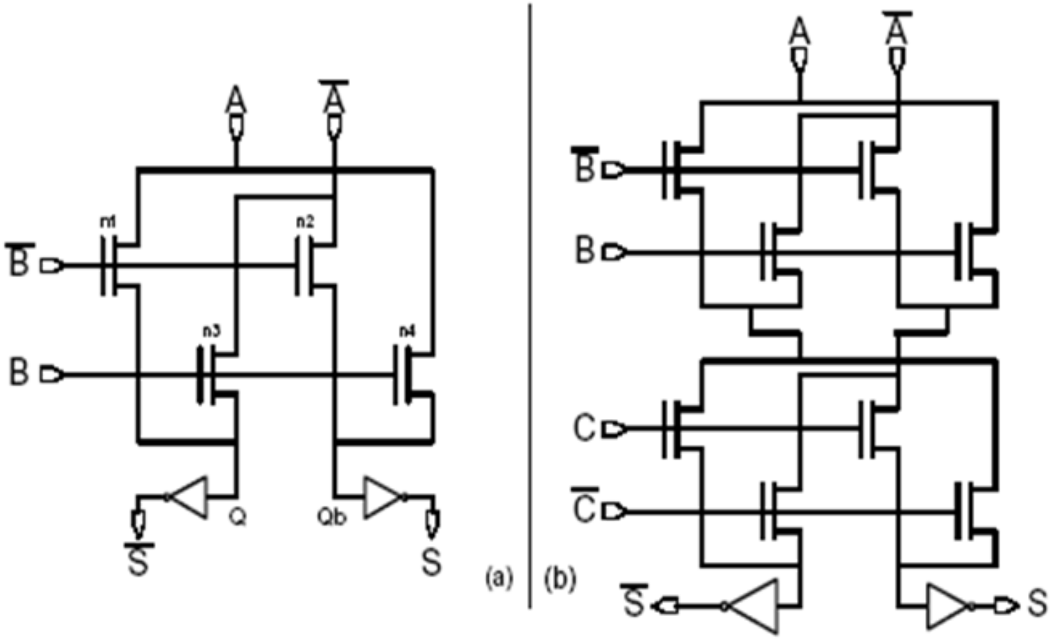
CPL NAND2



CPL NOR2

CPL XOR and Sum

- NMOS logic network (V_T drop)
- Fast
- Efficient implementation of arithmetic



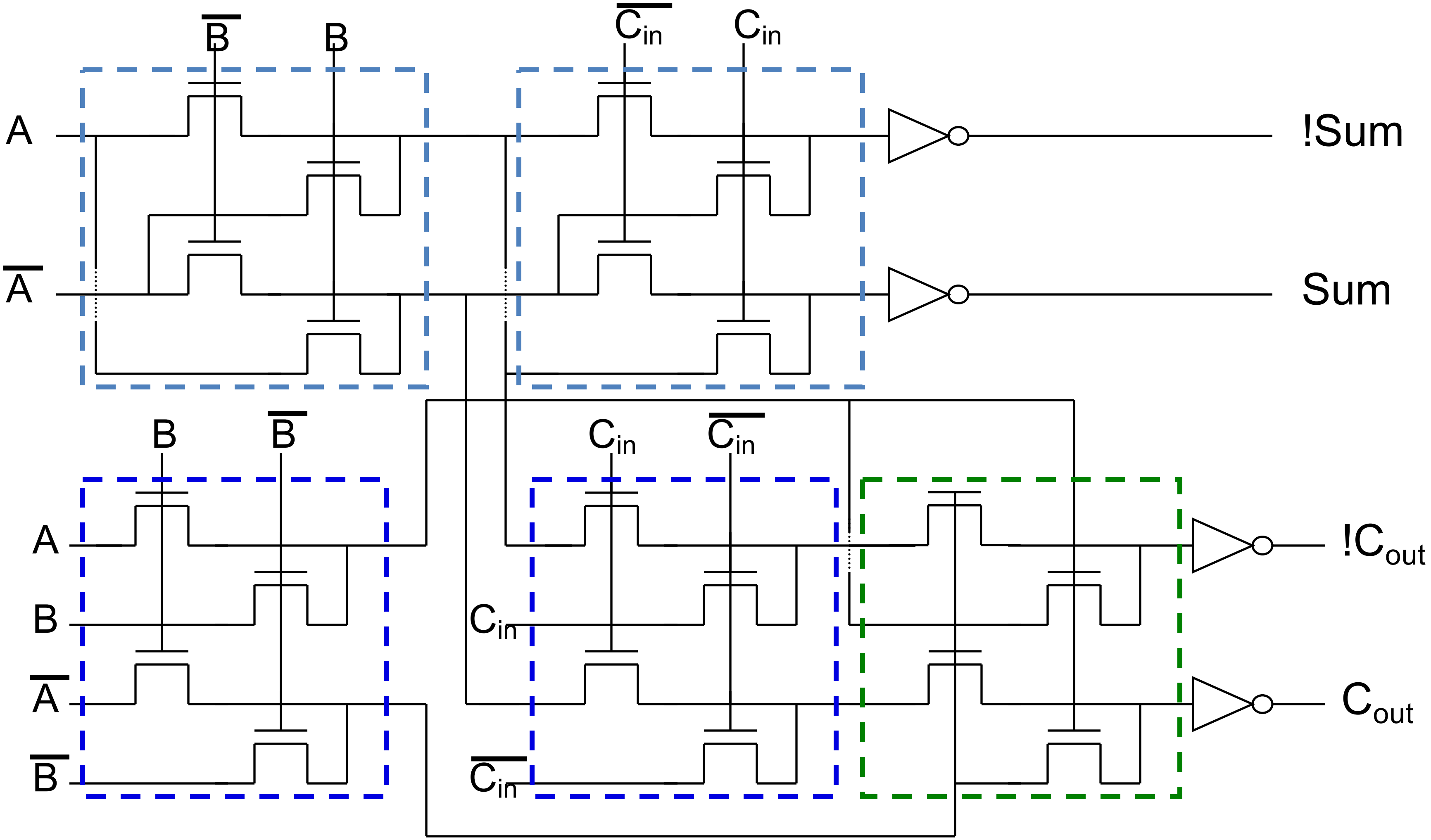
XOR

Sum

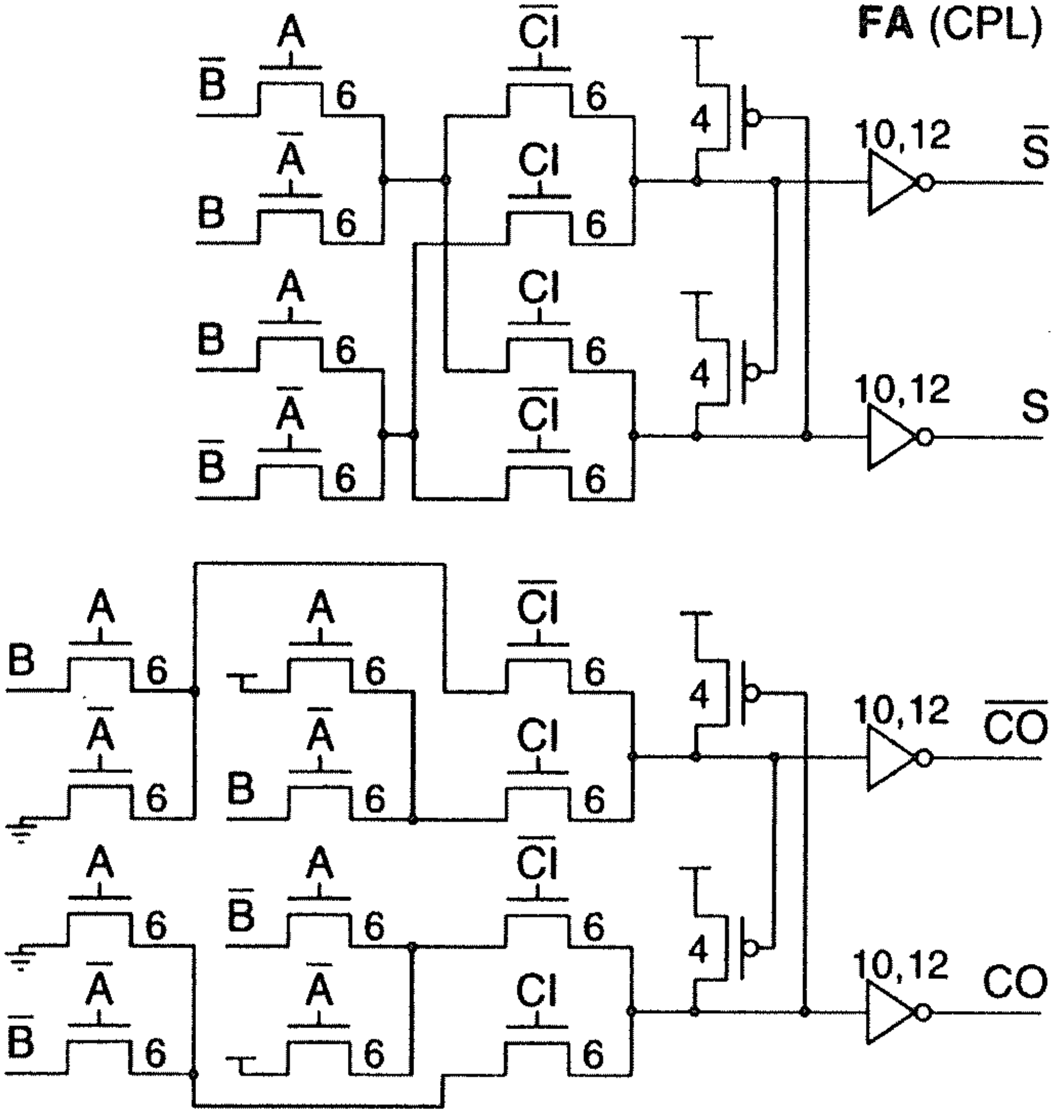
CPL Properties

- Differential so complementary data inputs and outputs are always available (so don’t need extra inverters)
- Still static, since the output defining nodes are always tied to V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

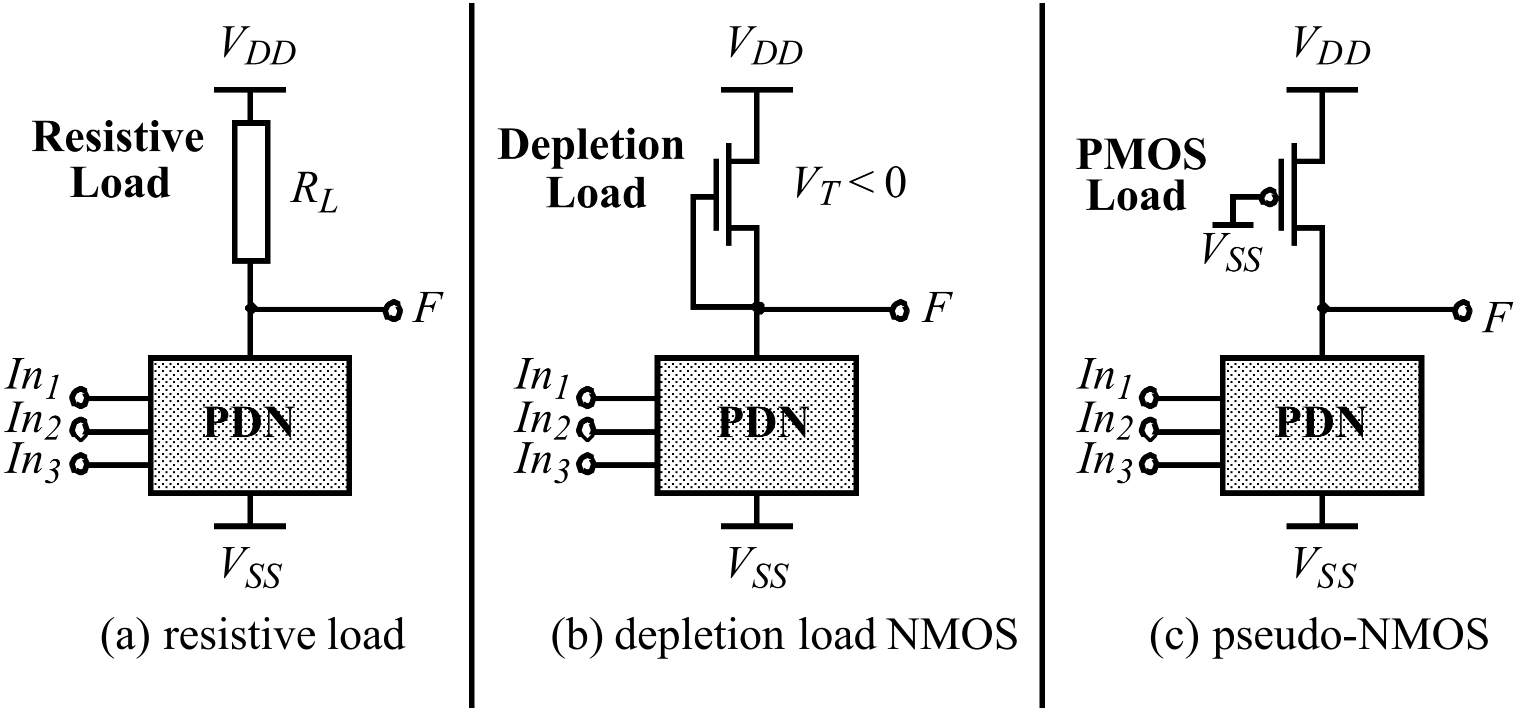
CPL Full Adder



Circuit Diagram of a CPL full adder



Ratioed Logic



(a) resistive load

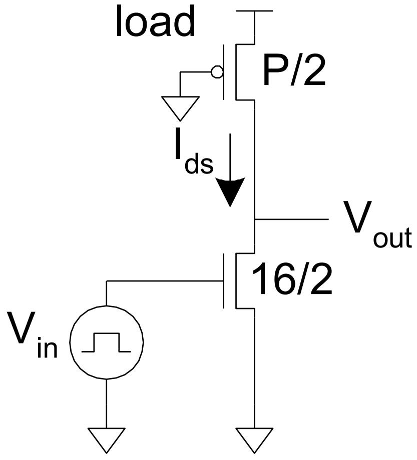
(b) depletion load NMOS

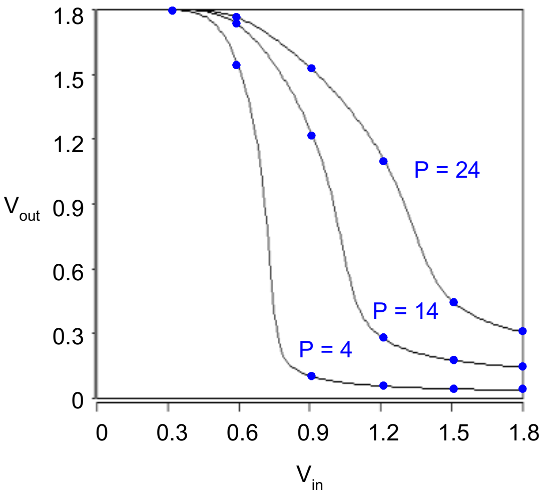
(c) pseudo-NMOS

Goal: to reduce the number of devices over complementary CMOS

Pseudo-nMOS

- In the old days, nMOS processes had no pMOS
  - Instead, use pull-up transistor that is always ON
- In CMOS, use a pMOS that is always ON
  - *Ratio* issue
  - Make pMOS about ¼ effective strength of pulldown network

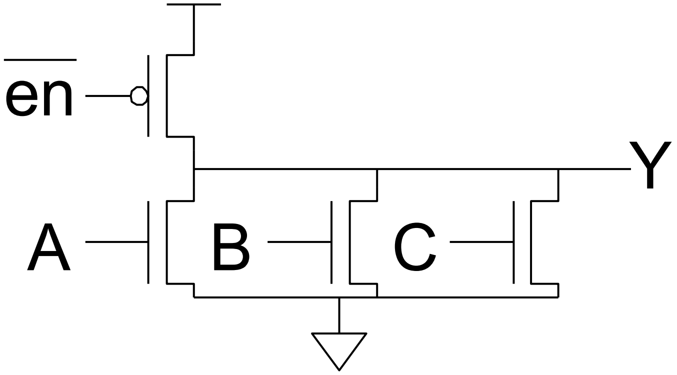




pMOS fights nMOS

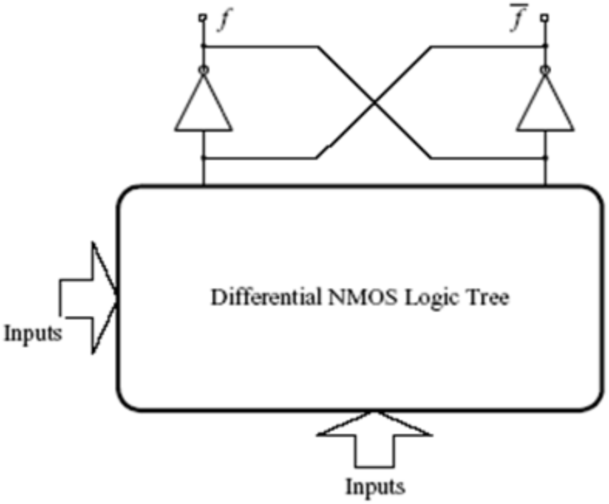
Pseudo-nMOS Power

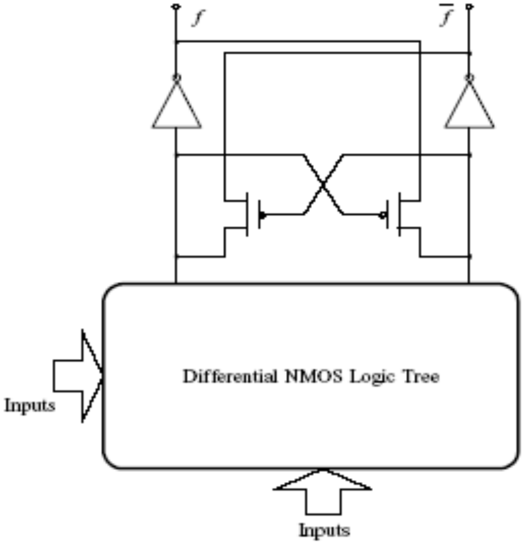
- Pseudo-nMOS draws power whenever Y = 0
  - Called static power $P = I_{DD}V_{DD}$
  - A few mA / gate * 1M gates would be a problem
  - Explains why nMOS went extinct
- Use pseudo-nMOS sparingly for wide NORs
- Turn off pMOS when not in use



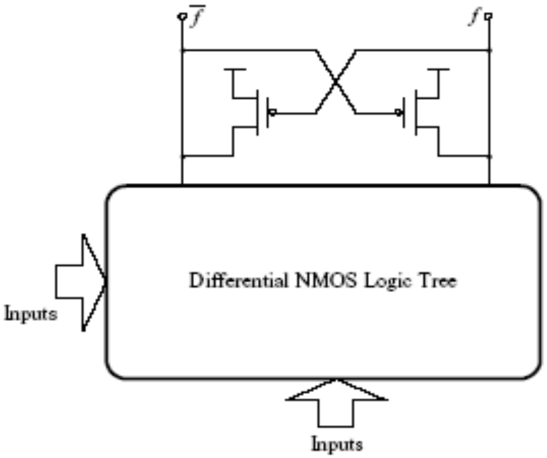
Different Restoration Schemes

- Swing-restored pass-transistor logic





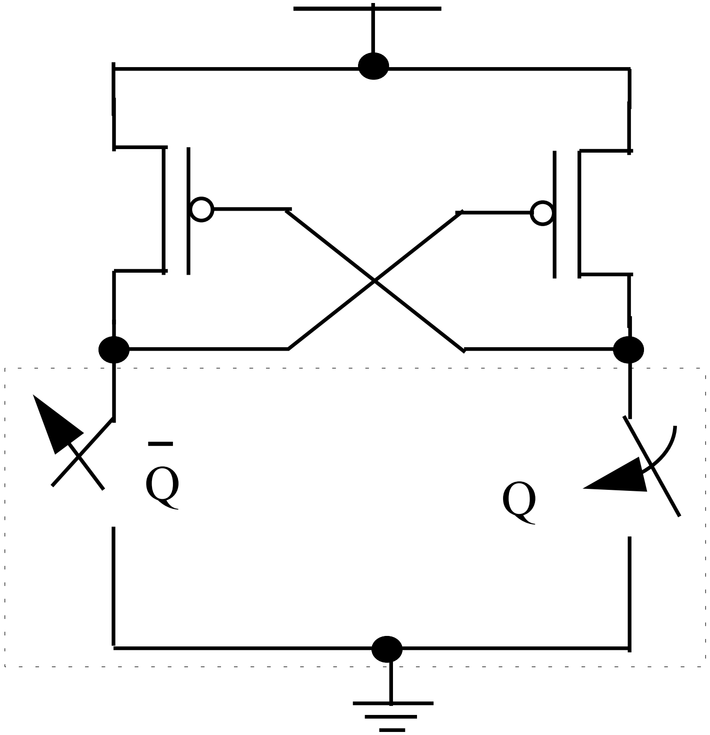
Energy Economized Pass-Transistor Logic



DCVS with Pass Gates (DCVS-PG)

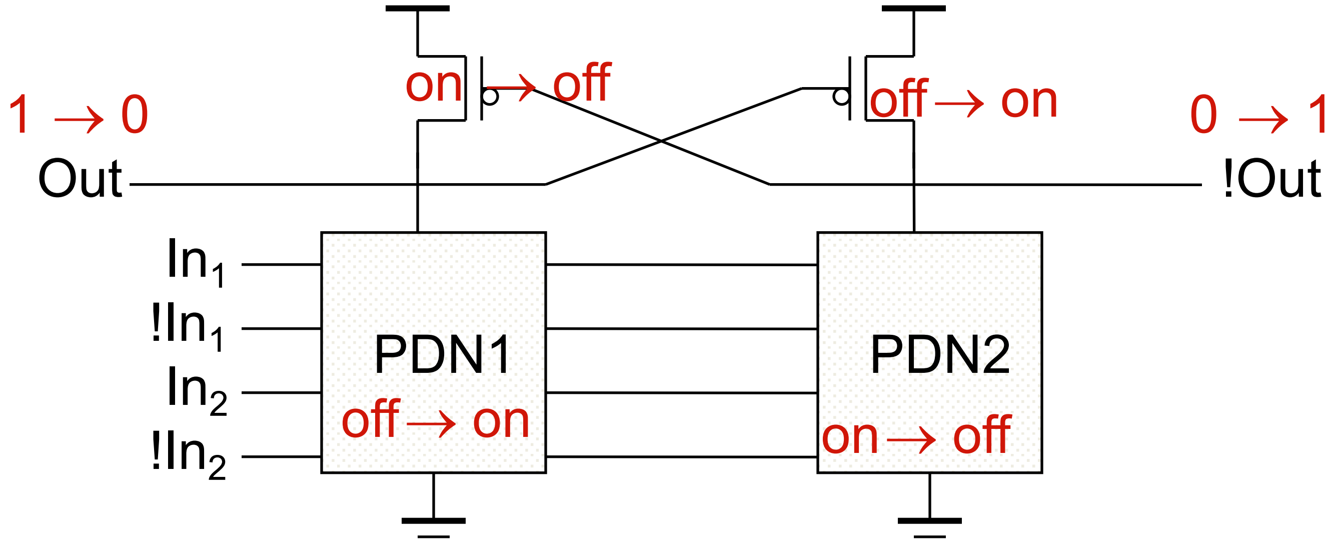
Differential Cascode Voltage Switch Logic

- Differential Cascode Voltage Switch (DCVS)
  - Differential Level Restoring
  - Complement outputs



DCVS Logic

- PDN1 and PDN2 are mutually exclusive
  - No DC power dissipation
  - Regenerative action sets PMOS latch to static outputs Q and Q’ of full VDD and GND logic level
  - NMOS rich =>increasing current and reducing load capacitance



DCVS Concept

$$Y(A,B,C,D,E,E,F,G)=\overline{G}\overline{A}\overline{F}+\overline{G}\overline{B}\overline{D}\overline{E}+\overline{G}\overline{B}\overline{C}\overline{F}+\overline{G}\overline{B}\overline{C}\overline{E}+\overline{G}\overline{C}\overline{D}\overline{E}$$

- ◆ Using complementary static logic : 38 transistor

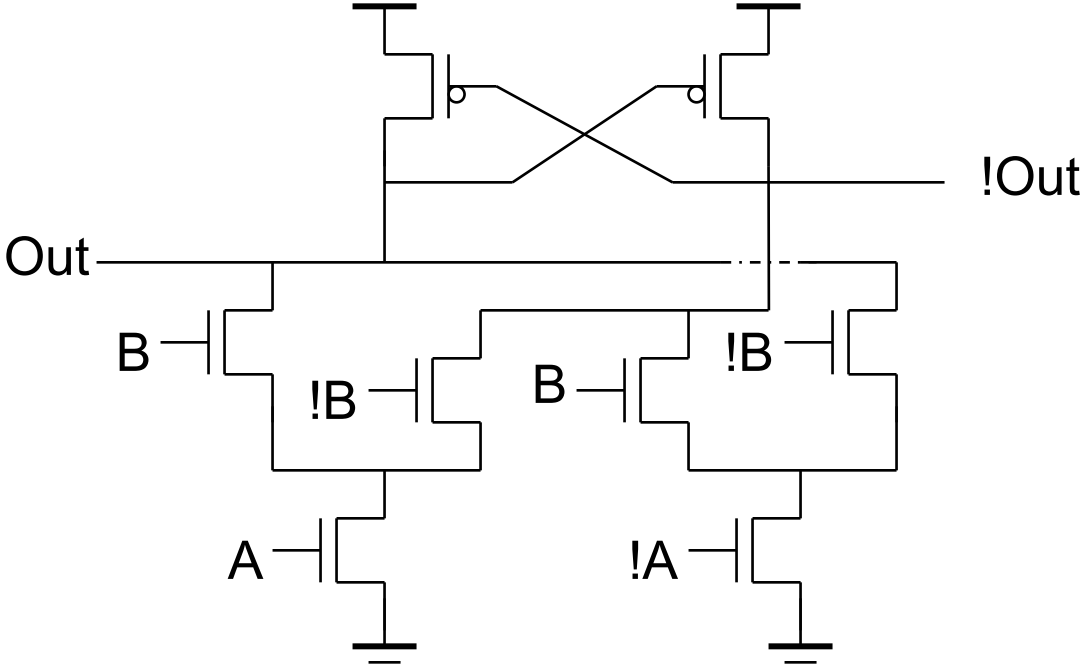
$$Y(A,B,C,D,E,E,F,G)=\overline{G}(\overline{A}\overline{F}+\overline{B}\overline{D}\overline{E}+\overline{C}(\overline{B}\overline{F}+\overline{E}(\overline{B}+\overline{D})))$$

- ◆ Using complementary static logic with cascade tree : 24 transistor

- ■ The cascade tree can be used in any logic type : try to extract as many common subexpression as possible.

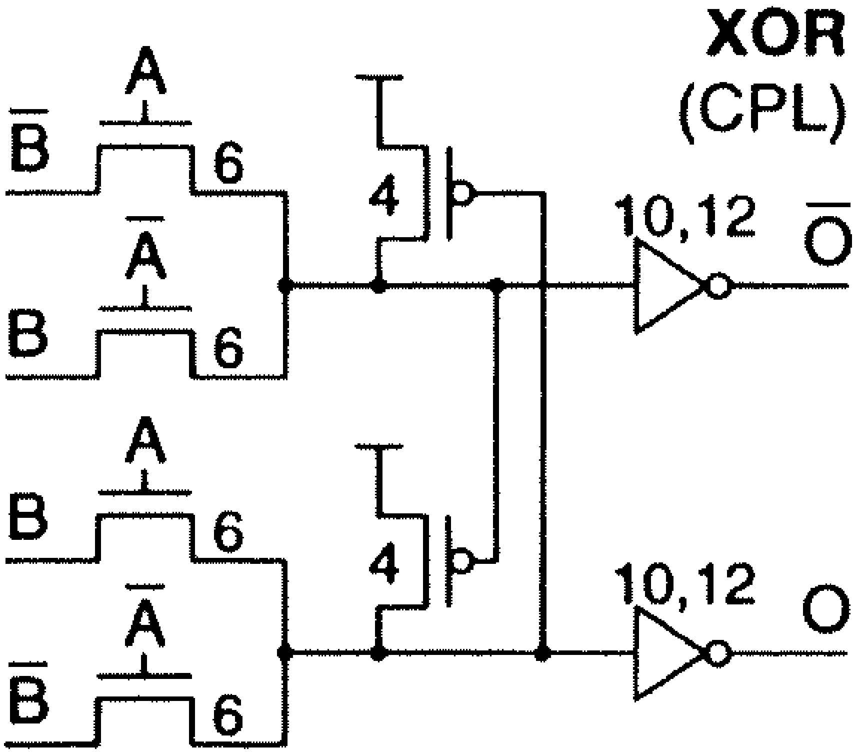
DCVS Example

- XOR-XNOR gate in only 8 transistors as opposed to 10 in complement static CMOS



DCVS+CPL XOR gate

- DCVS+CPL
  - ◆ or called DCVS + pass gate (DCVSPG)


XOR
(CPL)
A
$\bar{B}$
6
$\bar{A}$
B
6
4
10,12
$\bar{O}$
A
B
6
$\bar{A}$
$\bar{B}$
6
4
10,12
O