Digital IC Design

Lecture 9:
Layout of FinFET Standard Cells

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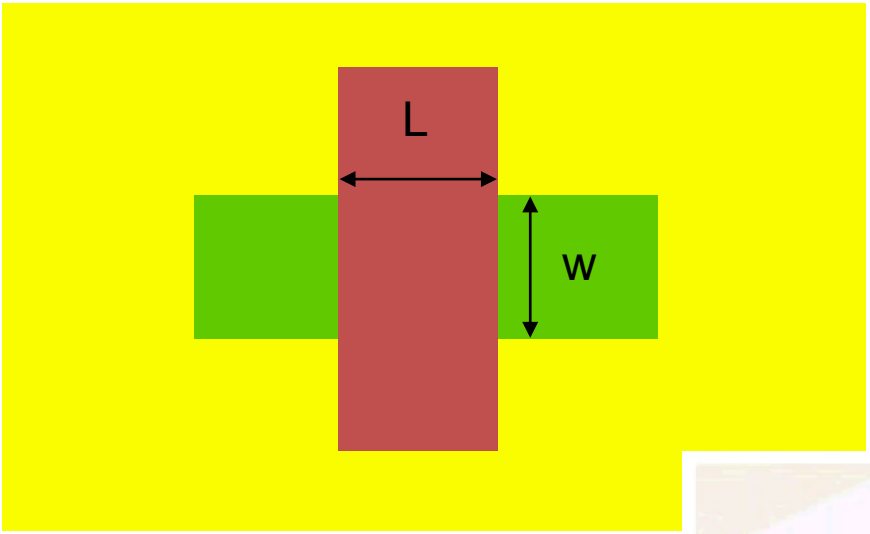
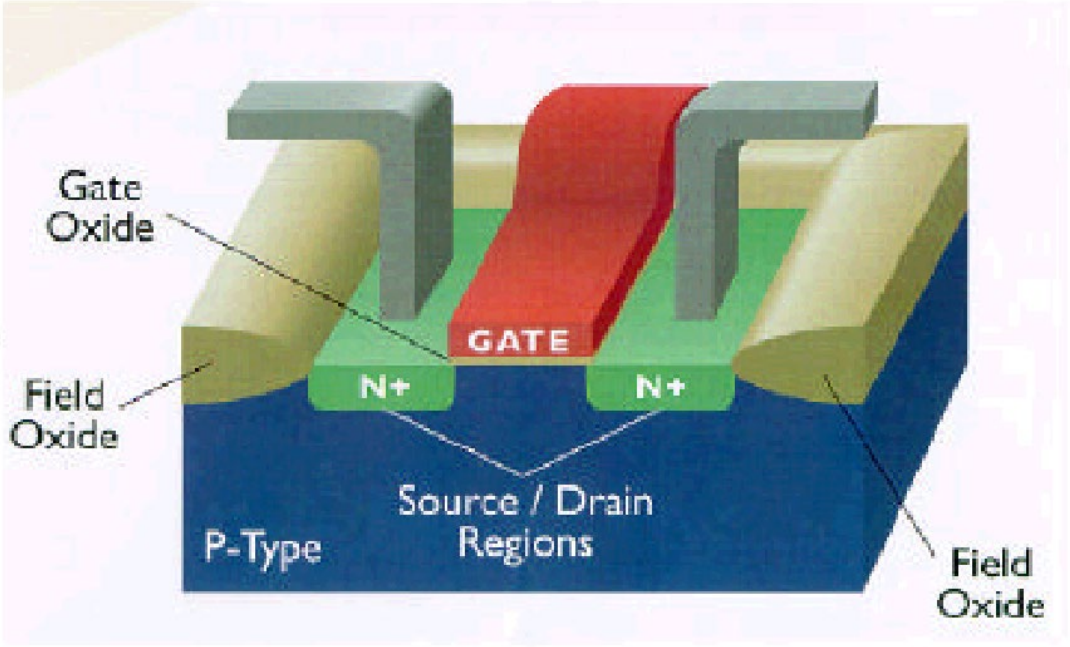
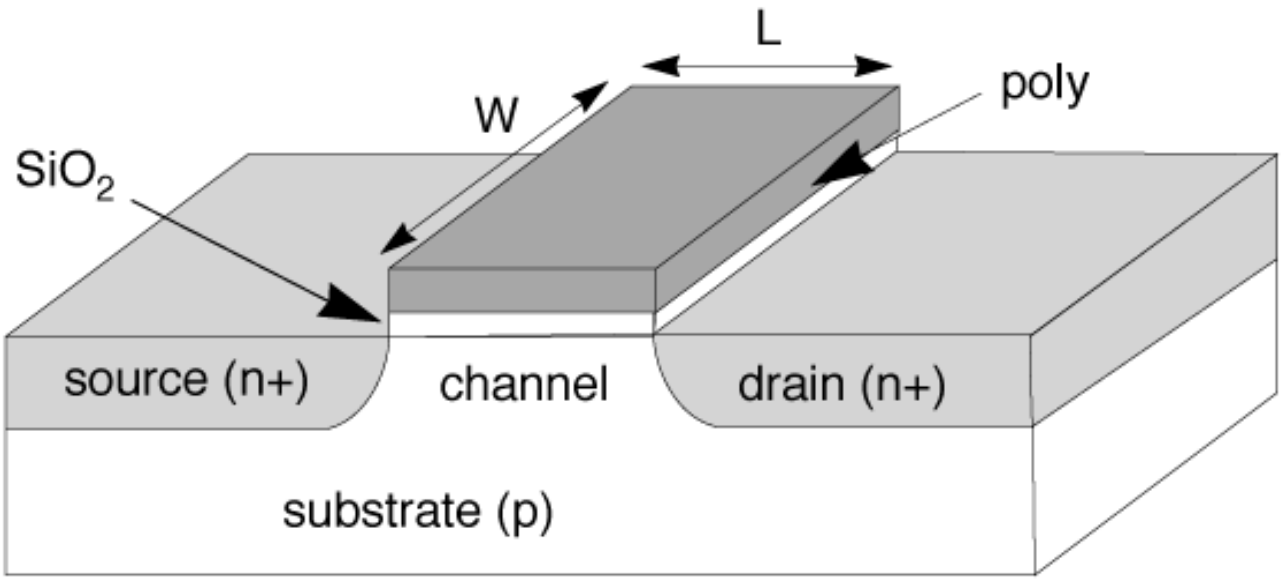
Transistor Layout





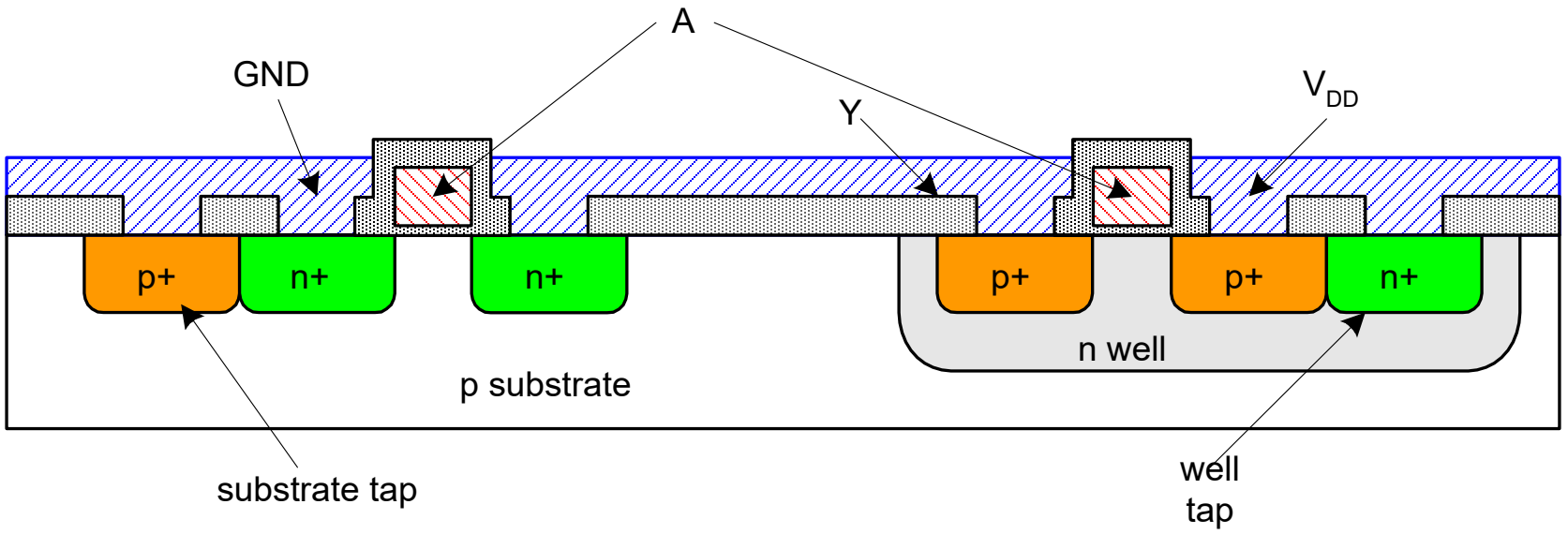
Transistor Structure

- n-type transistor



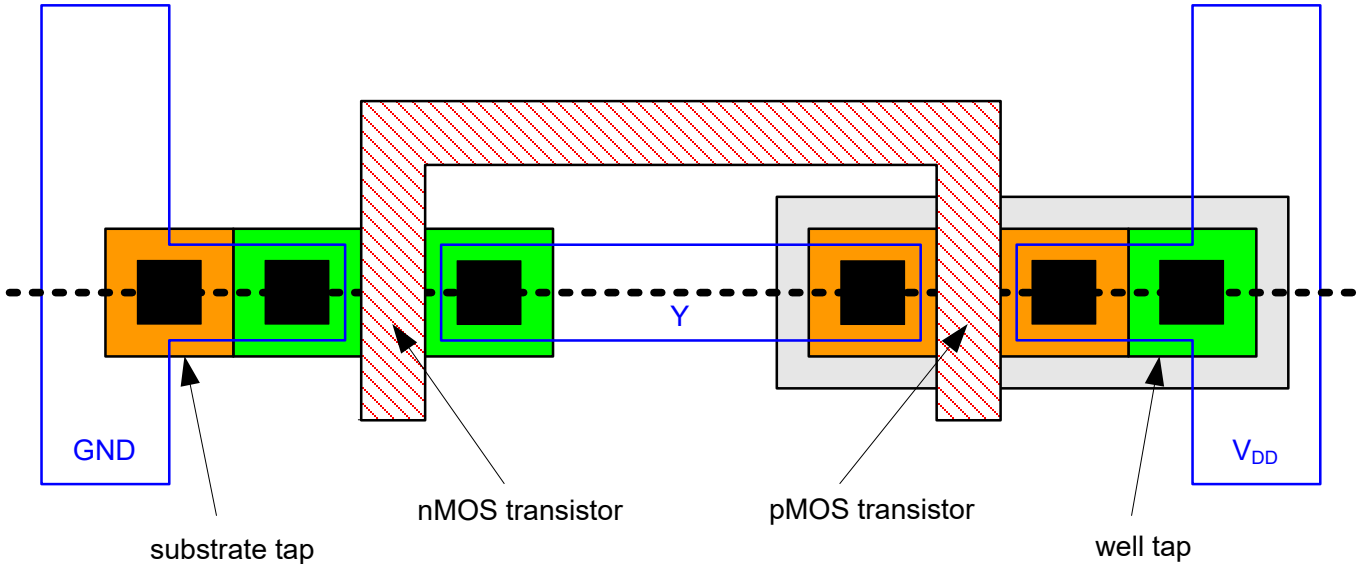
Inverter Cross-section Well and Substrate Taps

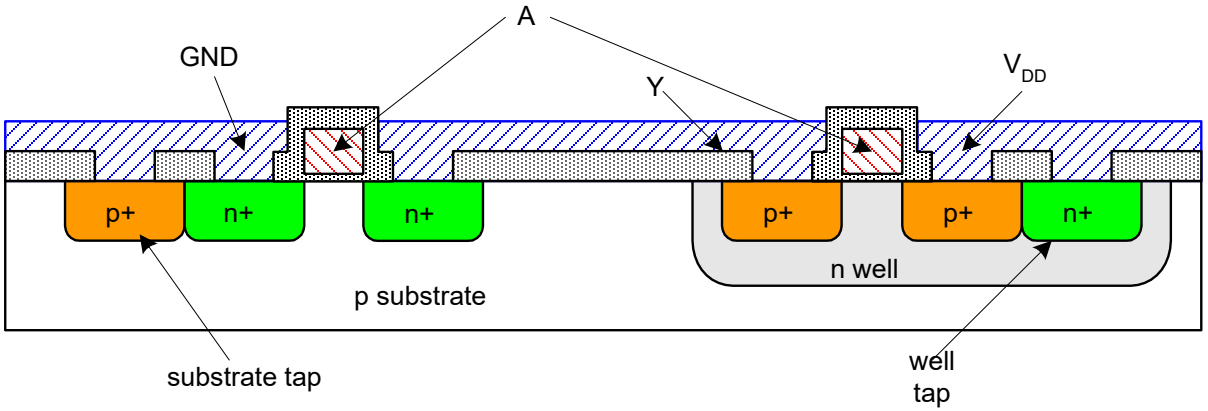
- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



Inverter Mask Set

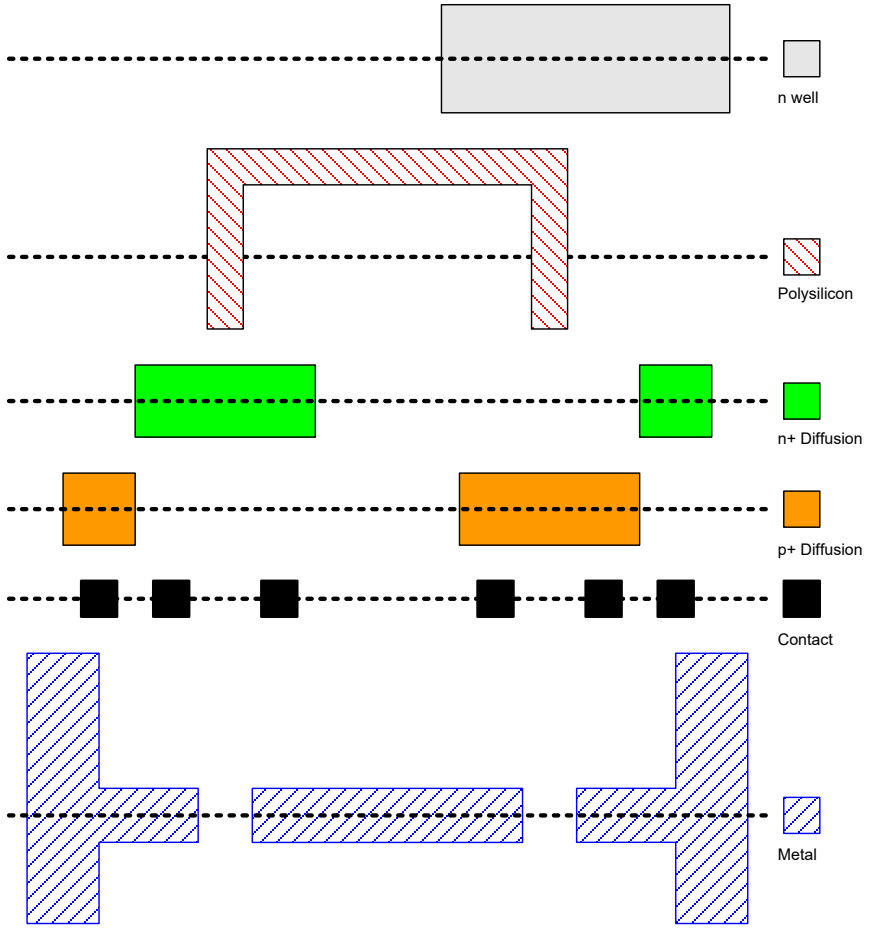
- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line





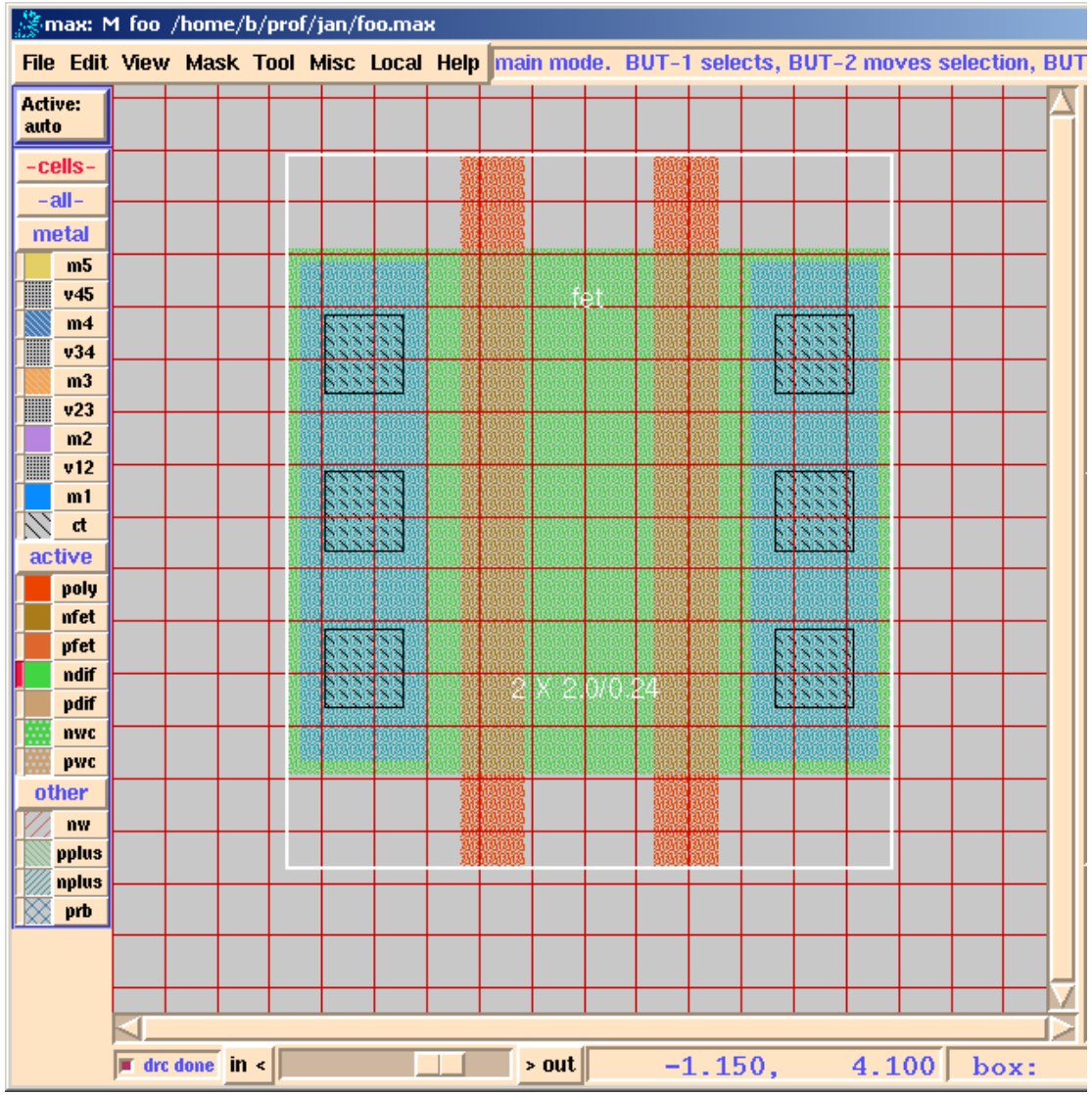
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

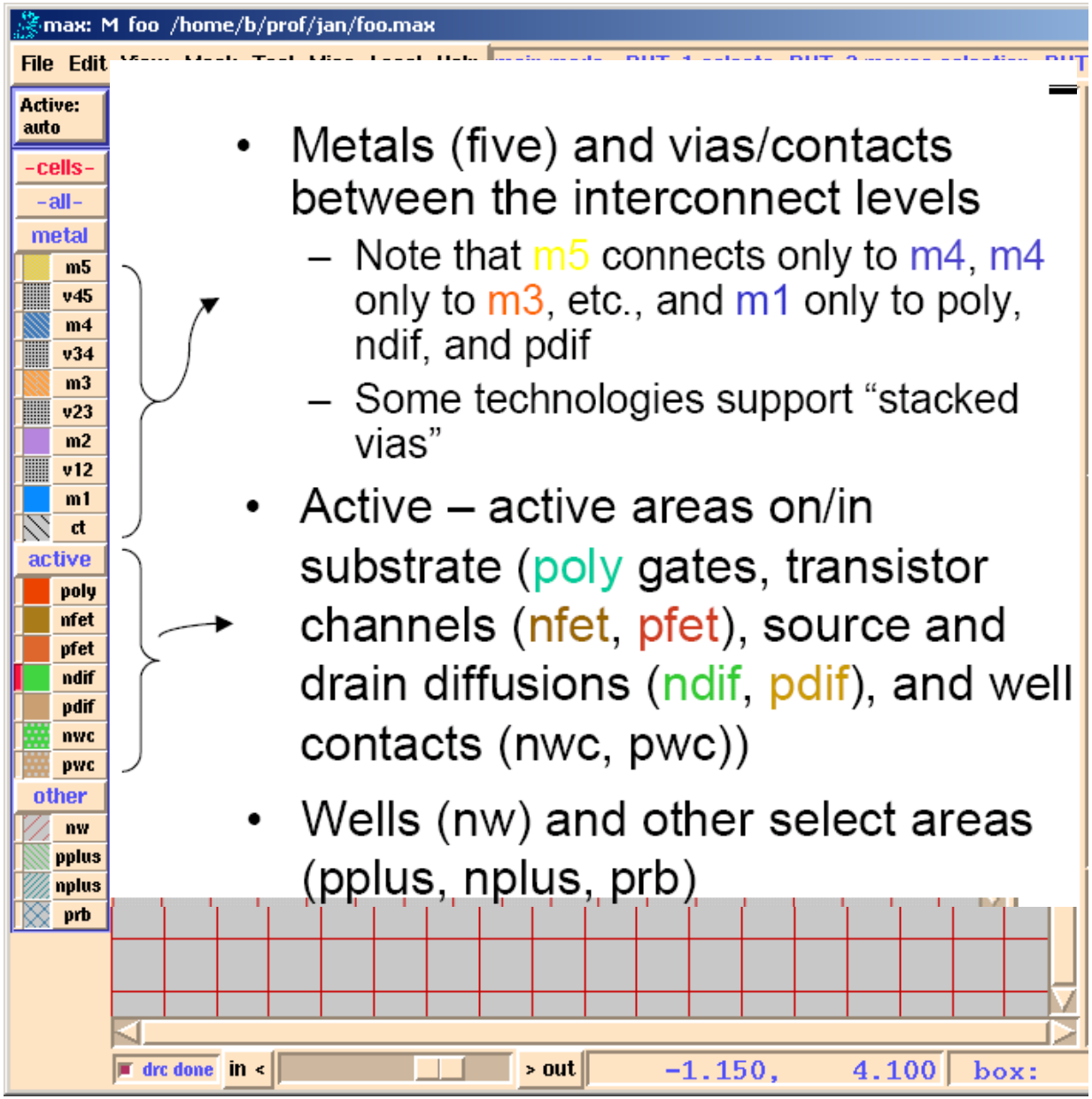


Layout Editor

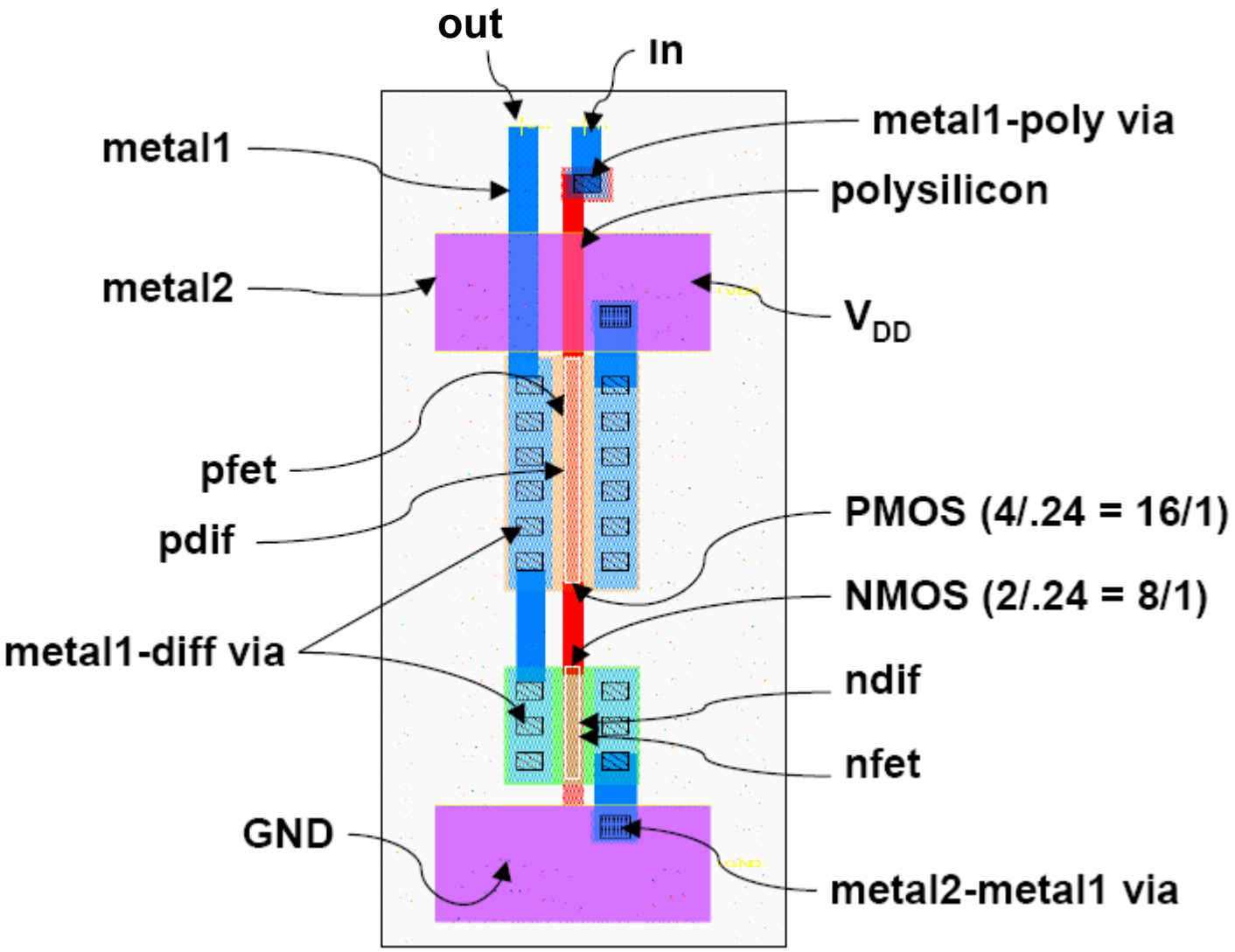
- Similar for all tools



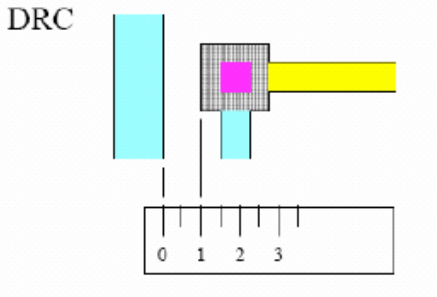
Layer Information



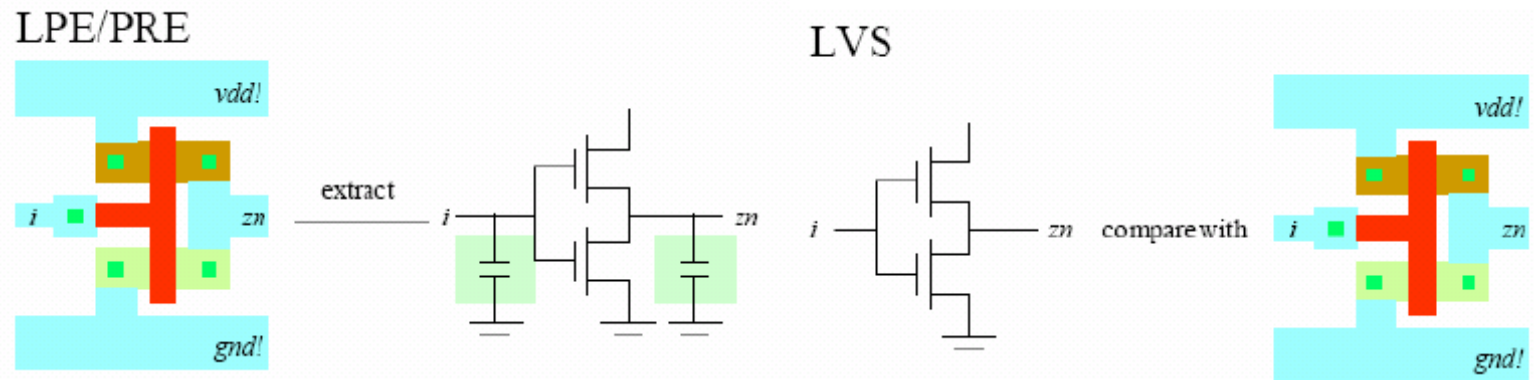
CMOS Inverter Layout



DRC/LVS/LPE after Layout

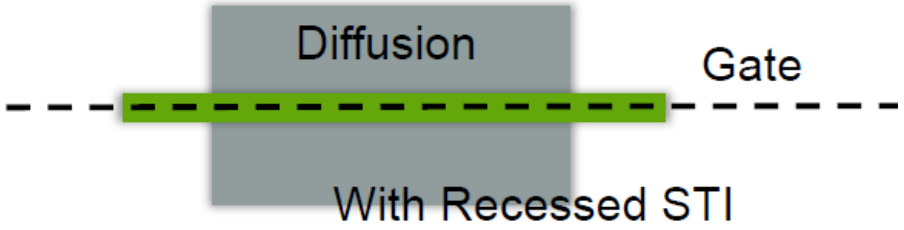


- DRC : Design Rule Checks
  - The operation checks for design rule violations.
- LVS : Layout Versus Schematic
  - The operation checks for inconsistencies between the schematic and the physical layout.
- LPE/PEX : Layout Parameter Extraction
  - Extract layout parameters, including transistors, parasitic capacitors, and resistors.
  - Extracted net-list will be used in Nanosim to run post layout simulation

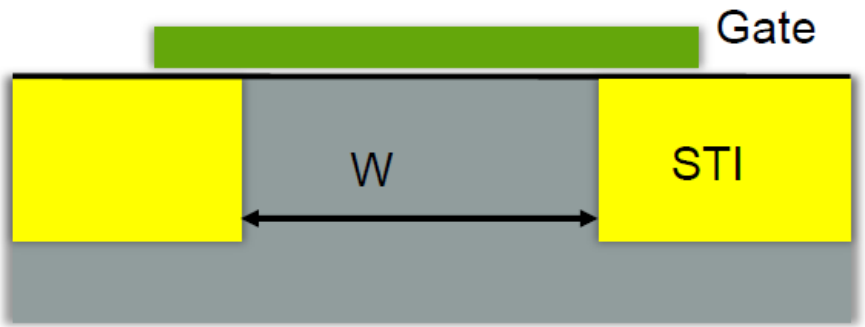


How to Think About FinFET

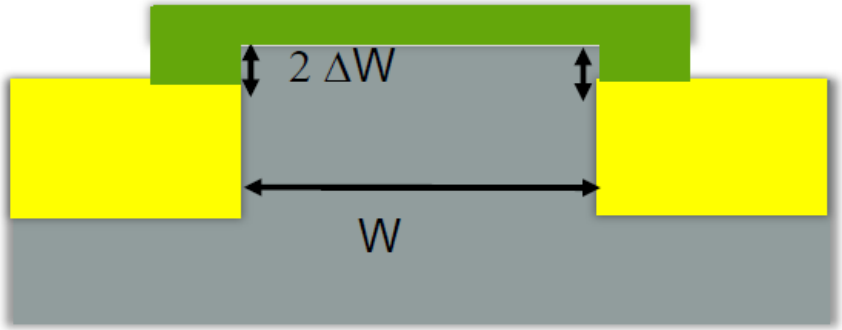
- **Large $W_{ELECTRICAL}$**



Top down planer transistor

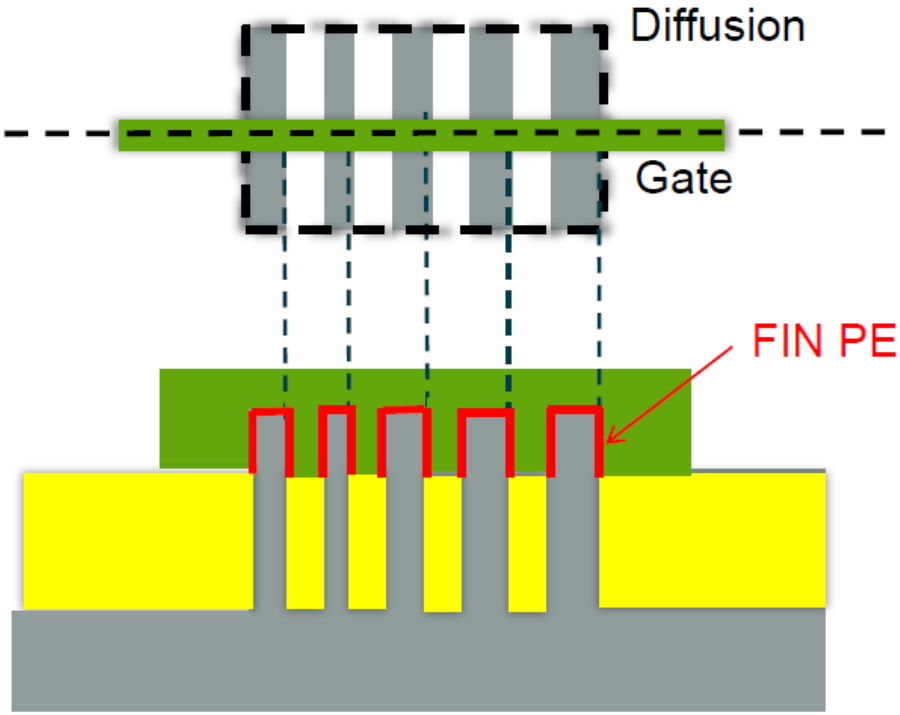


Xsection planer transistor



$W_{ELECTRICAL} = W + 2\Delta W$

FinFET: Key Advantage



Cut Diffusion into strips

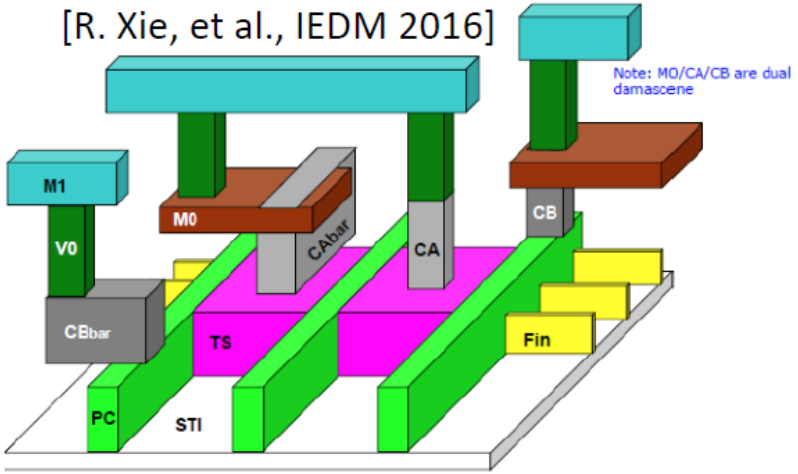
Recessed STI to set Fin Height

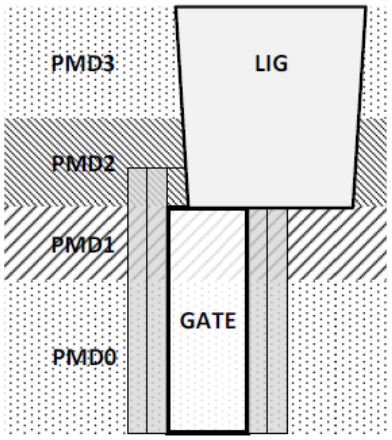
$$W_{ELECTRICAL} = FIN_{PERIMETER} = \#FINS\left(2FIN_H + FIN_W\right)$$

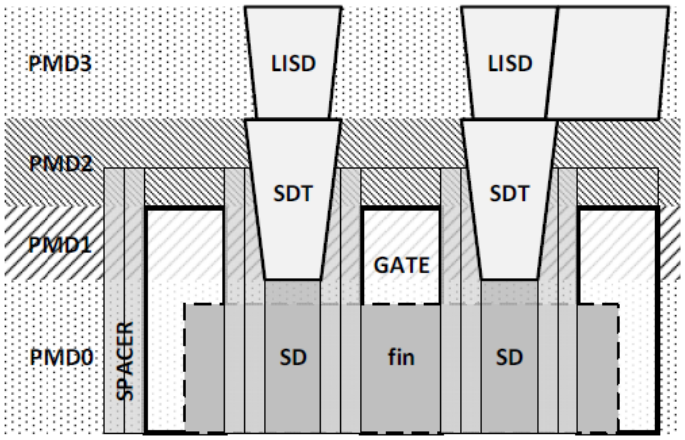
$$W_{ELECTRICAL} = \frac{PLANAR_{WIDTH}}{FIN_{PITCH}}\left(2FIN_H + FIN_W\right)$$

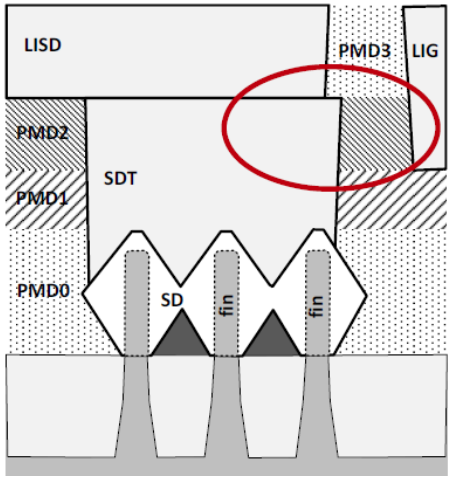
FEOL and MOL Cross Sections

- **Source-drain trench (SDT)**
  - Connects raised source-drain (SD) to MOL
  - Self-aligned to gate spacers
- **LISD**
  - Connects SD to M1 thru V0
- **LIG**
  - Connects Gate to M1 thru V0

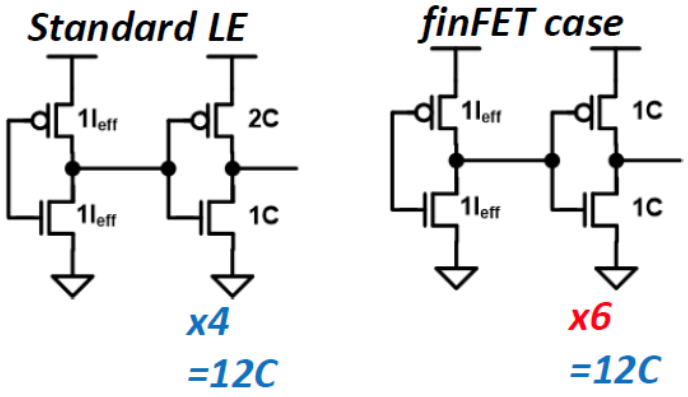


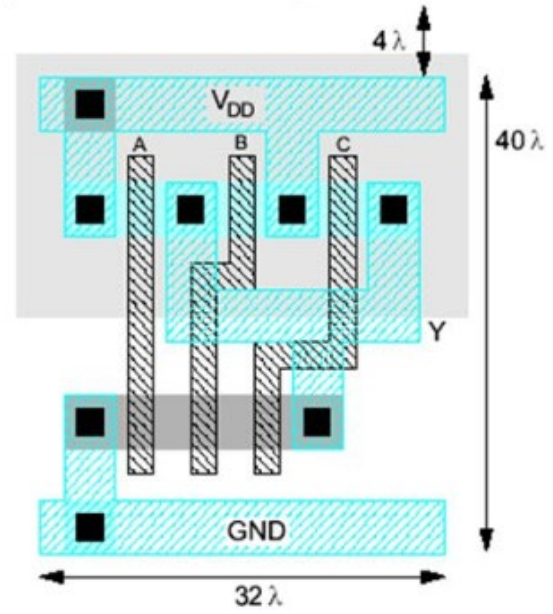


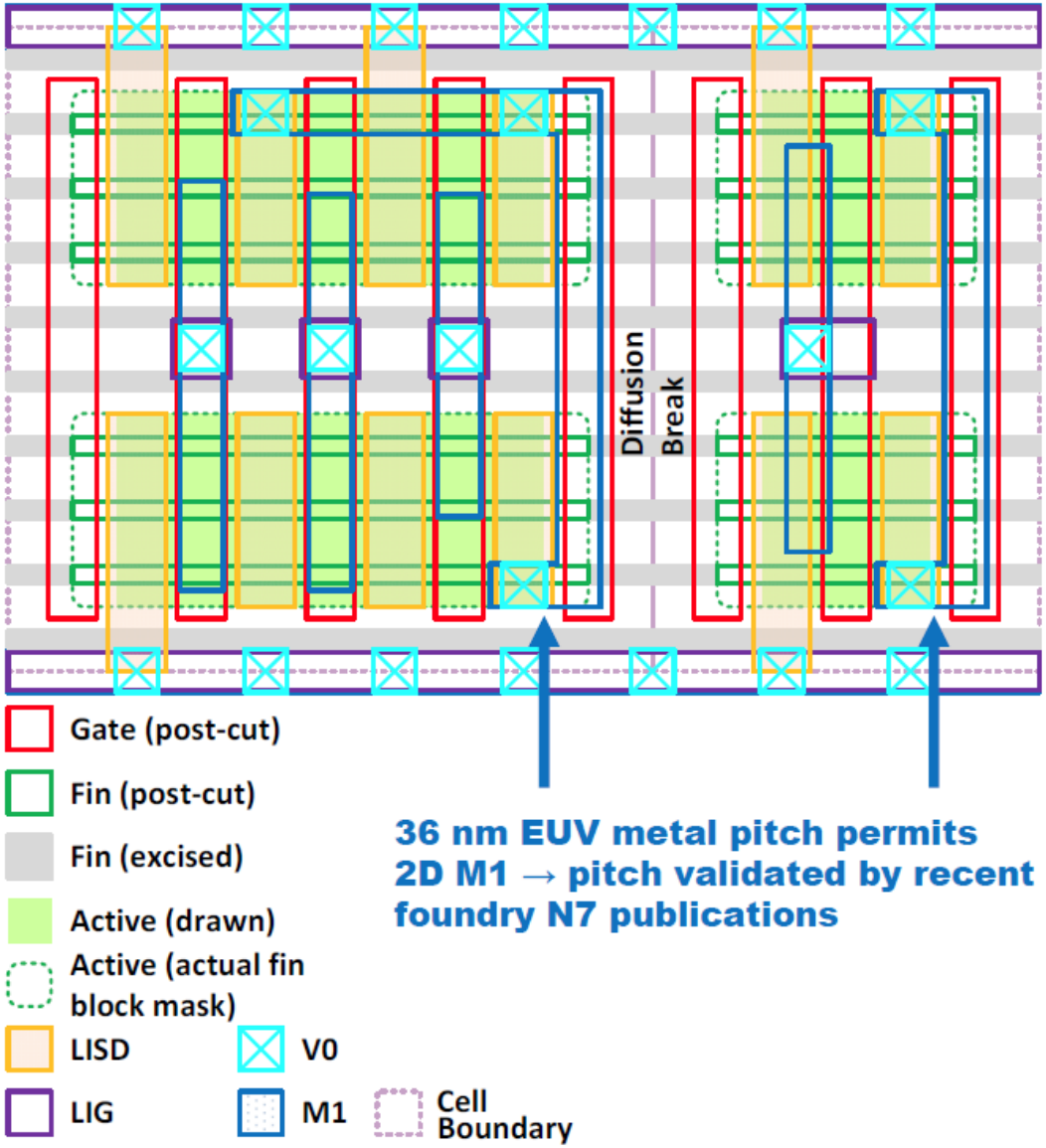




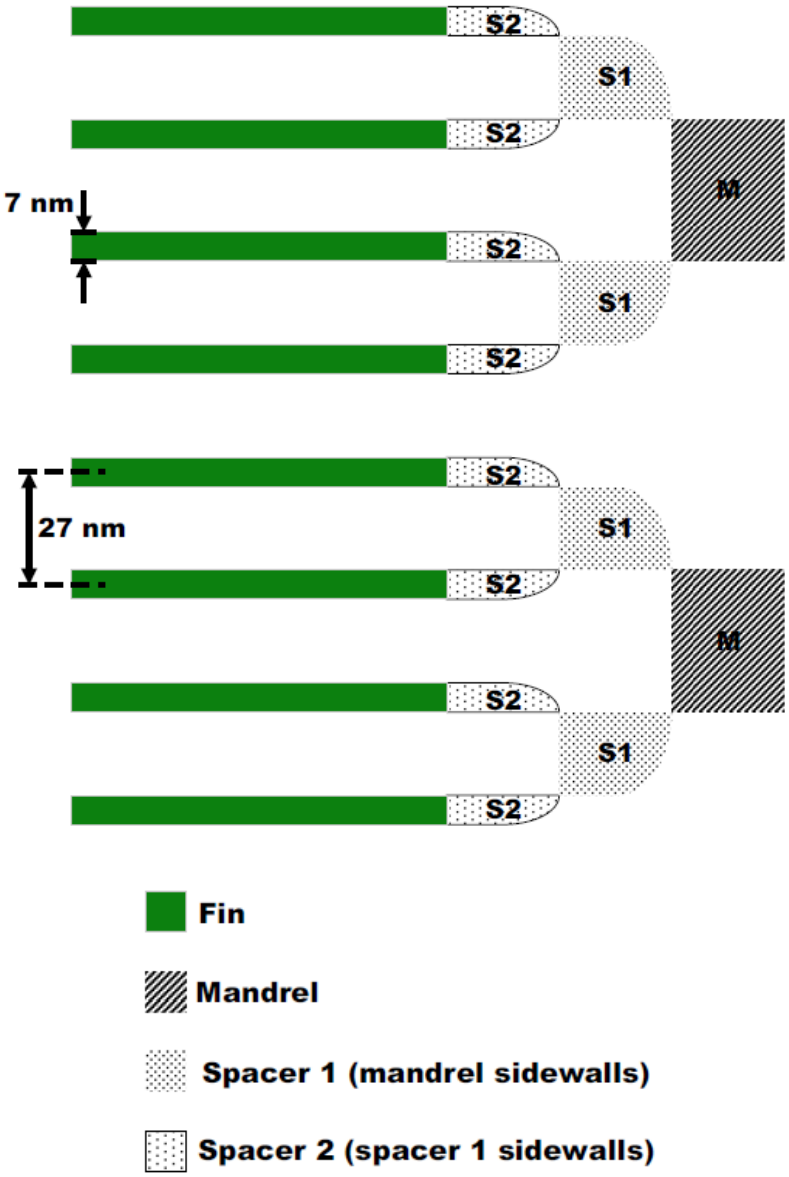
Standard Cell Architecture and Cross-section

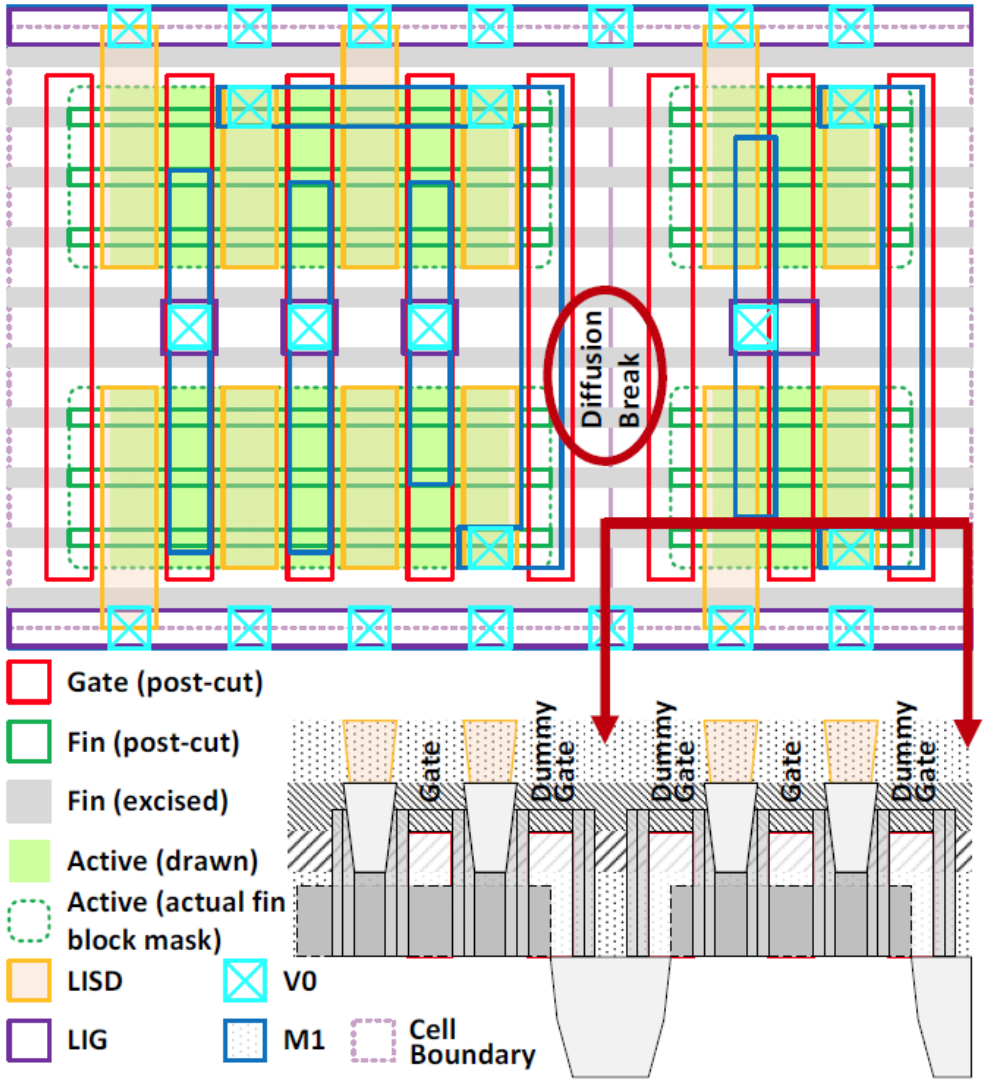




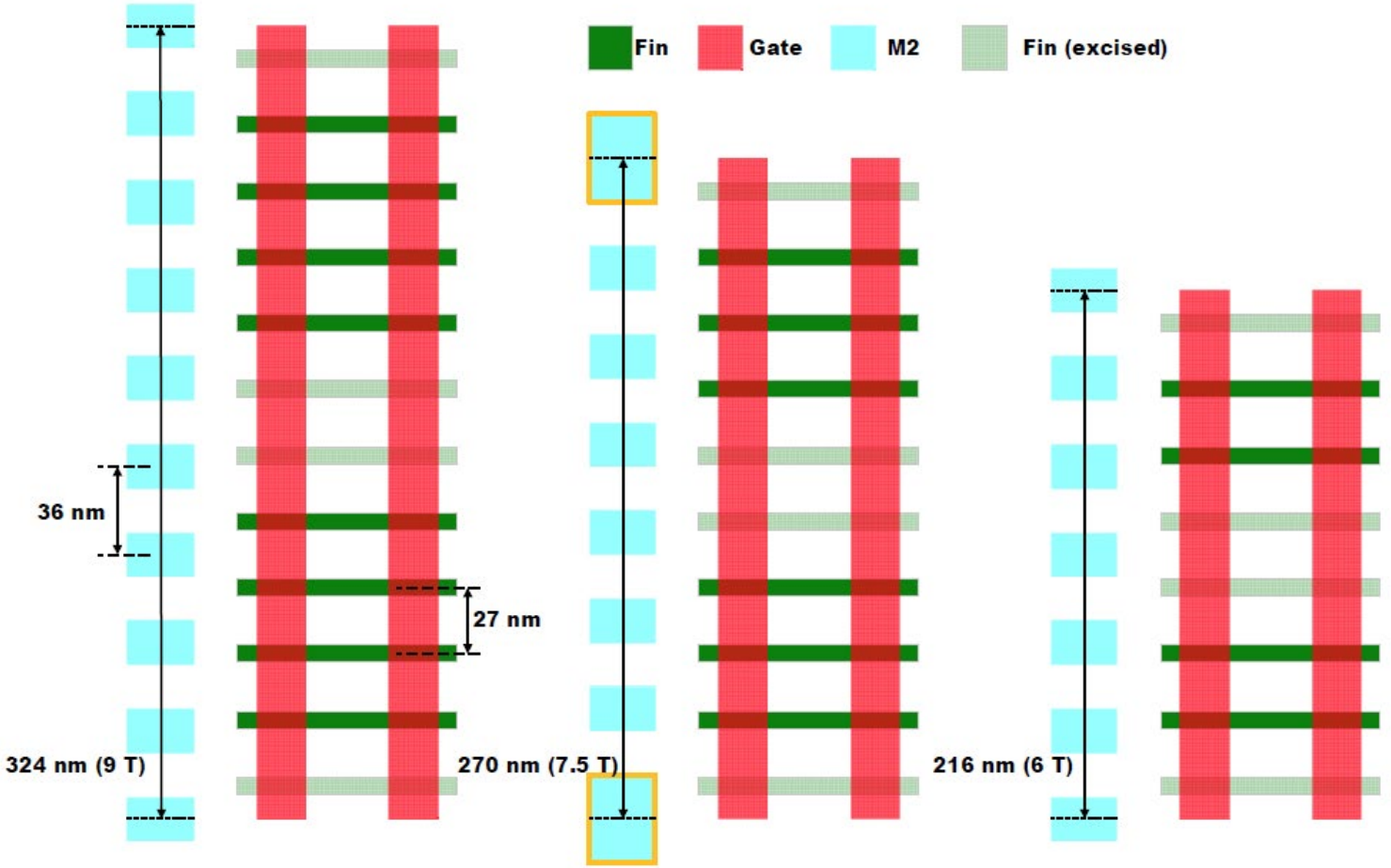


Diffusion Break





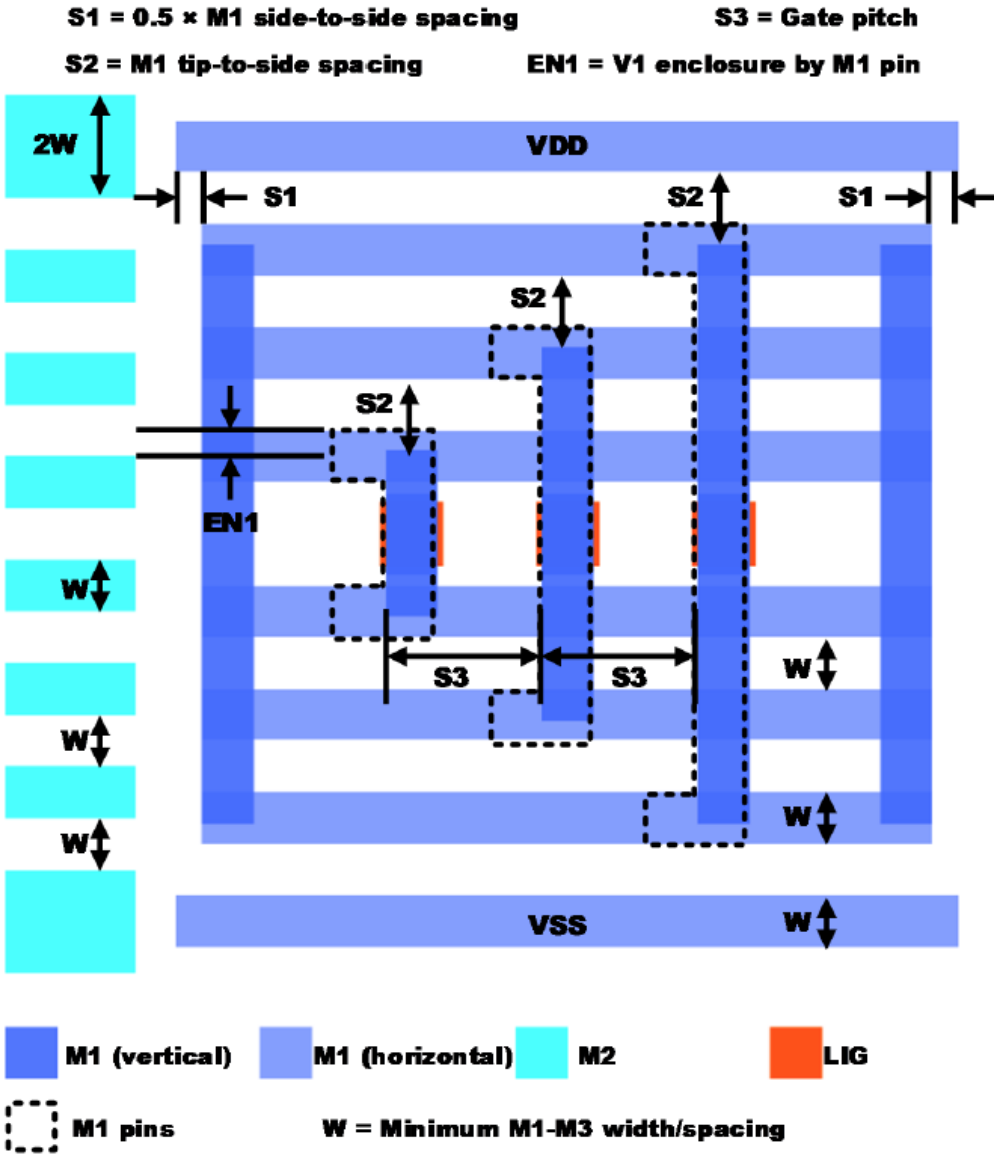
Cell Height in FinFET



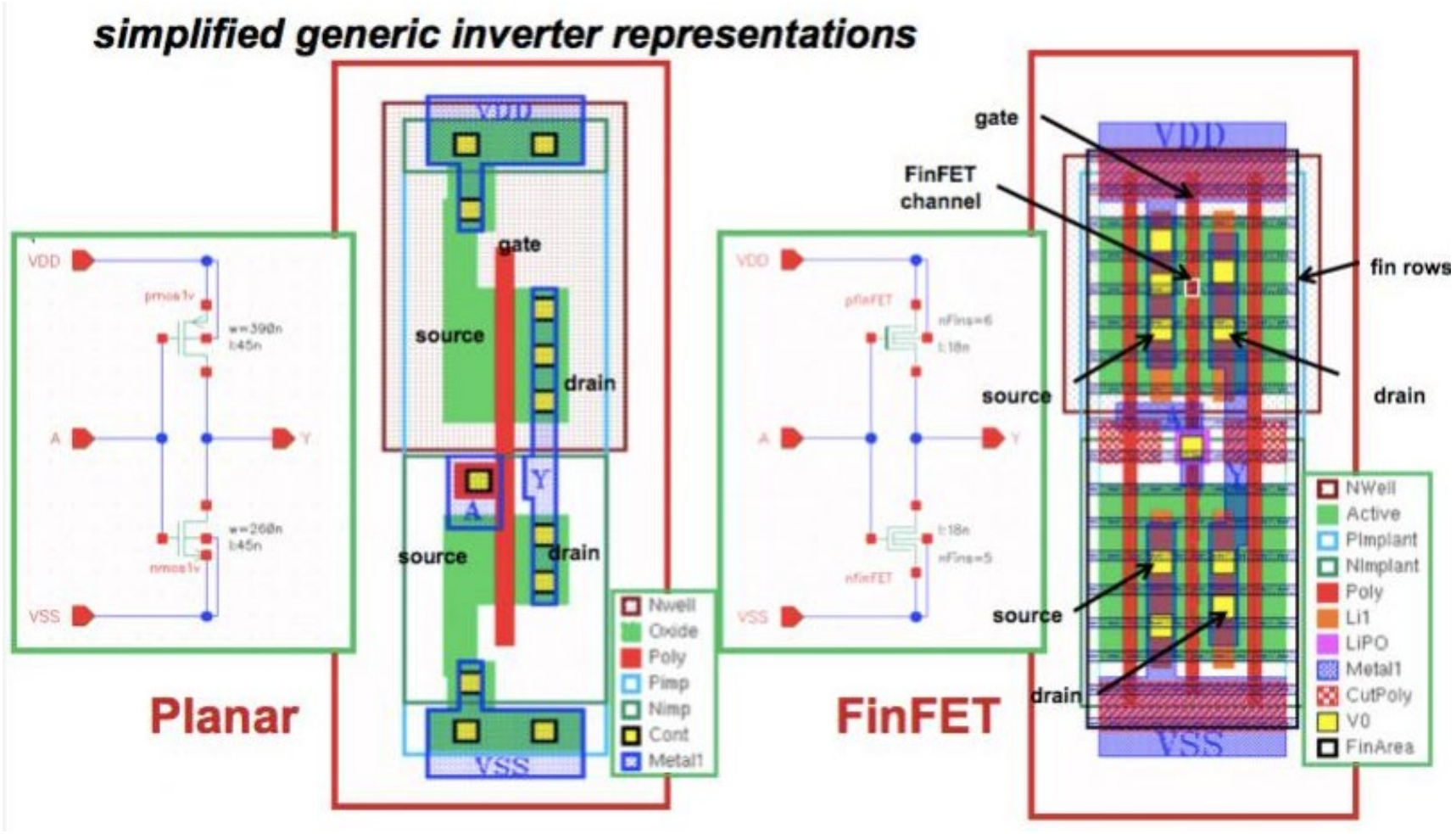
- 12 fin pitches, 9 M2 tracks
  - Easy intra-cell routing, rich library
  - Wasteful for density
- 10 fin pitches, 7.5 M2 tracks
  - Rich library without overly difficult routing or poor density
  - Allows wide M2 power rails
- 8 fin pitches, 6 M2 tracks
  - Difficult intra-cell routing, diminished library richness
  - Limited pin access

Standard Cell M1 Template

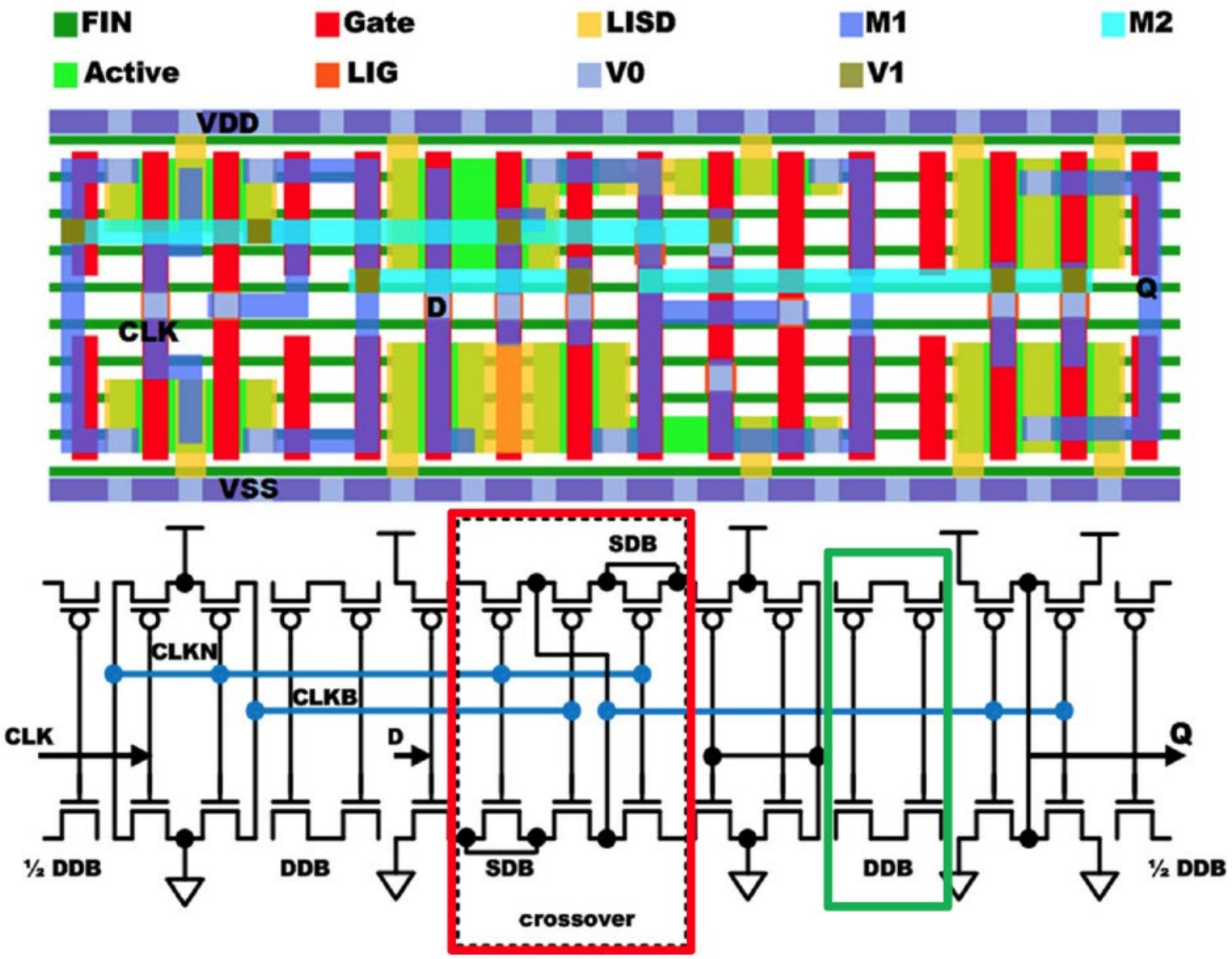
- M1 template enables rapid cell
- library development
  - –Larger M1 spacing at the center
    - Better pin access through M1 extension past M2 tracks
- C-shaped M1 pins
  - Avoid large tip-to-side design rules
  - Maximize pin access
  - No longer necessary on all pins



Planer to FinFET Layout Difference



Standard Cells: Latch



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