Memory Circuits & Systems

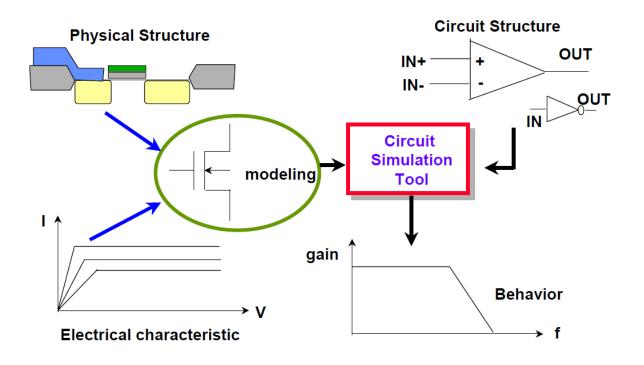
Design Tools HSPICE

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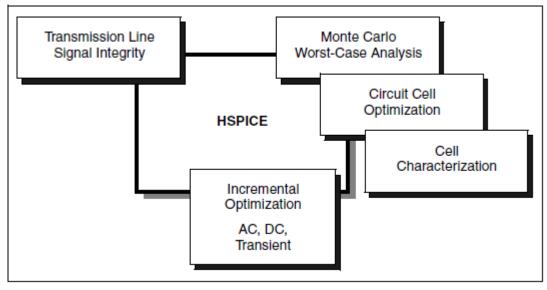
SPICE overview

- SPICE : Simulation Program with Integrated Circuit Emphasis
- Simulation : To predict the Circuit/System Characteristic after manufacturing
- Circuit simulation:



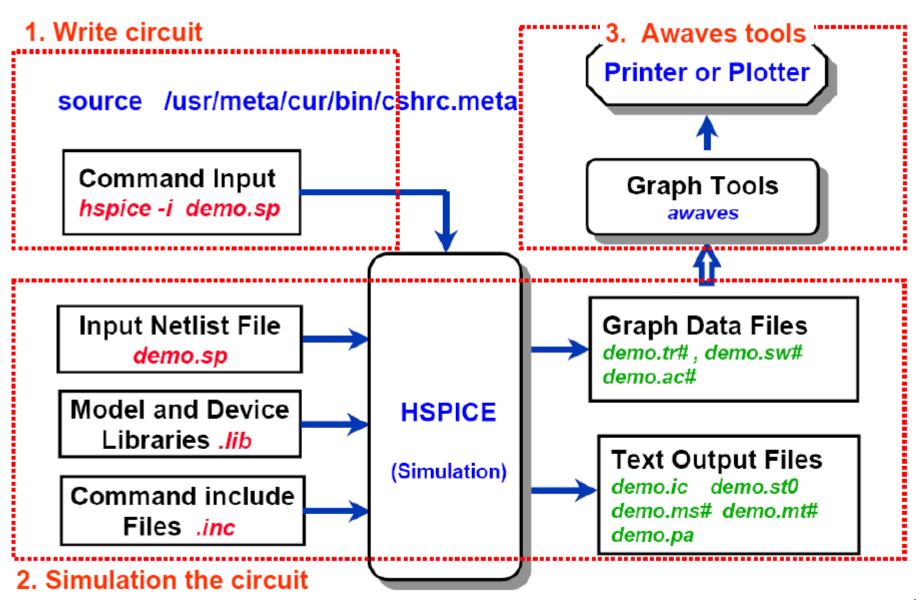
HSPICE Overview

- Synopsys HSPICE is an optimizing analog circuit simulator.
 - ◆ To simulate electrical circuits in steady-state, transient, and frequency domains.
 - ◆ Analysis of performance and yield, by using Monte Carlo, worst-case, parametric sweep, and data-table sweep analyses



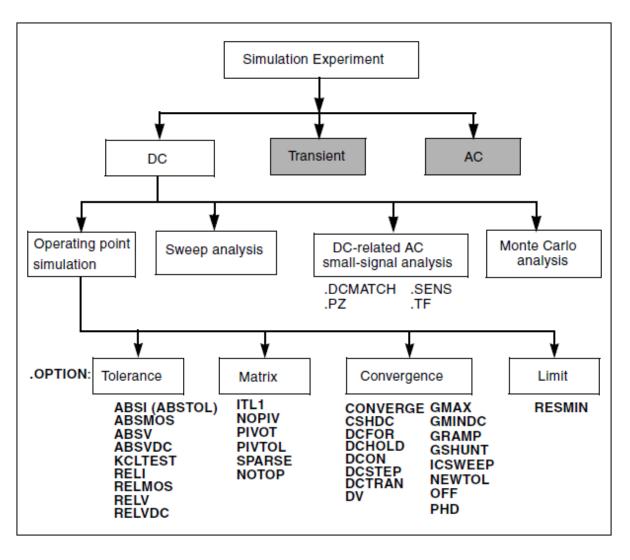
Sourced from: HSPICE® User Guide C-2009.03

HSPICE Data Flow



Simulation Modes

Transient / DC Analysis / AC analysis



Netlist Structure for Spice

```
Title ----→ Title Statement - Ignored during simulation
Models & Subckts ---→ .model... or .LIB or .Subckt
Components ----> c2 2 0 2pf
r1 1 0 1k
m1 1 2 3 4 mod L=10u W=30u
               ---> x3 2 3 INV
L = - > vin in 0 sin(0 2 10k 0.5 0)
Controls ----\rightarrow .option nomod nopage
             tran 1 10
                 .print v(5) i(r1)
             --- .plot v(3) v(in)
End file ----\rightarrow .end
```

Netlist Structure

```
.TITLE Hspice tutorial
****** hspice simulation options
.option post nomod brief measdgt=7 captab
****** process and temperature options
.include '65nm bulk.pm'
.temp 25
.global VDD GND
****** parameters
.param supply=1v
.param wp=0.2u
.param wn=0.08u
.param slew=30p
******* input / voltage sources
vs vdd gnd supply
vin tin gnd pulse(0 supply 0.5n slew slew 0.47n 1n)
****** circuit
MM0 OUT IN VDD VDD PMOS W=wp L=0.065u M=1.0
MM1 OUT IN GND GND NMOS W=wn L=0.065u M=1.0
****** hspice simulation modes
.tran 1p 5n *sweep width 0.045u 0.2u 0.001u
****** measurements
.meas tran Tdr Trig v(in) val='0.5*supply' rise=2
            Targ v(out) val='0.5*supply' fall=2
.meas tran Tdf Trig v(in) val='0.5*supply' fall=2
            Targ v(out) val='0.5*supply' rise=2
```

.end

- Case insensitive!
- .TITLE
- .include / .lib
- .option
 - ◆ post
 - ◆ measdgt=7
 - ◆ captab
- .temp
- global .
- param .
- end .end

7

Library Input Statement

Include Statement

.Include '\$installdir/parts/ad'

Lib Definition and Call Statement

```
.Lib TT <-- Corner name
.Model nmos_tt nmos (level=49
Vt0=0.7+TNOM=27 .....)
.ENDL TT
```

.Lib '~users/model/tsmc/logic06.mod' TT

■ PROTECT <--Prevent the listing of included content
.LIB '~users/model/tsmc/logic06.mod'' TT
.UNPROTECT

Element Identifier & Scale Factors

First Letter	Element
С	Capacitor
D	Diode
1	Current Source
L	Linear Inductor
M	MOS transistor
Q	Bipolar transistor
R	Resistor
V	Voltage Source
X	Subcircuit call

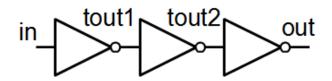
Prefix	Scale Factor Symbol	Factor
tera	Т	1e+12
giga	G	1e+9
mega	Meg	1e+6
kilo	k	1e+3
milli	m	1e-3
micro	U	1e-6
nano	n	1e-9
pico	p	1e-12
femto	f	1e-15
atto	a	1e-18

Element Syntax

- Case insensitive!
- Passive components
 - ◆ Rxxx node1 node2 value
- ◆ C, L, etc.
 ♦ ex, r1 1 2 10k 2
 R1 10k 1
 C1 5p in out
 Active component
 - ◆ Mxxx Drain Gate Source Bulk Model width length <multiple>
 - ex.
 mtest1 out in vdd vdd pmos w=195n l=65n m=1
 mtest2 out in gnd gnd nmos w=65n l=65n m=1

Subcircuit

- .SUBCKT NAME Node1 <Node2 ...> <param1 ...> circuit description
 - .ENDS
- Subcircuit call
 - ◆ Xxxx Node1 <Node2 ...> NAME <param1 ...>



.global VDD GND

********************** circuit

MM0 tout1 IN VDD VDD PMOS W=195n L=65n MM1 tout1 IN GND GND NMOS W=65n L=65n

MM2 tout2 tout1 VDD VDD PMOS W=390n L=65n MM3 tout2 tout1 GND GND NMOS W=130n L=65n

MM4 out tout2 VDD VDD PMOS W=780n L=65n MM5 out tout2 GND GND NMOS W=260n L=65n

.SUBCKT INV IN OUT wp=195n wn=65n MM0 OUT IN VDD VDD PMOS W=wp L=65n MM1 OUT IN GND GND NMOS W=wn L=65n .ENDS

.global VDD GND

****** circuit

X0 IN tout1 INV X1 tout1 tout2 INV wp=390n wn=130n X2 tout2 OUT INV wp=780n wn=260n

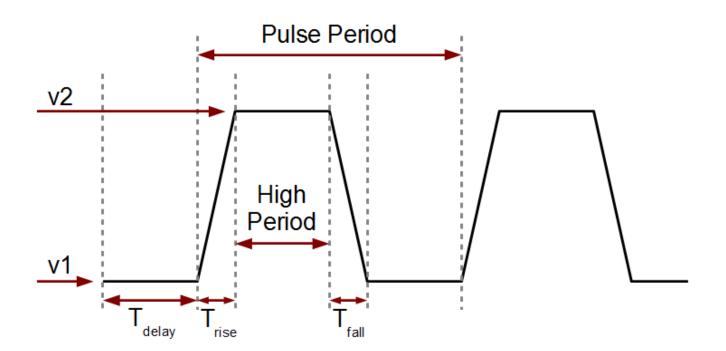
.end

Independent Voltage and Current Sources

- Vxxx n+ n- [DC=] dcval tranfun [AC=acmag acphase]
 - ◆ v1 1 0 DC=5v
 - ♦ v2 2 0 5v
- Ixxx n+ n- [DC=] dcval tranfun [AC=acmag acphase]
 - ♦ i3 3 0 5mA
- tranfun
 - lacktriangle PULSE(v1 v2 T_{delay} T_{rise} T_{fall} $P_{high-width}$ P_{period})
 - ◆ PWL(t1 v1, <t2 v2, t3 v3...> <R<=repeat>> <TD=delay>)
 - ◆ SIN(V_{offset} V_{acmag} <Freq T_{delay} Dfactor>)
 - ◆ Exponential

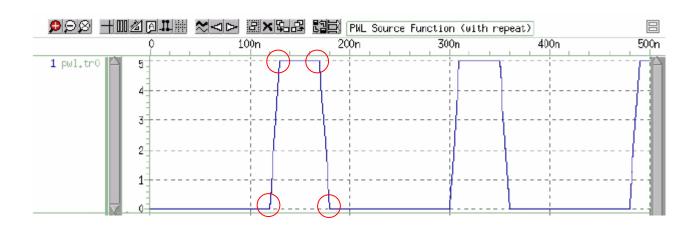
Pulse Voltage Source

- Vxxx node1 node2 PULSE(v1 v2 T_{delay} T_{rise} T_{fall} P_{high-width} P_{period})
- Vin 1 0 PULSE(0v 5v 5ns 2ns 2ns 5ns 14ns)



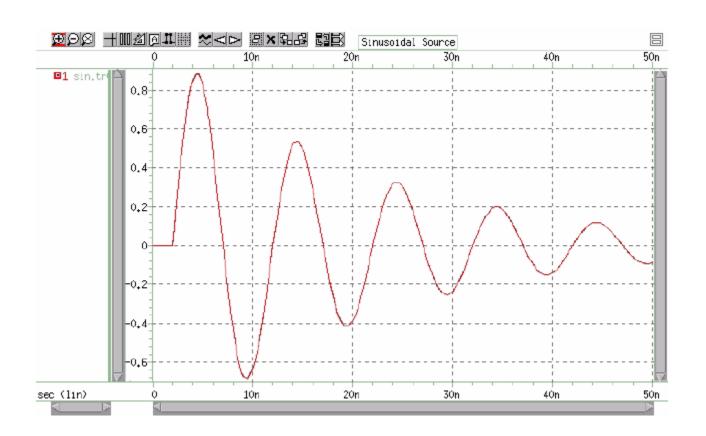
Piecewise linear (PWL) Voltage Source

- Vxxx node1 node2 PWL(t1 v1, <t2 v2, t3 v3...> <R<=repeat>> <TD=delay>)
- v1 1 0 pwl(60n 0v, 120n 0v, 130n 5v, 170n 5v, 180n 0v, R 0)



Sinusoidal Voltage Source

- Vxxx node1 node2 SIN($V_{offset} V_{acmag} < Freq T_{delay} D_{factor} >$)
- VIN 3 0 SIN(0 1 100meg 2ns 5e7)



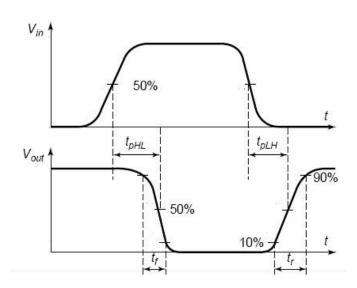
Transient Analysis

- .tran <timestep> <total simulation time>
- sweep <variable> <start value> <end value> <step>
- .tran 1p 5n
- .tran 1p 5n sweep temp 0 25 5

- dc.
- .ac
- HSPICE® User Guide: Simulation and Analysis

Measurements

- .meas(ure) <mode> <name> <type description>
- .meas tran TpHL Trig v(in) val=0.5V rise=2
- Targ v(out) val=0.5V fall=2
- .meas tran TpLH Trig v(in) val='0.5*supply' fall=2
- Targ v(out) val='0.5*supply' rise=2



Measurements

- .meas(ure) <mode> <name> <type description>
- Mode
 - ◆ DC / AC / TRAN
- Type
 - ◆ Trig, Targ / AVG / MAX / MIN / PP
- .measure dc vout find V(out1) when V(in)=0.9
- .measure tran Pavg avg I(out) from=5n to=50n
- Measured results are listed in .mt# file

Multiple Analyses

.alter

- Simulation all over again using new parameters
- .mt0 .mt1 .mt2 etc.
- ◆ .tr0 .tr1 .tr2 etc.

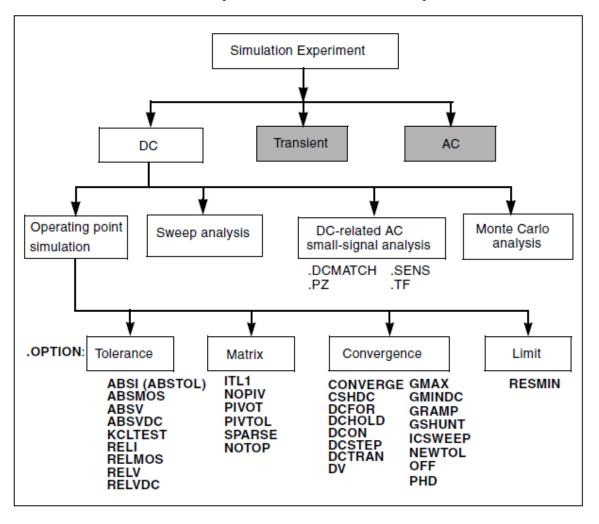
.sweep

- ◆ Simulation using new parameters but with the same initial point
- ◆ All in the same .mt0/.tr0

```
********************************* process and temperature options
.temp 25
****** parameters
.param supply=1v
.param wp=0.2u
.param wn=0.08u
.param slew=30p
****** hspice simulation modes
.tran 1p 5n *sweep temp 0 25 5
****** measurements
.meas tran Tdr Trig v(in) val='0.5*supply' rise=2
              Targ v(out) val='0.5*supply' fall=2
.meas tran Tdf Trig v(in) val='0.5*supply' fall=2
              Targ v(out) val='0.5*supply' rise=2
.alter
.param supply=0.5v temp=25
.alter
.param supply=0.5v temp=50
.end
```

Simulation Modes

Transient / DC Analysis / AC analysis



DC Operating Point Analysis

- Initialization and analysis
 - ◆ First thing to set the DC operating point values for all nodes and sources : set capacitors OPEN & inductors SHORT
 - ◆ Using .IC or .NODESET to set the Initialized Calculation
- OP statement print:
 - ◆ Node Voltages
 - Source Currents
 - Power Dissipation
 - Semiconductors Device Currents, Conductance, Capacitance

DC Sweep & DC Small Signal Analysis

.DC Analysis : Syntax

```
.DC var1 start1 stop1 incr1 < var2 start2 stop2 incr2 > )
.DC var1 start1 stop1 incr1 <SWEEP var2 DEC/OCT/LIN/POI np start2 stop2 >)
```

Examples

```
.DC VIN 0.25 5.0 0.25
.DC VDS 0 10 0.5 VGS 0 5 1
.DC TEMP -55 125 10
.DC TEMP POI 5 0 30 50 100 125
.DC xval 1K 10K 0.5K SWEEP TEMP LIN 5 25 125
.DC DATA=datanm SWEEP par1 DEC 10 1K 100K
.DC par1 DEC 10 1K 100K SWEEP DATA=datanm
```

AC Sweep & AC Small Signal Analysis

.AC Analysis : Syntax

```
.AC DEC/OCT/LIN/POI np fstart fstop
.AC DEC/OCT/LIN/POI np fstart fstop < SWEEP var start stop incr >
```

Examples

```
.AC DEC 10 1K 100MEG

.AC LIN 100 1 100Hz

.AC DEC 10 1 10K SWEEP Cload LIN 20

.AC DEC 10 1 10K SWEEP Rx POI 2 5K 15K

.AC DEC 10 1 10K SWEEP DATA=datanm
```

Transient Analysis

.TRAN Analysis : Syntax

```
.TRAN tincr1 tstop1 <tincr2 tstop2 ...> <START=val>
.TRAN tincr1 tstop1 <tincr2 tstop2 ...> <START=val> UIC <SWEEP...>
```

• Examples :

- . TRAN 1NS 100NS
- TRAN 10NS 1US UIC
- . TRAN 10NS 1US UIC SWEEP TEMP -55 75 10 \$ step=10
- .TRAN 10NS 1US SWEEP load POI 3 1pf 5pf 10pf
- . TRAN DATA=datanm

Measurements(1/2)

- .meas(ure) <mode> <name> <type description>

 - ◆ Type

 Find, when/ AVG / MAX / MIN / Trig, Targ / PP
- EX1:
 - .meas dc vout find V(out1) when V(in)=0.9
- Ex2:
 - ◆ .meas tran Pavg avg I(out) from=5n to=50n
- Ex3:
 - .meas pwr avg POWER

Measurements(2/2)

• EX3:

results are listed in .mt# file

Output Files Summary (HSPICE)

Output File Type	ExTensi
Output Lis	.lis #
DC Analysis Results	.sw #
DC Analysis Measurement Results	.ms #
AC Analysis Results	.ac #
AC Analysis Measurement Results	.ma #
Transient Analysis Results	.tr #
Transient Analysis Measurement Results	.mt #
Subcircuit Cross-Listing	.pa #
Operating Point Node Voltages (Initial Condition)	.ic

Output Statement

- Output Commands :
 - .PRINT : Print Numeric Analysis Results
 - .PLOT : Generates Low Resolution Plot in .lis file
 - PROBE : Allows Save Output Variables Only into the Graph Date Files
- MEASURE : Print Numeric Results of Measured Specifications

Hspice Execution Command

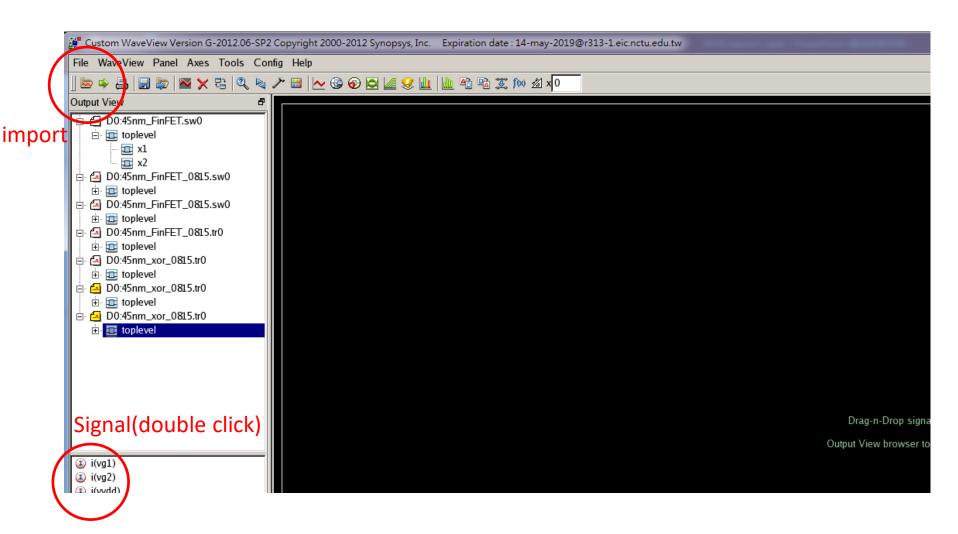
- HSPICE
 - ◆ %> hspice NETLIST.sp >NETLIST.lis
 - ◆ It will show Job Conclude!(or Job Abort!)
 - ◆ If abort, please see the result file(.lis) to find out the error

```
[smillims1212@r313-1 ~/20180813]$ hspice 45nm_xor_0815.sp > 45nm_xor_0815.lis
>info: ***** hspice job concluded
```

◆ %> hspice −i NETLIST.sp −o NETLIST.lis

WaveView for Graphical Waveform

■ %> wv &



Digital Vector File

- Vector Pattern Definition Section
 - ◆ Define Name 、 Magnitude 、 I/O 、 Time unit of stimulus
- Waveform Characteristic Section
 - ◆ Define Rise/Fall time ➤ Threshold voltage of signals
- Tabular Data Section
 - ◆ Define different logic level with corresponding time of stimulus

Vector Pattern

Syntax:

Radix XXXX XXXX Vname name[7:0] 10 XXXX XXXX Tunit ns Period XX Trise XX Tfall XX Tdelay XX Vih xx Vil XX XXXX XXXX XXXX XXXX

XXXX XXXX

```
Example:
```

```
1111 1111
Radix
Vname AAA[7:0]
10
       iiii iiii
Tunit
       ns
Period 10
     0.5
Trise
Tfall
    0.5
Tdelay 1
Vih
        1.0
Vil
       0.0
1010 1001 $ 0ns~ 10ns
0010 0111 $ 10ns~20ns
0110 0001 $ 20ns~30ns
```

Example:

```
Radix 4 4 1
Vname A[3:0] B[3:0] C
       i i i
10
Tunit
        ns
Period
       10
Trise
       0.5
Tfall 0.5
Tdelay
       1
Vih
        1.0
Vil
       0.0
1111 1001 1 $ Ons~ 10ns
0000 1111 1 $10ns~20ns
1111 0111 0 $ 20ns~30ns
```

.vec 'file_name.vec'