Digital IC Design

Exercise 1
Basic Logic Gates

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Exercise 1-1: DC characteristics (25%)

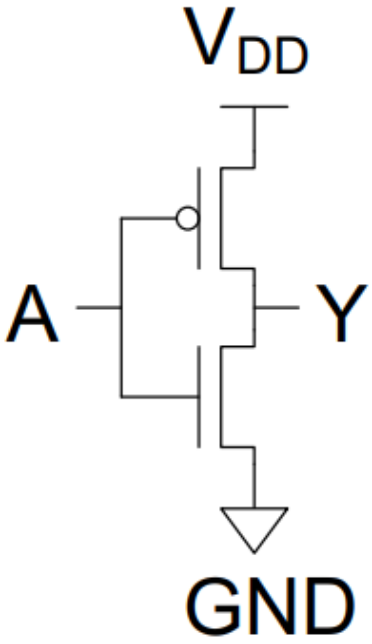
- Simulate DC characteristics of FinFETs and planer MOSs by minimal feature sizes
  - V_{gs}-I_{DS} of FinFET (N-FinFET & P-FinFET) in one figure
    - Number of Fin = 1
    - Vdd = 0.7v
  - V_{gs}-I_{DS} of CMOS (NMOS & P-MOS)in one figure
    - minimal width and Length = 16nm
    - Vdd = 0.7v

Exercise 1-2: Voltage Transfer Curve (25%)

- Select the smallest and largest inverters from ASAP 7nm standard cell library and simulate the voltage transfer characteristic (VTC).
  - Netlist of standard cells: asap7sc7p5t_INVBUF_RVT.sp
  - Plot VTC curves of these 2 inverters under different voltages (Vdd = 0.7V, 0.6V, 0.5V and 0.4V)
- Design unit-sized inverters such that their logic threshold voltage is at $\frac{Vdd}{2}$ (vdd = 0.7v)
  - Plot the VTC curve
    - Using FinFETs (7nm_TT.pm)
    - Using Planer MOSs (16mos.pm)

Exercise 1-3: Power consumption (25%)

- Measure the power consumption of the inverters, designed in 1-2.
  - Input buffer: Buffer.sp
  - Output loading: FO4 (4 inverters) + 10 fF as wire loading
  - Vdd = 0.7v
  - Input pattern need more than 20.
  - Input signal switching frequency
    - 1GHz
    - 2GHz
    - 4GHz



Exercise 1-4: Characteristics of NOR2/NAND2 (25%)

- Select the smallest **NOR2** and **NAND2** from ASAP 7nm standard cell library
  - Input buffer: Buffer.sp
  - Output loading: FO4 (4 inverters) + 10 fF as wire loading
    - Inverter: smallest inverters in ASAP 7nm standard cell library
  - Netlist of standard cells:
    - asap7sc7p5t_INVBUF_RVT.sp
    - asap7sc7p5t_SIMPLE_RVT.sp
  - Vdd = 0.7v
  - Measure Tr, Tf, Tplh, Tphl

Submission on e3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip)** and upload this single file on E3 platform

- Naming rules of files
  - Upload file: **Ex1_#ID.zip**
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    - Hspice code: **Ex1_1.sp**
      Ex1_2.sp
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- Due date: 10/16 PM 23:55