Digital IC Design

Lec 1: Overview & Design Methodology

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General Information

- **Instructor : Professor Po-Tsang (Bug) Huang**
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  - Office Hours: After class or by appointment @ MIRC 601

- **Regular class hours**
  - Monday 1:20 AM – 4:20 PM

Grading of this Course

- **20% Exercises**
  - On-line choice questions for Each Lecture
- **60% Labs (self-evaluation for your grades)**
  - Tools: Verilog, HSPICE
  - Most exercises are related to circuit-level implementation
- **20% Final Team Project**

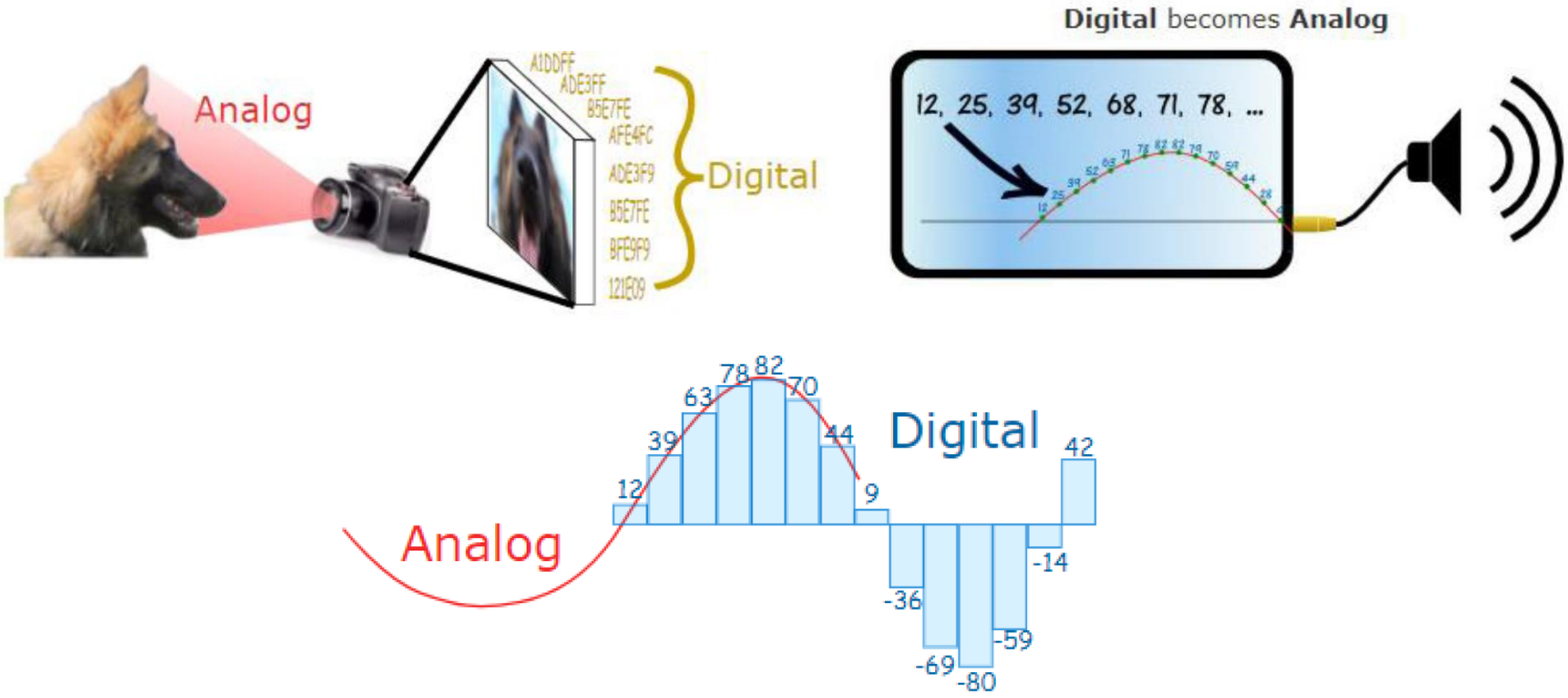
Undergraduate Course v.s. Graduate Course

- **Undergraduate courses (VLSI)**
  - Basic transistor and circuit models
  - Basic circuit design styles
  - First experiences with design – creating a solution with given numbers of specifications

- **Graduate courses**
  - Transistor models of varying accuracy
  - Design under constraints: power-constrained, flexible, robust,…
  - Learning the more advanced techniques
  - Study the challenges facing design in the near future
  - Creating new solutions to challenging design problems

Digital Processing or Digital Computing

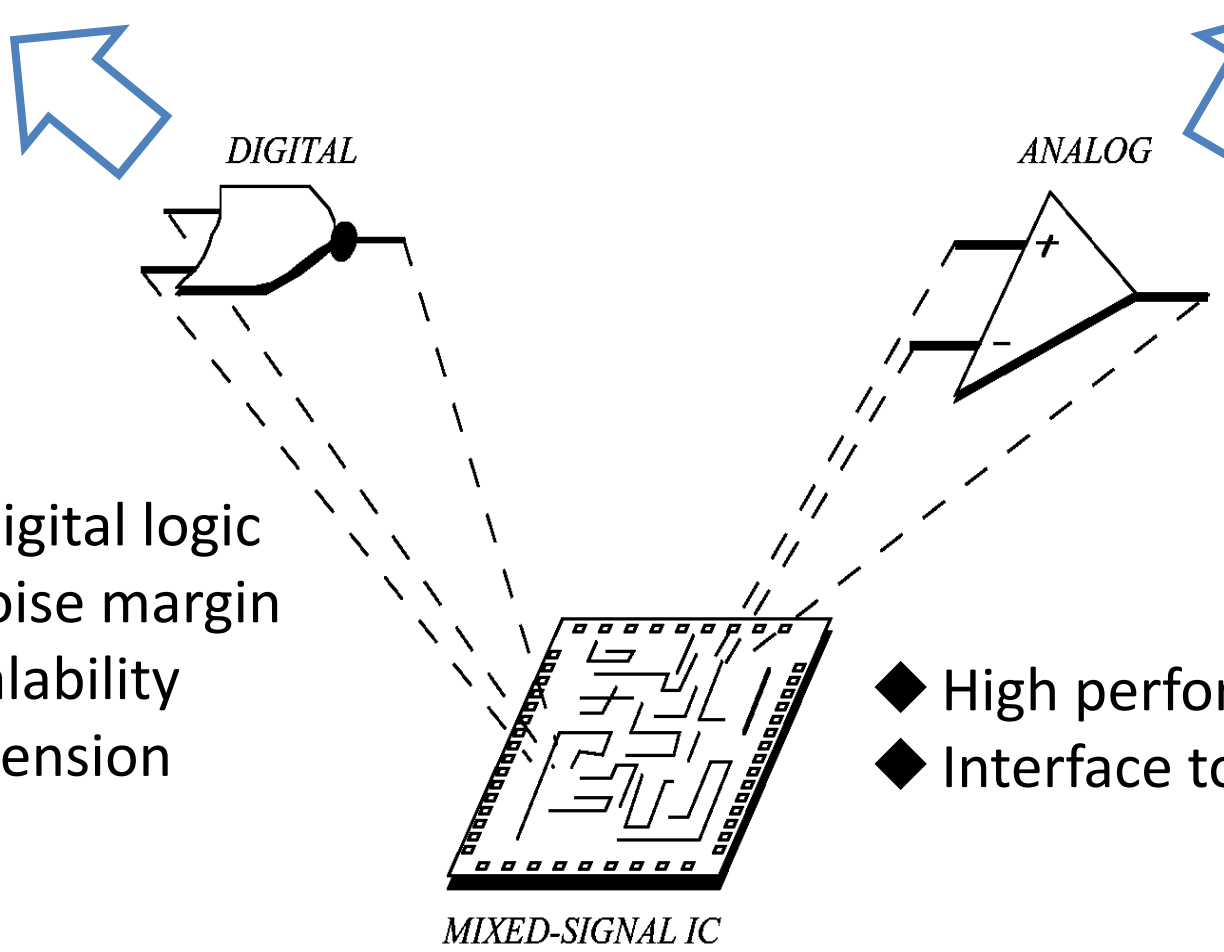
- Analog real world v.s. digital computing system
  - Discrete digital data (binary digits: 0 & 1)



Digital Circuits and Analog Circuits

Software

Sensor, power

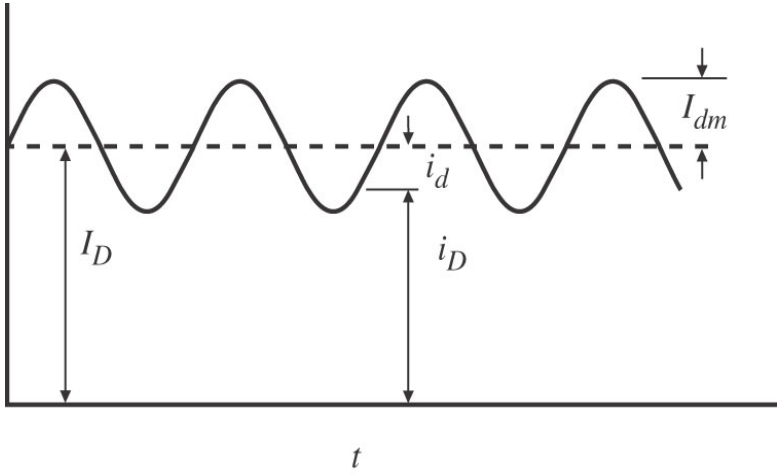


- Dense digital logic
- Large noise margin
- High scalability
- Easy extension

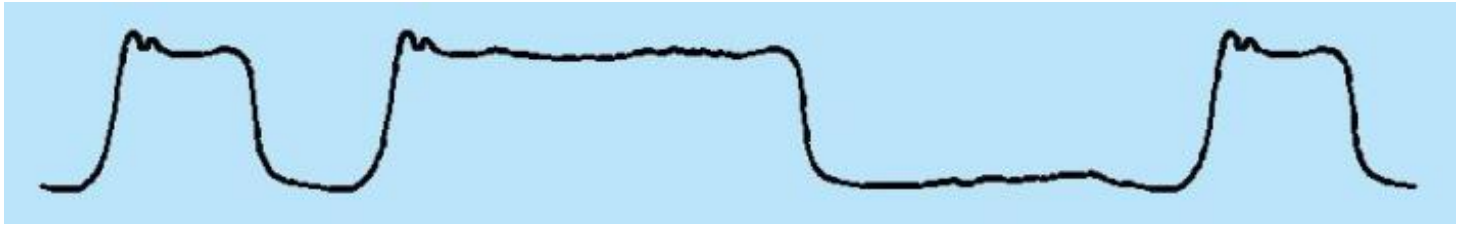
- High performance
- Interface to real world

Signal Characteristics

- Analog signals
  - DC + Small signals

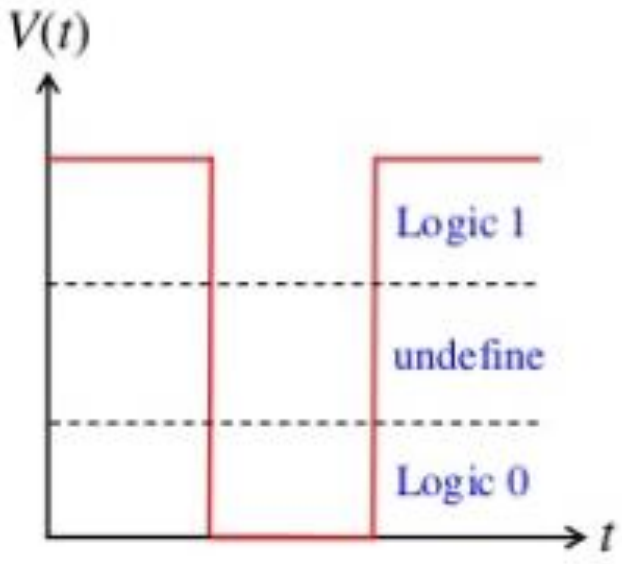


- Digital binary signals
  - 0 & 1



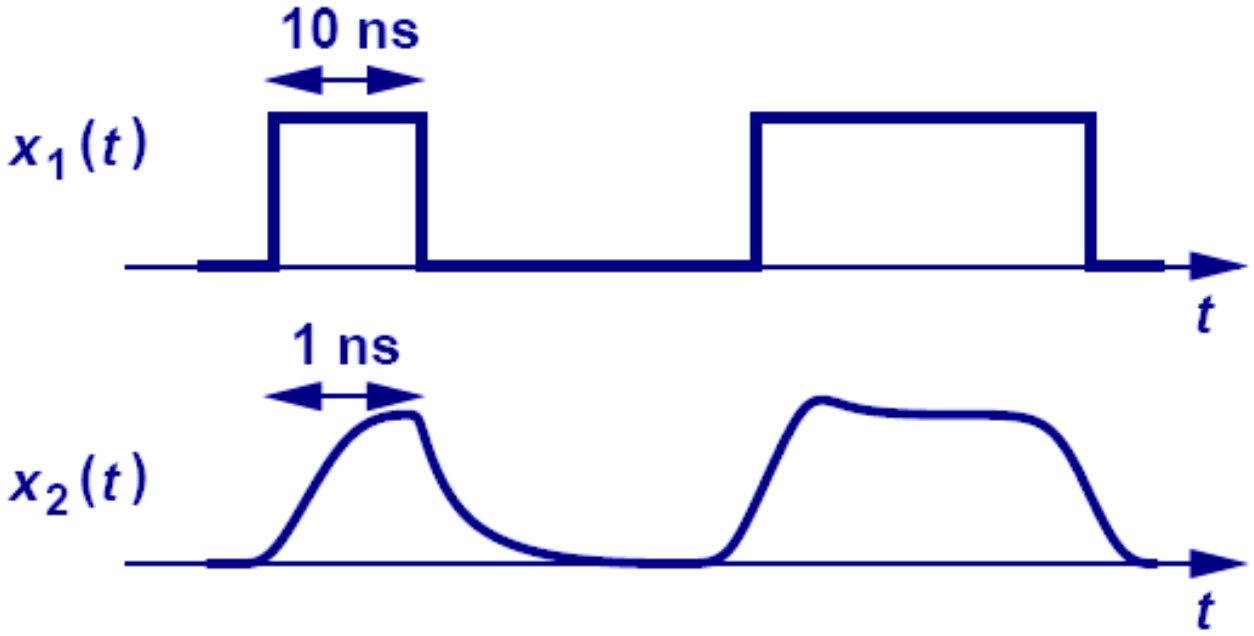
Binary Digital Signal

- **An information variable represented by physical quantity.**
- Binary values are represented abstractly by:
  - Digits 0 and 1
  - Words (symbols) False (F) and True (T)
  - Words (symbols) Low (L) and High (H)
  - And words on and off
- Binary values are represented by ranges of values of physical quantities.



Binary digital signal

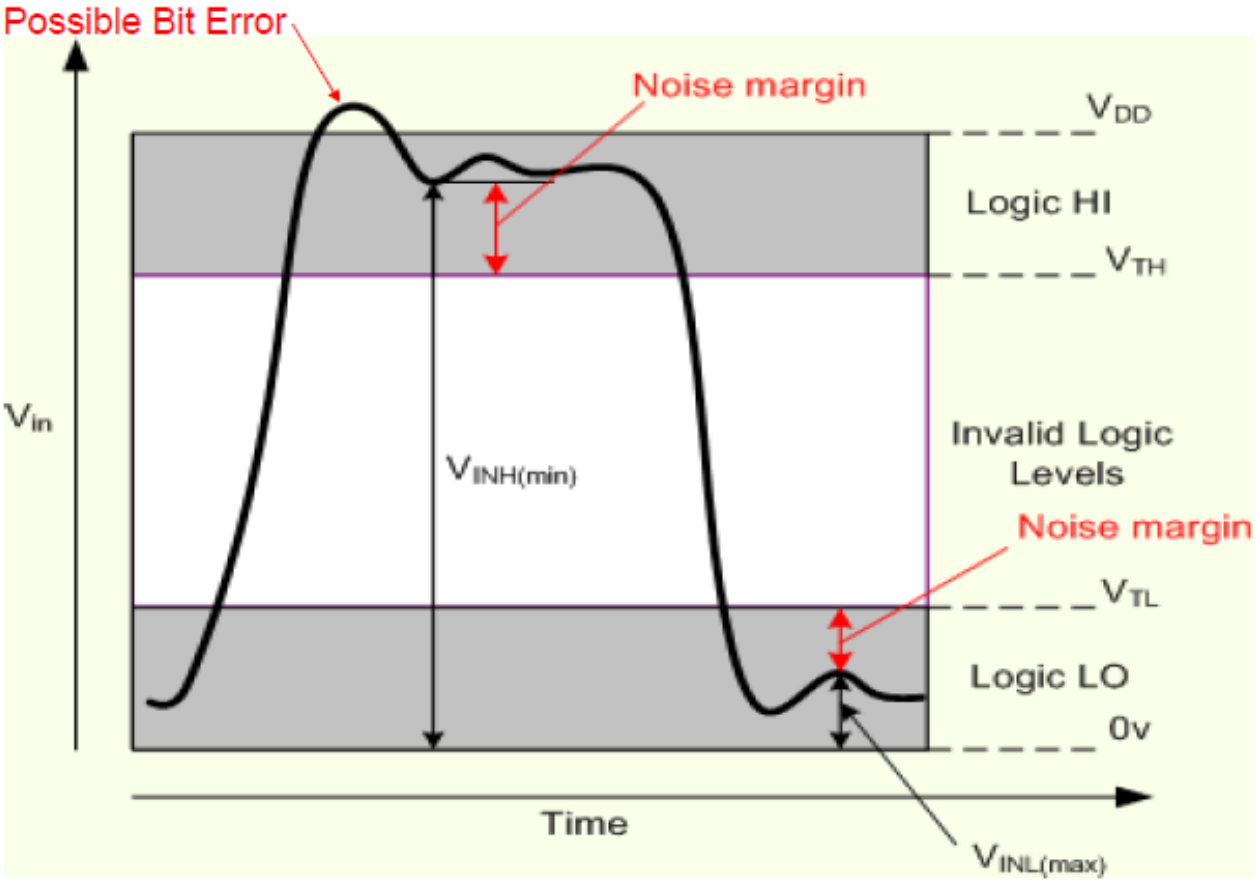
Digital or Analog Signal?



- $X_1(t)$ is operating at 100Mb/s and $X_2(t)$ is operating at 1Gb/s.
- A digital signal operating at very high frequency is very “analog”.

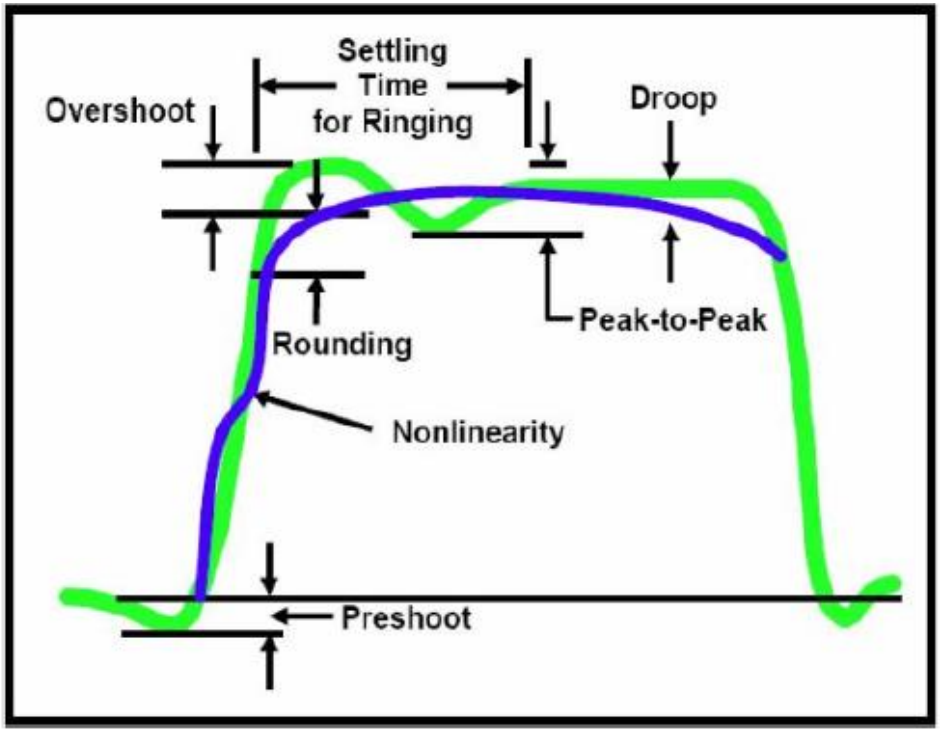
Binary Logic Level

- The signal voltage must make into the “End Zone” within the allotted period of time.

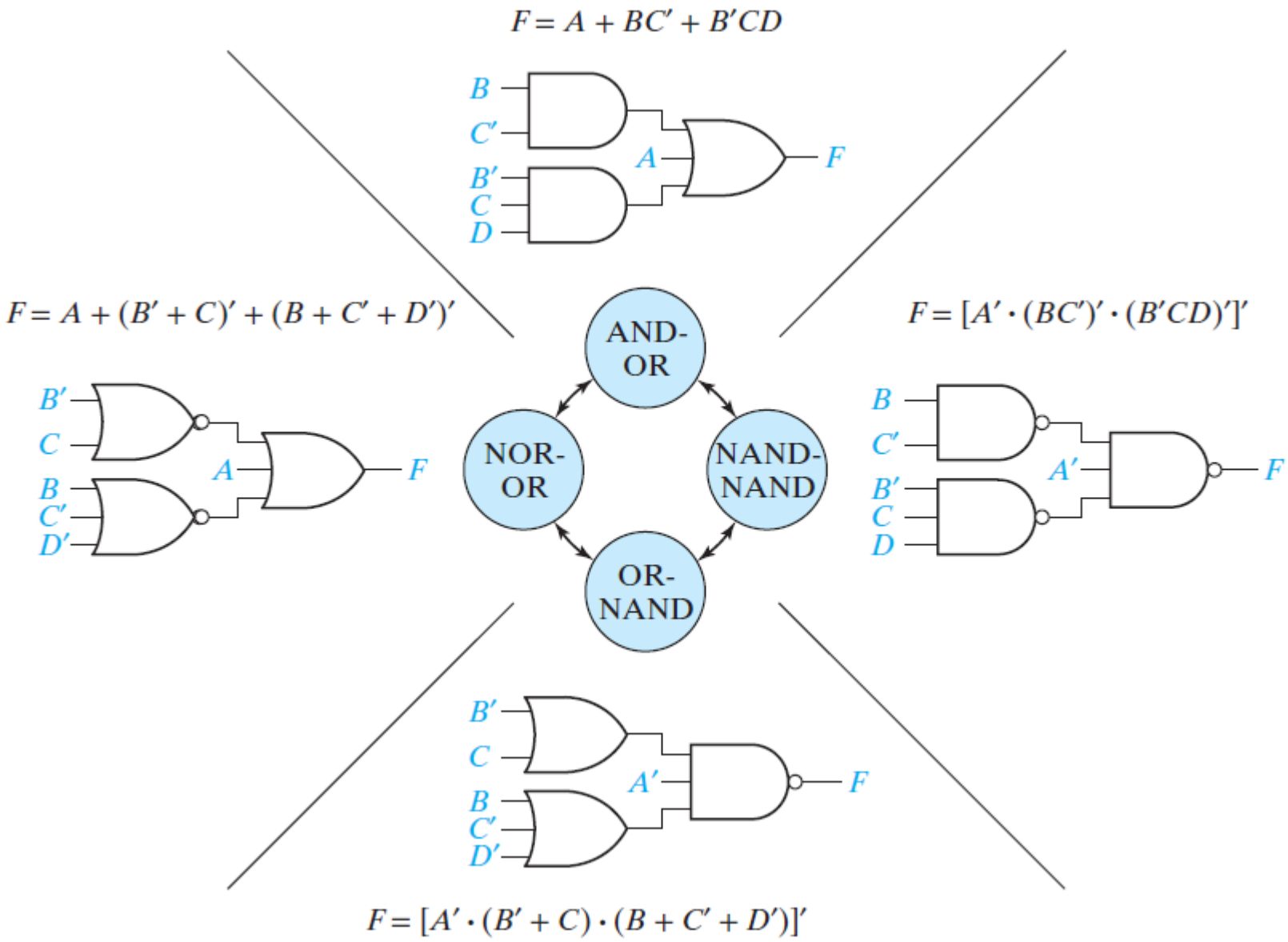


Introduction to Signal Aberration

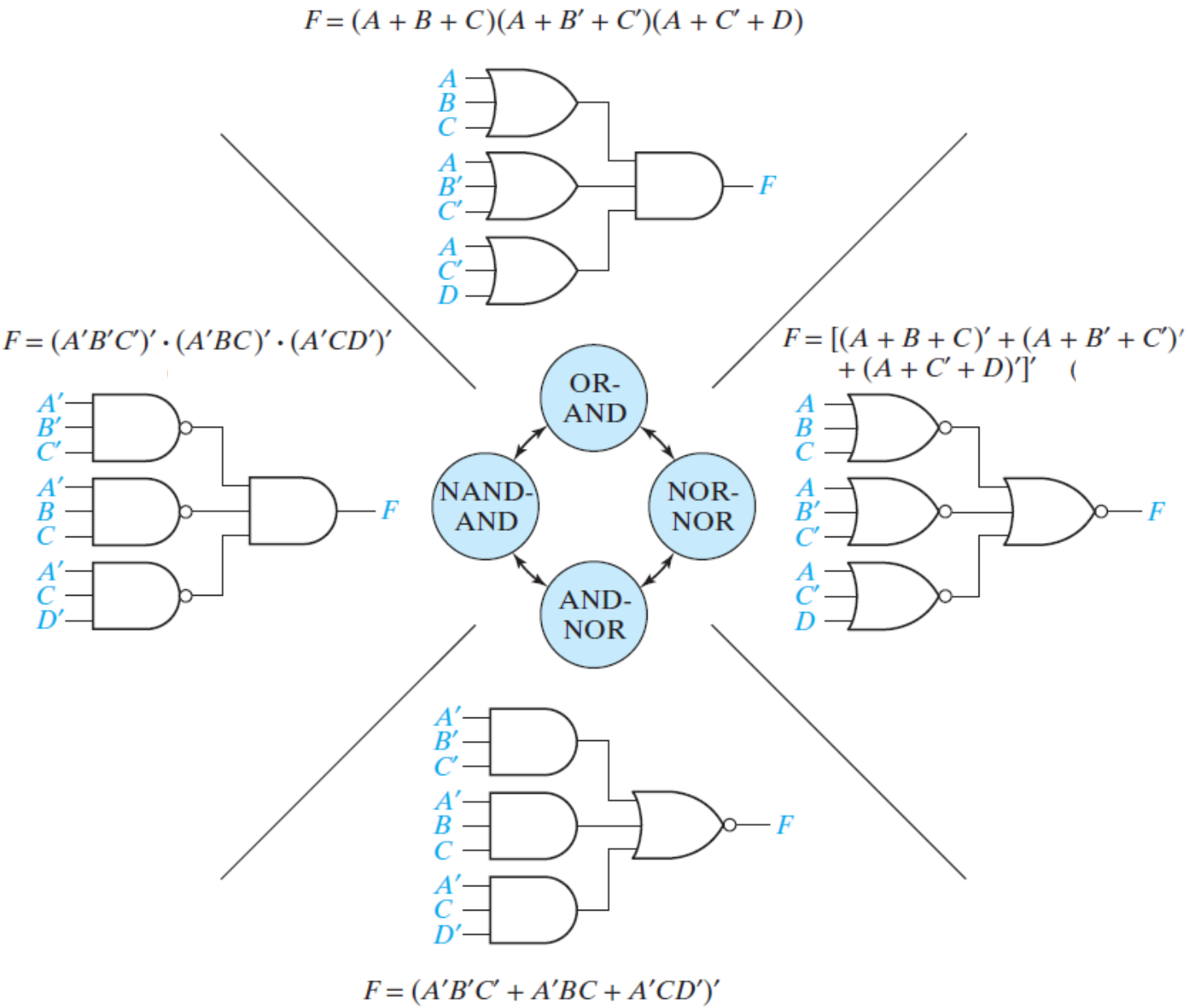
- Power noises (power integrity)
- Parasitic R,L,C
- Coupling effect
- Non-continuous physical links



2-level Circuits

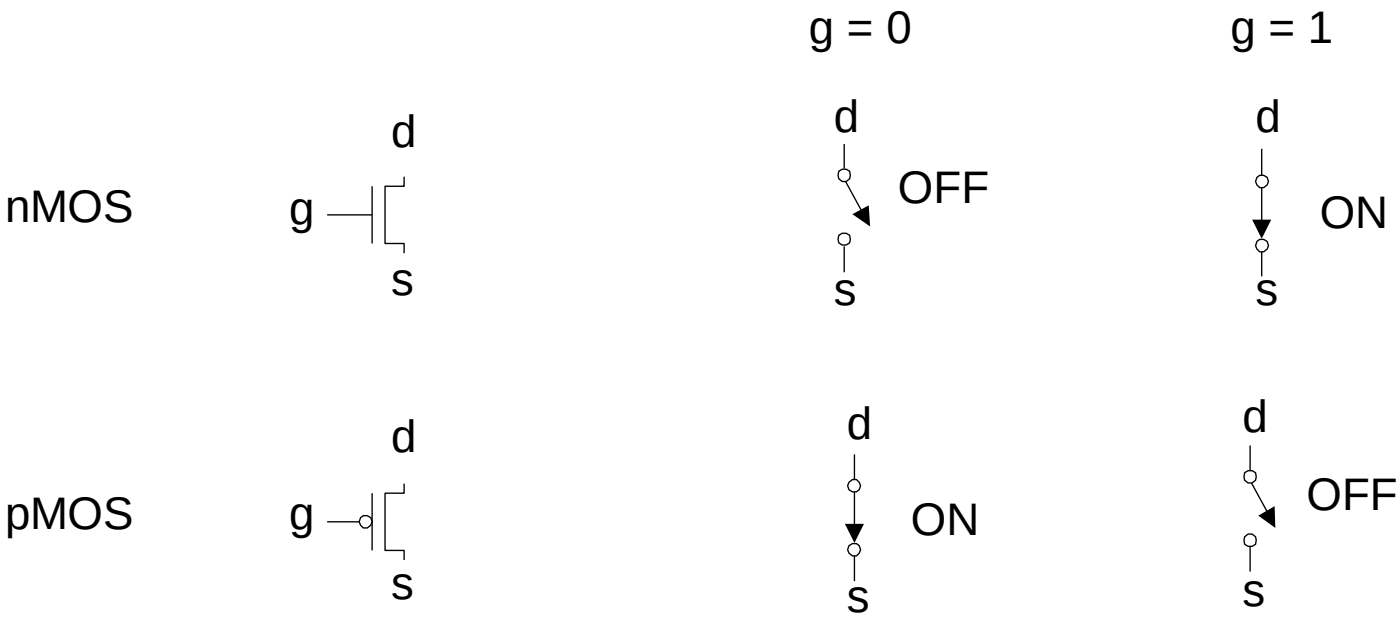


2-level Circuits



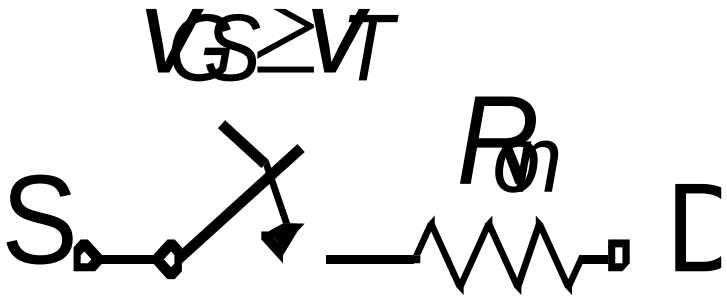
Transistors as Switches

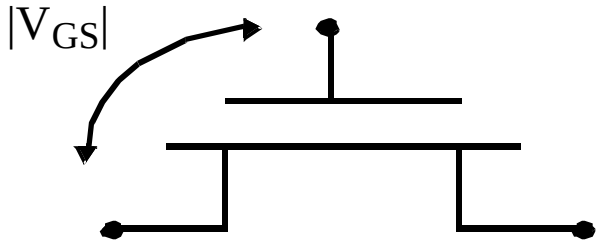
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



What is Transistor?

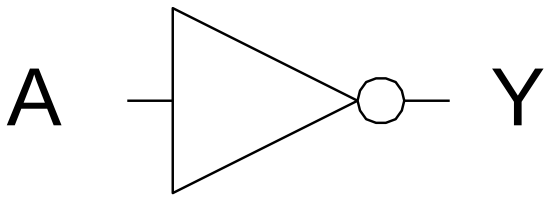
A Switch! ⟷ An MOS Transistor

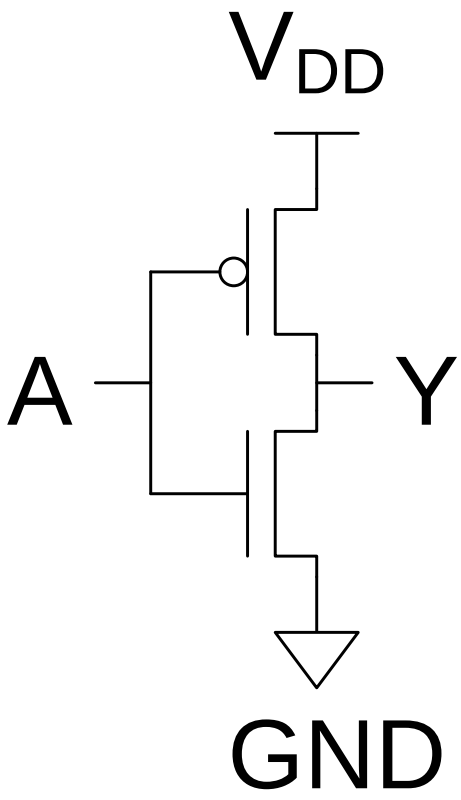




CMOS Inverter

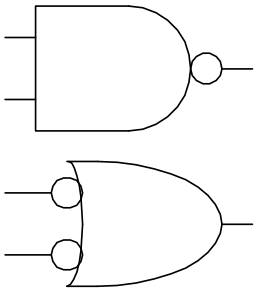
A	Y
0	1
1	0

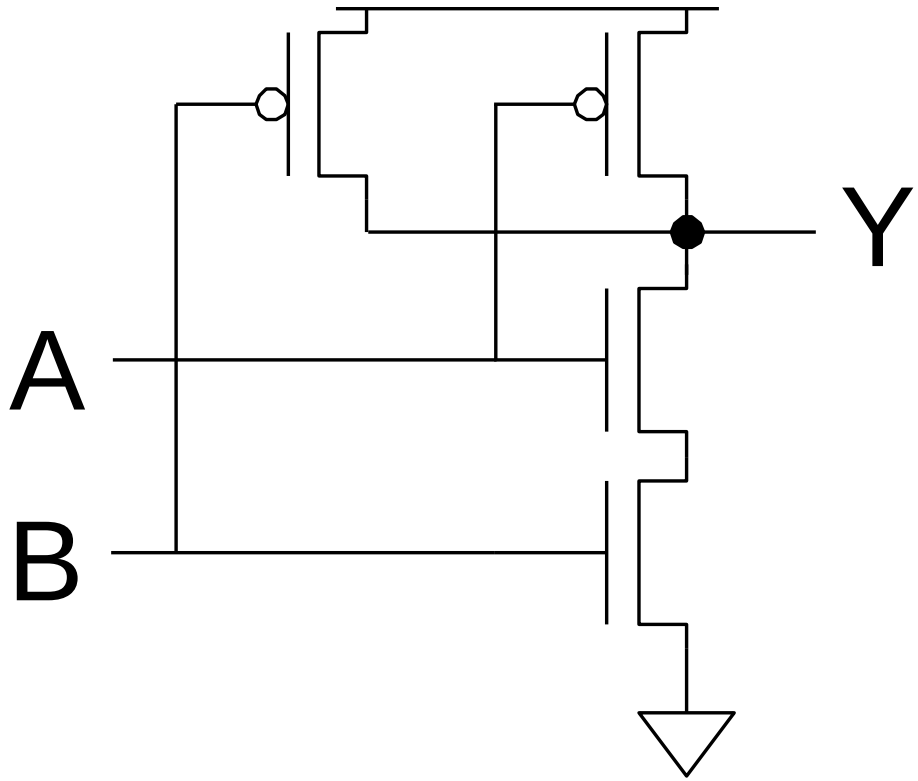




CMOS NAND Gate

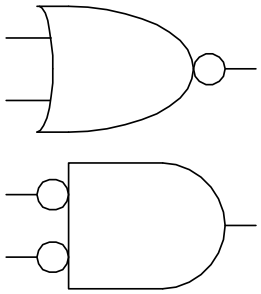
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

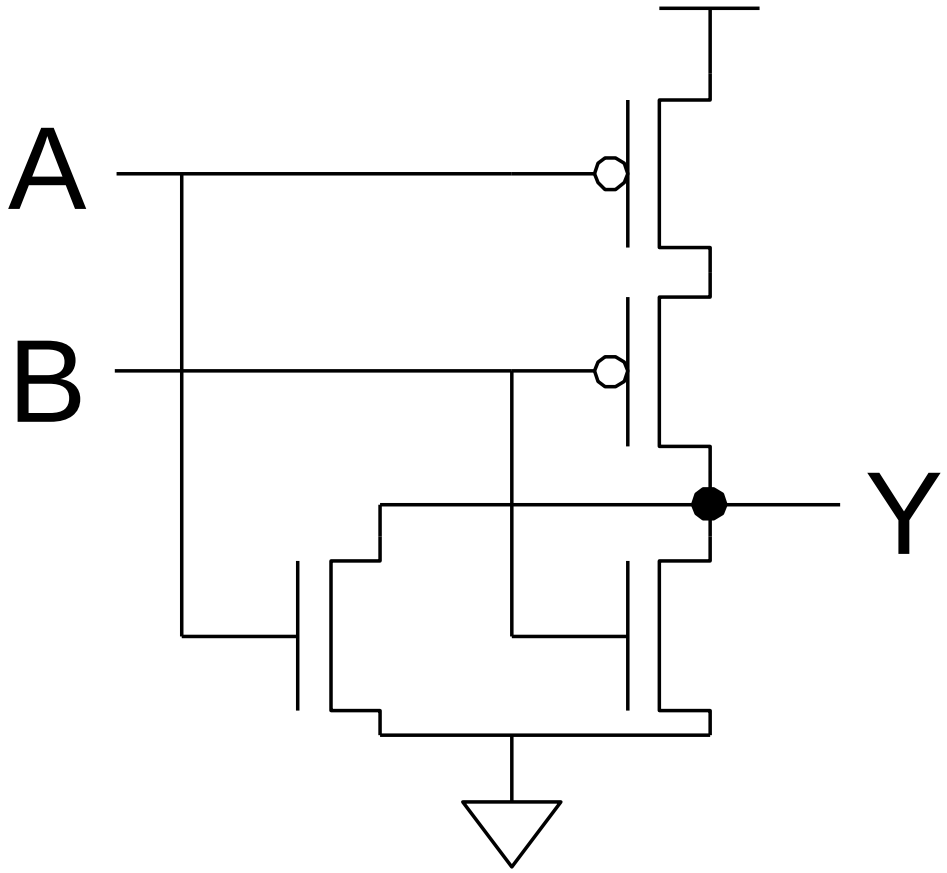




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

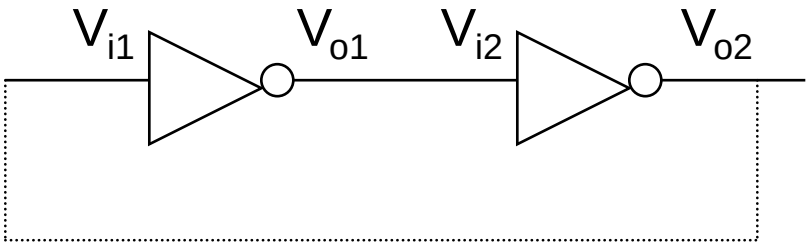




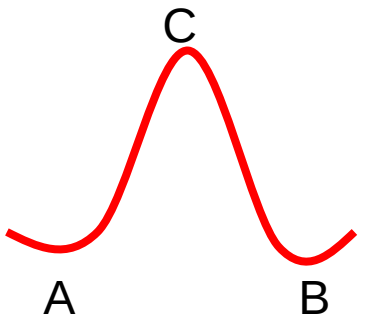
Basic Logic for Digital System in CMOS ICs

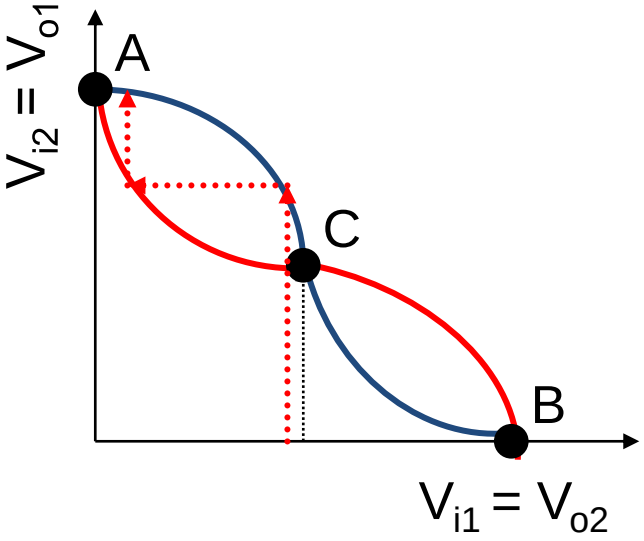
- Combination logic
  - Control switch (MUX)
  - Computation (XOR)
  - Basic logic – INV, NAND, NOR
- Sequential circuits & Finite State Machine (FSM)
  - Storage element (Latch, Flip-Flop)
- Data storage
  - Register file, SRAM, eDRAM, eFlash…
- I/O (input/output)
  - ESD protection, driving ability, level-sensing

The Regenerative Property for SRAM



cascaded inverters

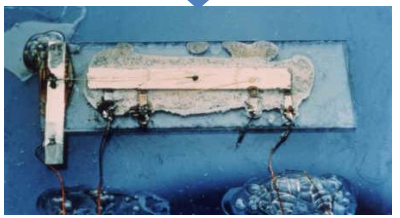


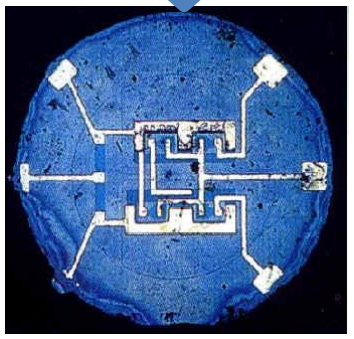


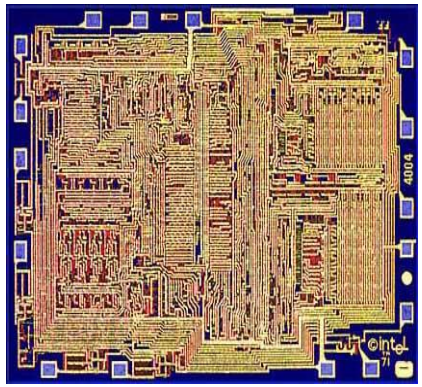
If the gain in the transient region is larger than 1, only A and B are stable operation points. C is a metastable operation point.

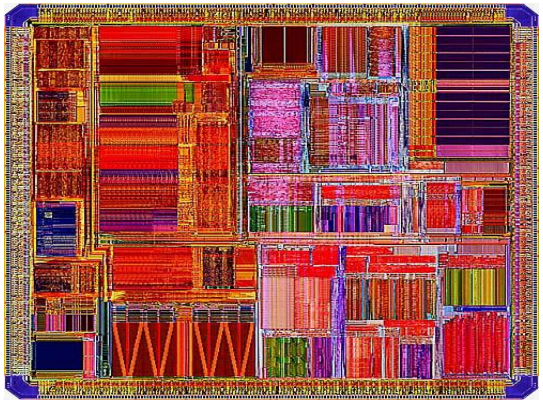
How to put together millions of transistors?

- Well chosen design methodologies
- Well chosen architectures
- Extensive use of power full CAD tools
- Strict design management
- Well chosen testing methodologies
- Design re-use
- One can NOT use same design methodologies and architectures when complexity increases orders of magnitude









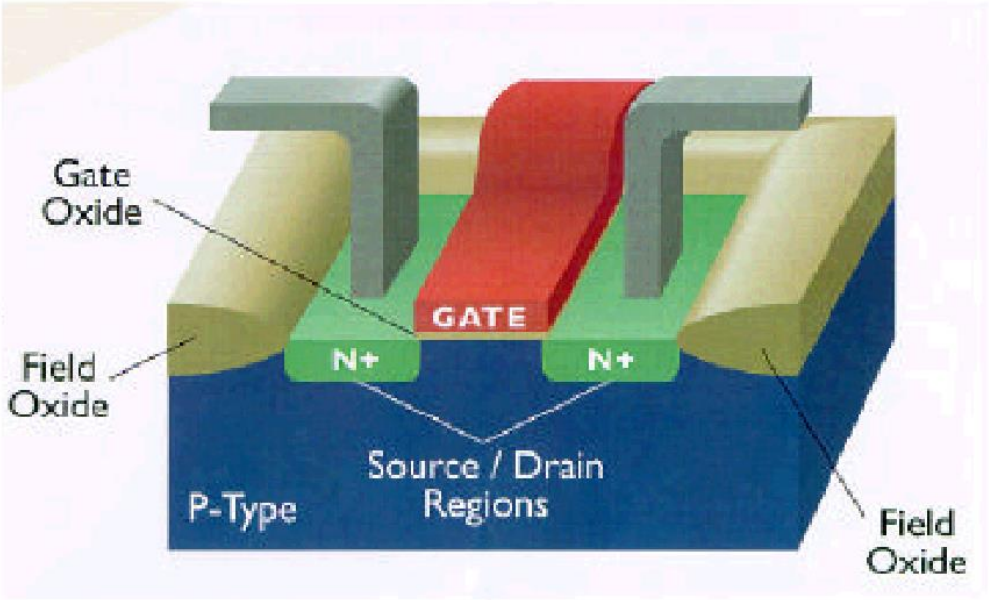
General Principles

- **Technology changes fast => important to understand general principles**
  - optimization, tradeoffs
  - work as part of a group
  - leverage existing work: programs ,building blocks
- **Concepts remain the same:**
  - Example: relays -> tubes -> bipolar transistors -> MOS transistors -> FinFET -> GAAFET (MBCFET)

Future Trend for advanced technology nodes or 3DIC

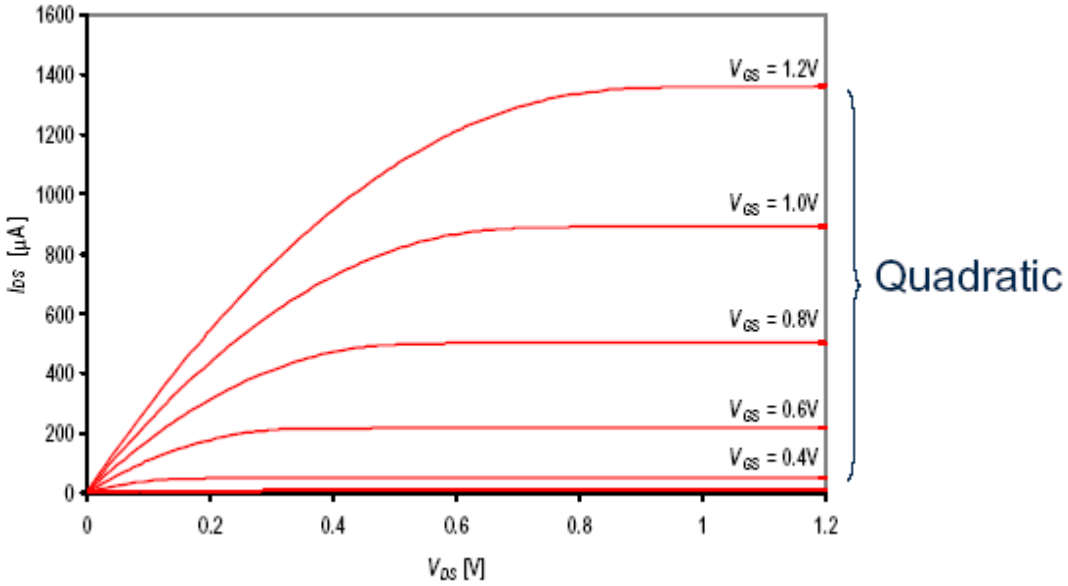
DTCO: Design-technology co-optimization

MOS Transistor: 3D Perspective

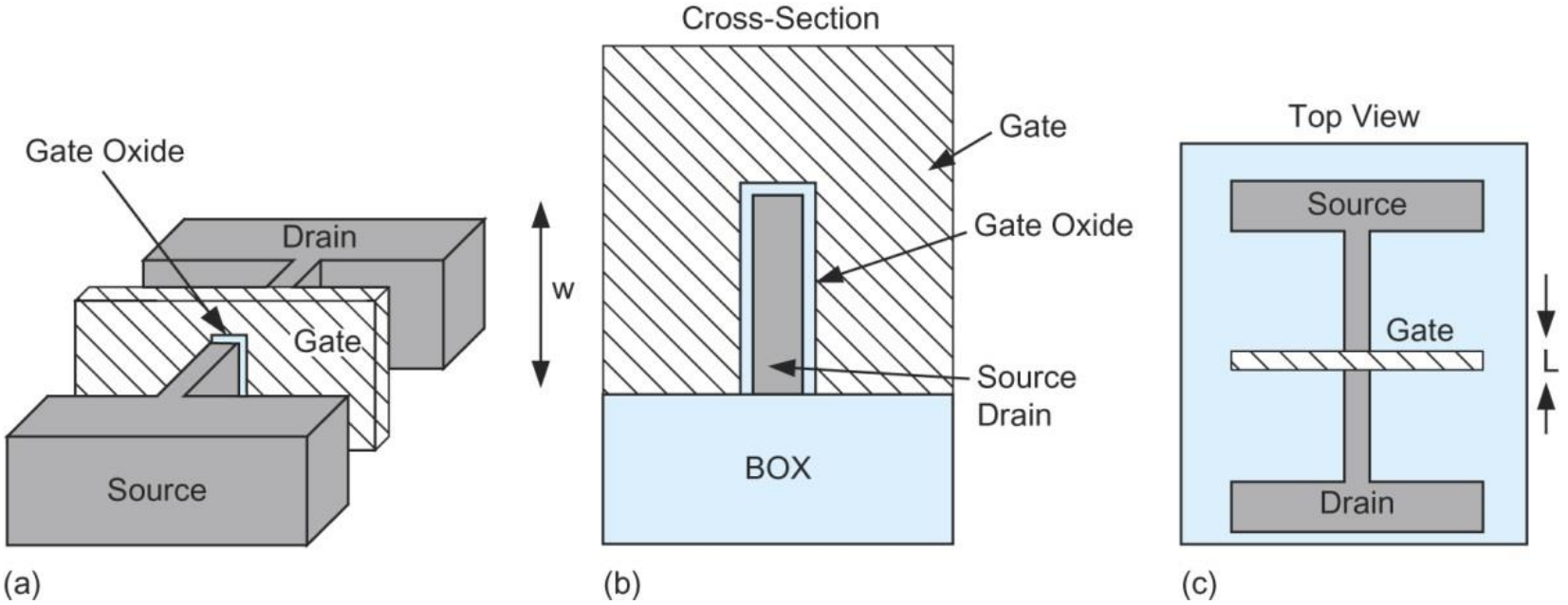


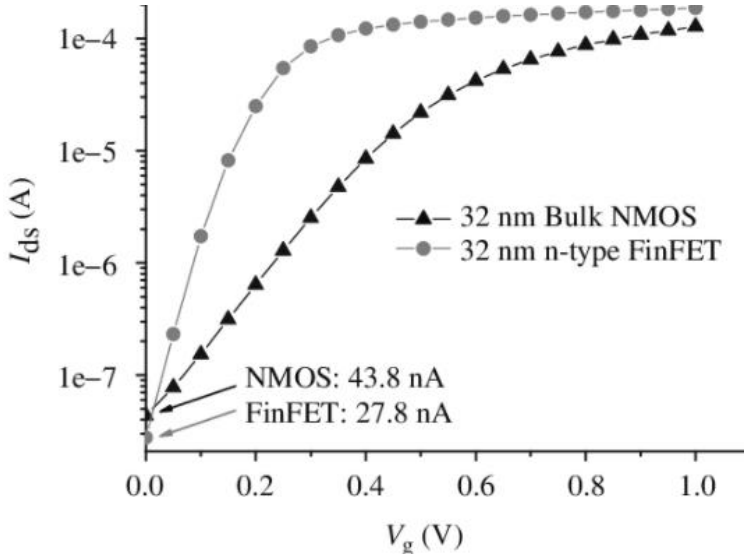
$$I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{Th} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^2$$

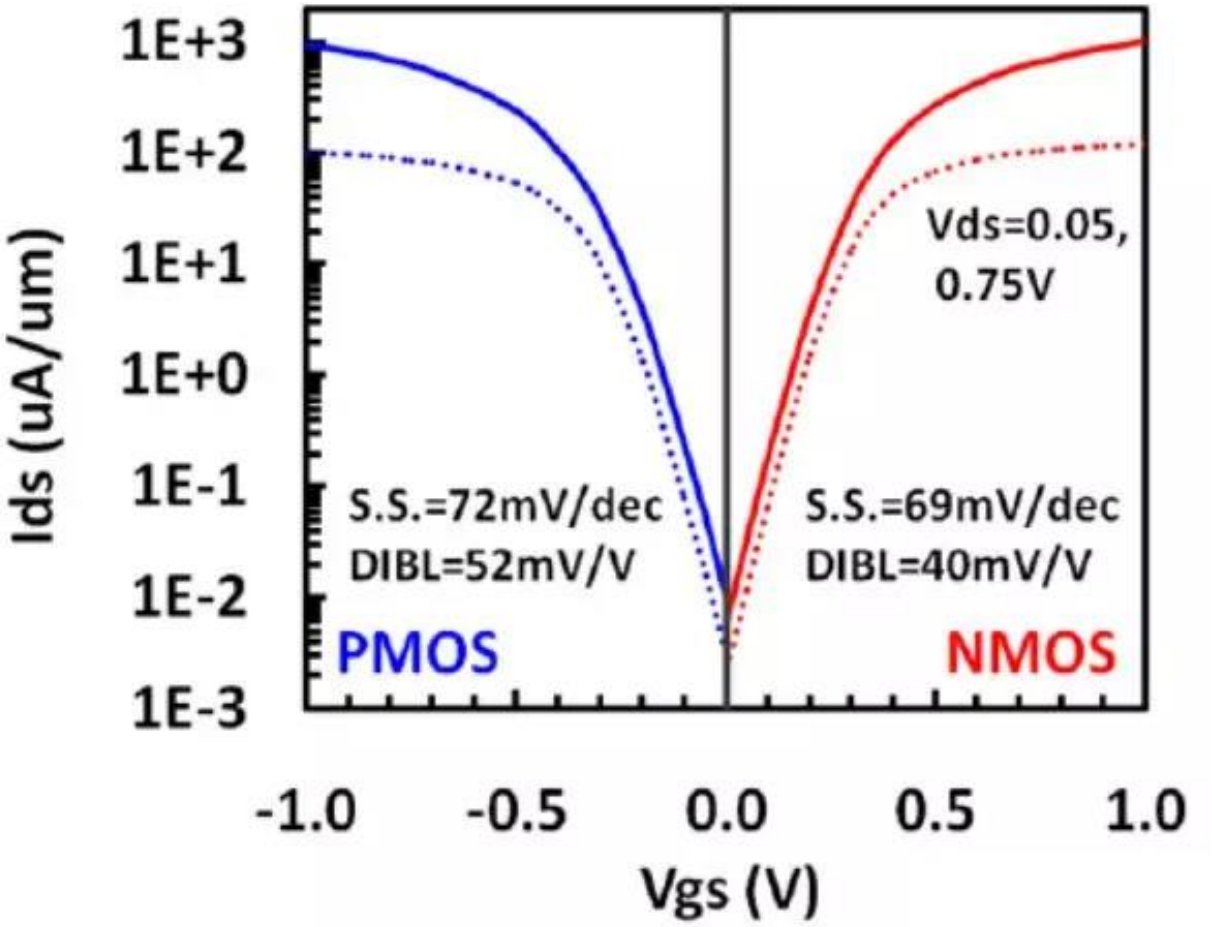


FinFET


Gate Oxide
Drain
Gate
Source
(a)
w
Cross-Section
Gate
Gate Oxide
Source
Drain
BOX
(b)
Top View
Source
Gate
Drain
L
(c)

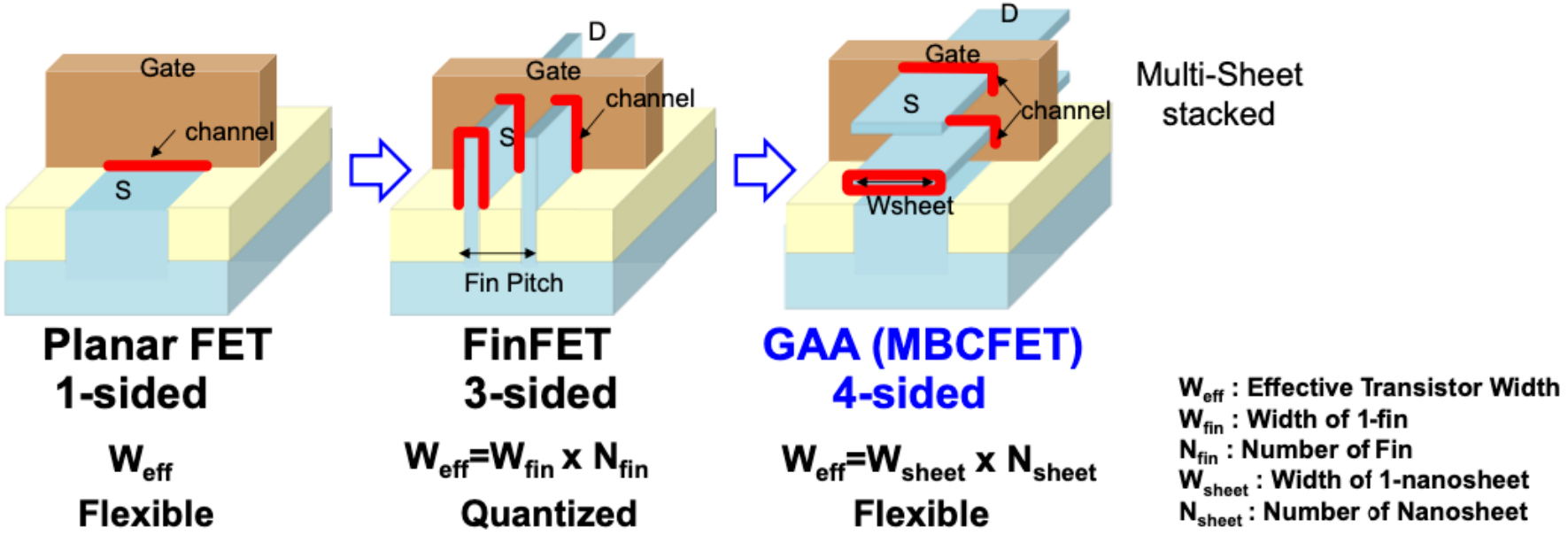

1e–4
1e–5
1e–6
1e–7
I_{ds} (A)
32 nm Bulk NMOS
32 nm n-type FinFET
NMOS: 43.8 nA
FinFET: 27.8 nA
0.0
0.2
0.4
0.6
0.8
1.0
V_g (V)

Complementary Charastertcis



GAAFET, MBCFET, RibbonFET

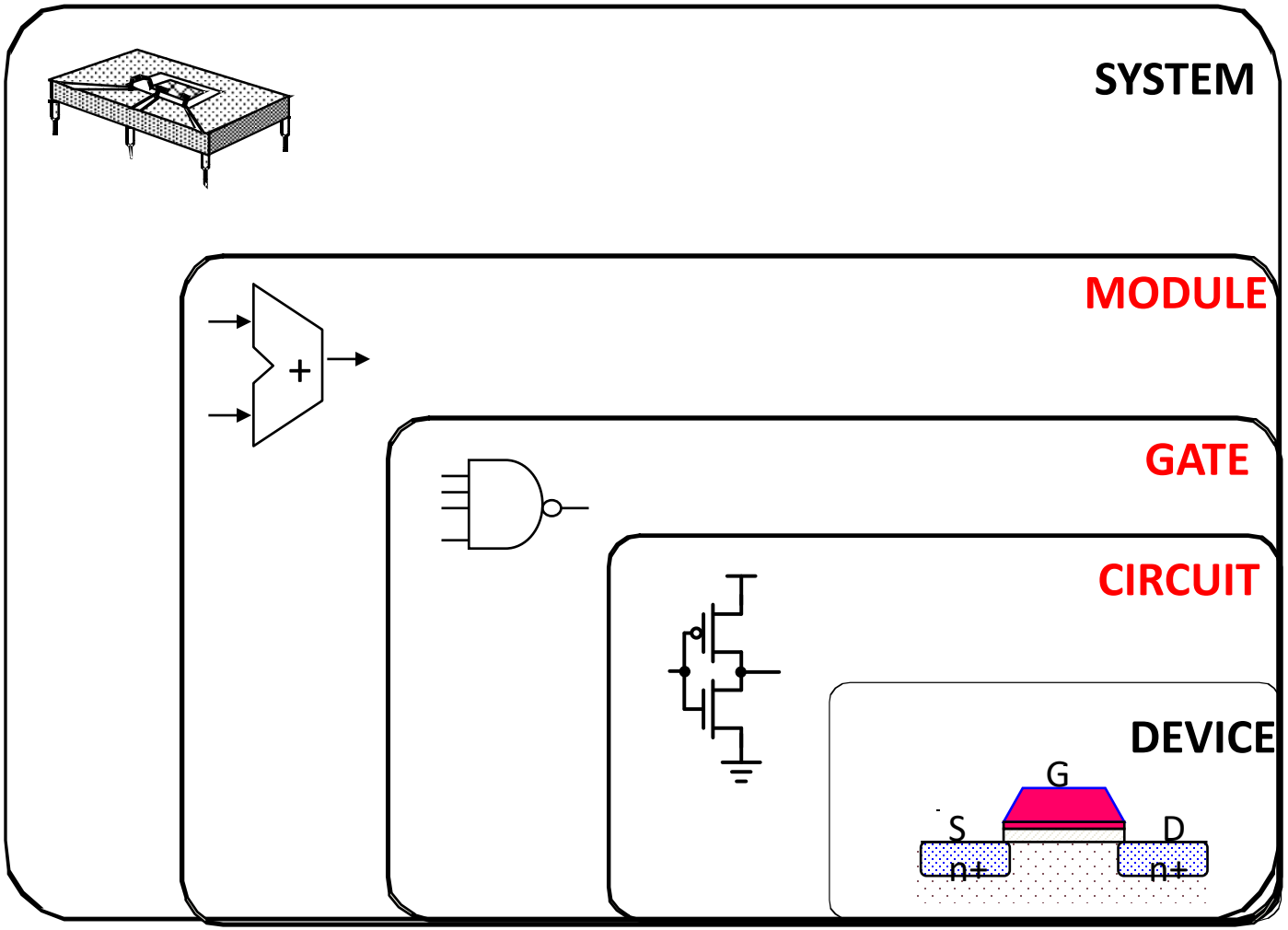
- Transistors have evolved to provide better PPA for designers
- GAA is the ultimate transistor with 4-sided channel
  - GAA flexible Weff provides more freedom to optimize PPA



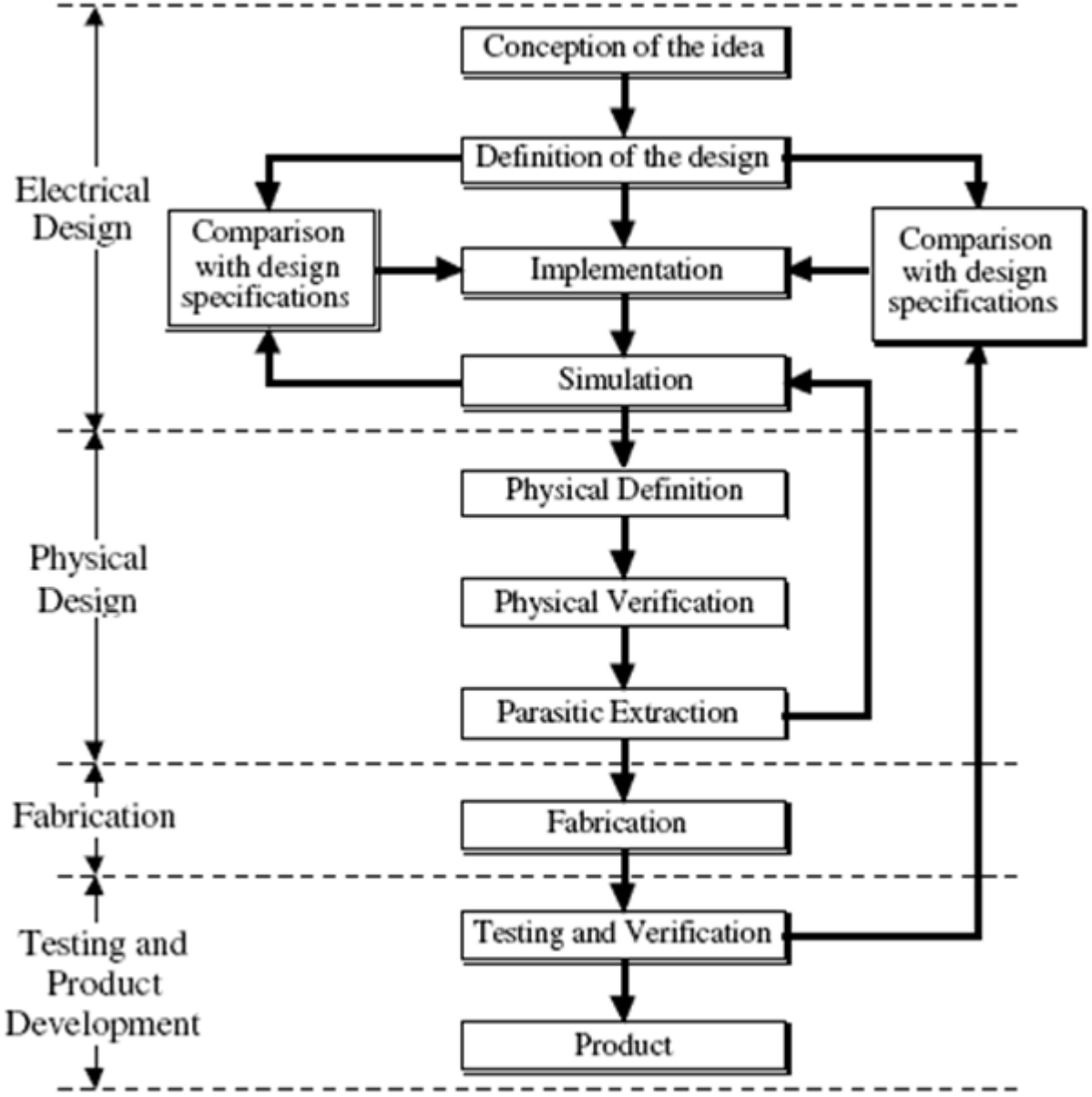
Design Abstraction Levels

Top-Down Design

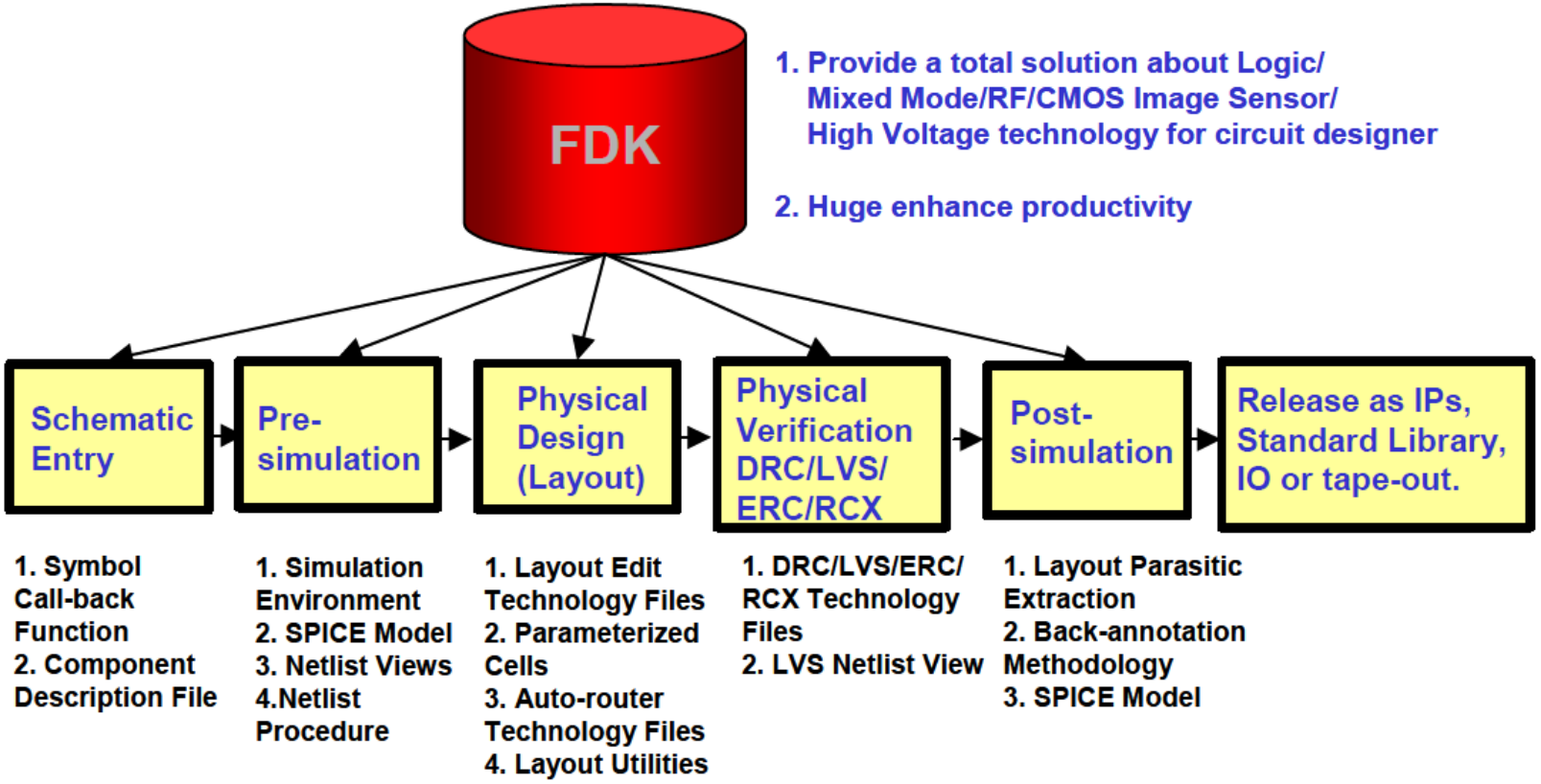
Bottom-Up Library



Typical IC Design Flow (Methodology)



Foundry Design Kit (FDK, PDK)



Full-Custom Design

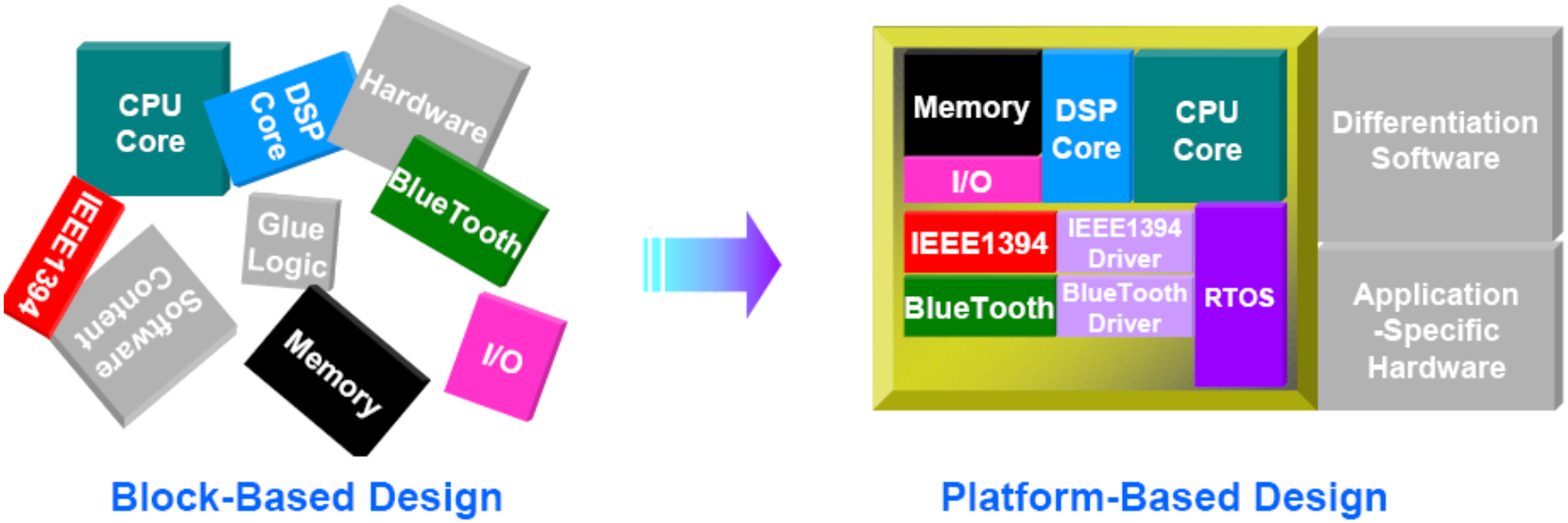
- Design some or all of the circuits, logic cells, layout specifically
  - Required cells/IPs are not available
  - Existing cell libraries can not meet the requirements
    - Area, speed or power consumption
  - Technology migration (analog or mixed-mode design)
  - Demand long design time

Cell-based (IP-Based) Design

- Use pre-designed logic cells (known as standard cells) and micro cells or IPs
- Each standard cell can be optimized individually
- All mask layers are customized
- Custom blocks can be embedded

System Design Paradigm

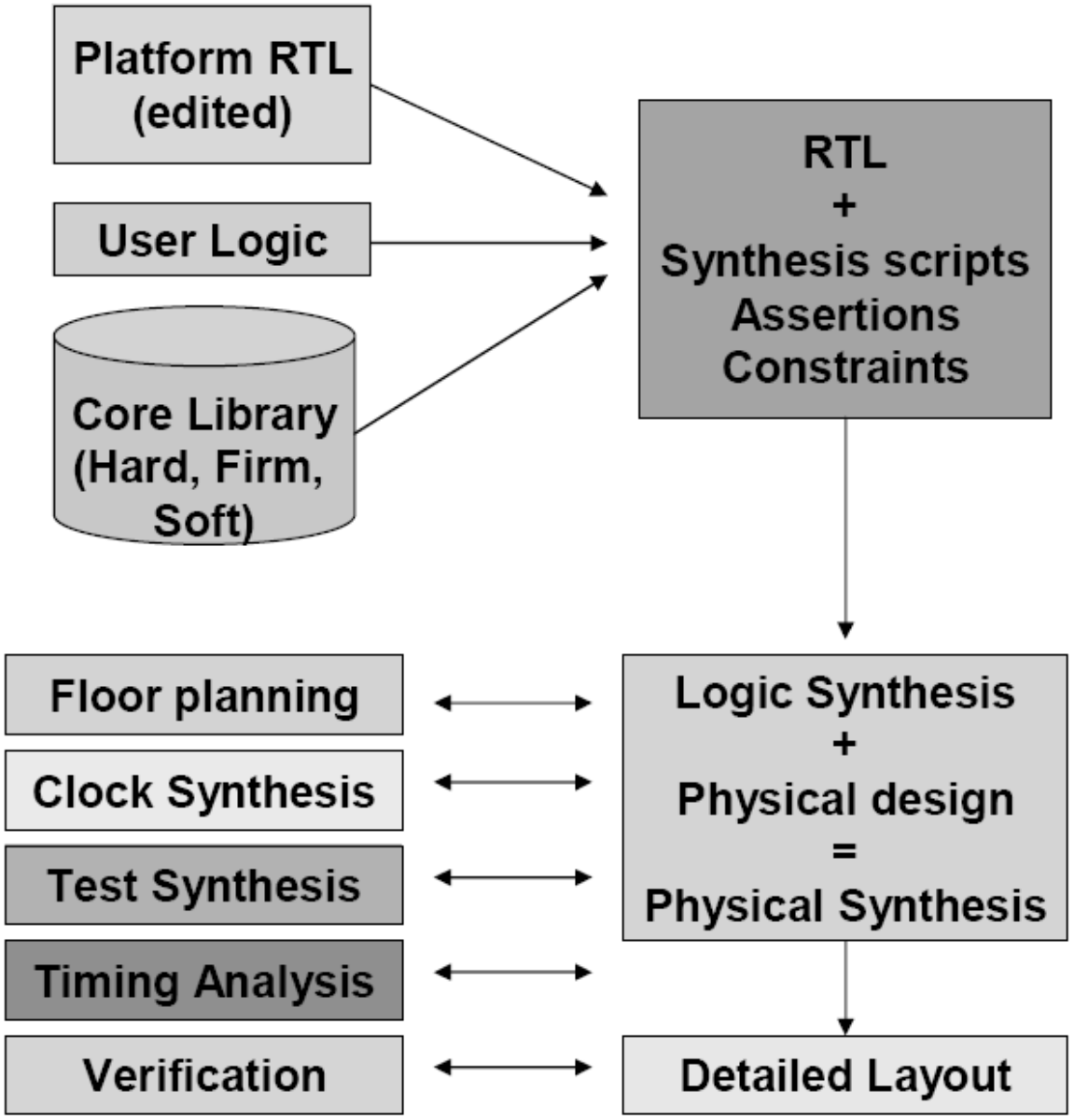
- Data computation (functional IP)
- Data communication (platform)
- Data storage (memory)



Block-Based Design

Platform-Based Design

SoC Hardware Design Methodology

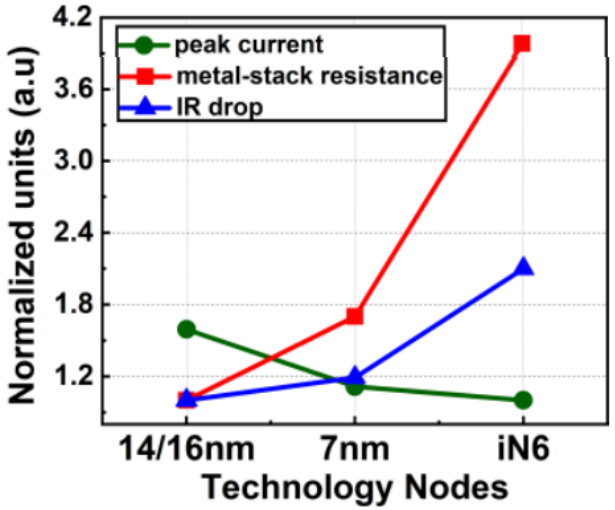


Design Metrics

- Evaluate performance of a digital circuit and System
  - Cost
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function
  - Robustness
  - Reliability
  - Scalability

Design Challenges for Future IC Design

- Large variations
- Increasing leakage current
- Increasing RC of Interconnects
- Power integrity (large power noises)



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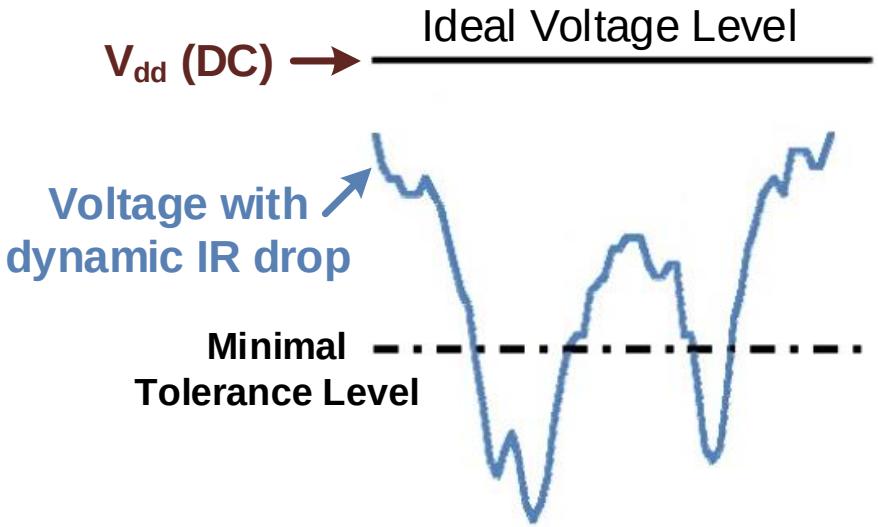
Static IR drop



Dynamic IR drop

Problems of Wire Delay

- Wire loading: timing optimization is based on a wire loading model.
- Loading of gate = input capacitance of following gates + wire capacitance
  - Gate loading known by synthesizer
  - Wire loading must be estimated
  - R-C delay calculation very complicated