Digital IC Design

Lec 4-1:

Combinational Circuits – CMOS Logic

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Cell-based (IP-Based) Design

- Use pre-designed logic cells (known as standard cells) and micro cells or IPs
- Each standard cell can be optimized individually
- All mask layers are customized
- Custom blocks can be embedded

Standard Cell Library

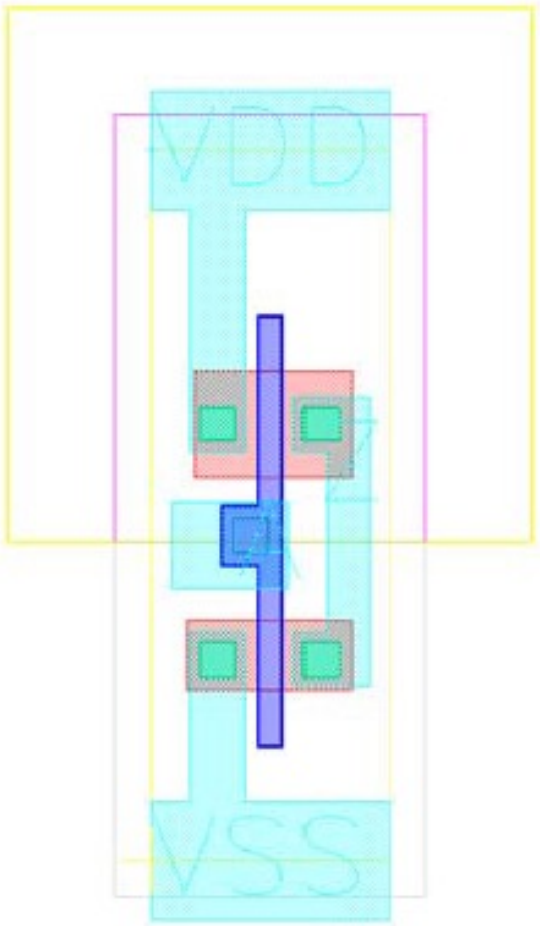
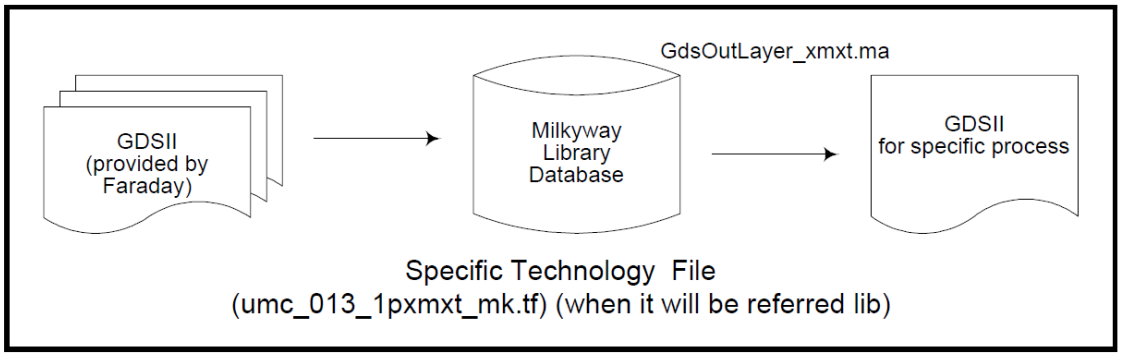
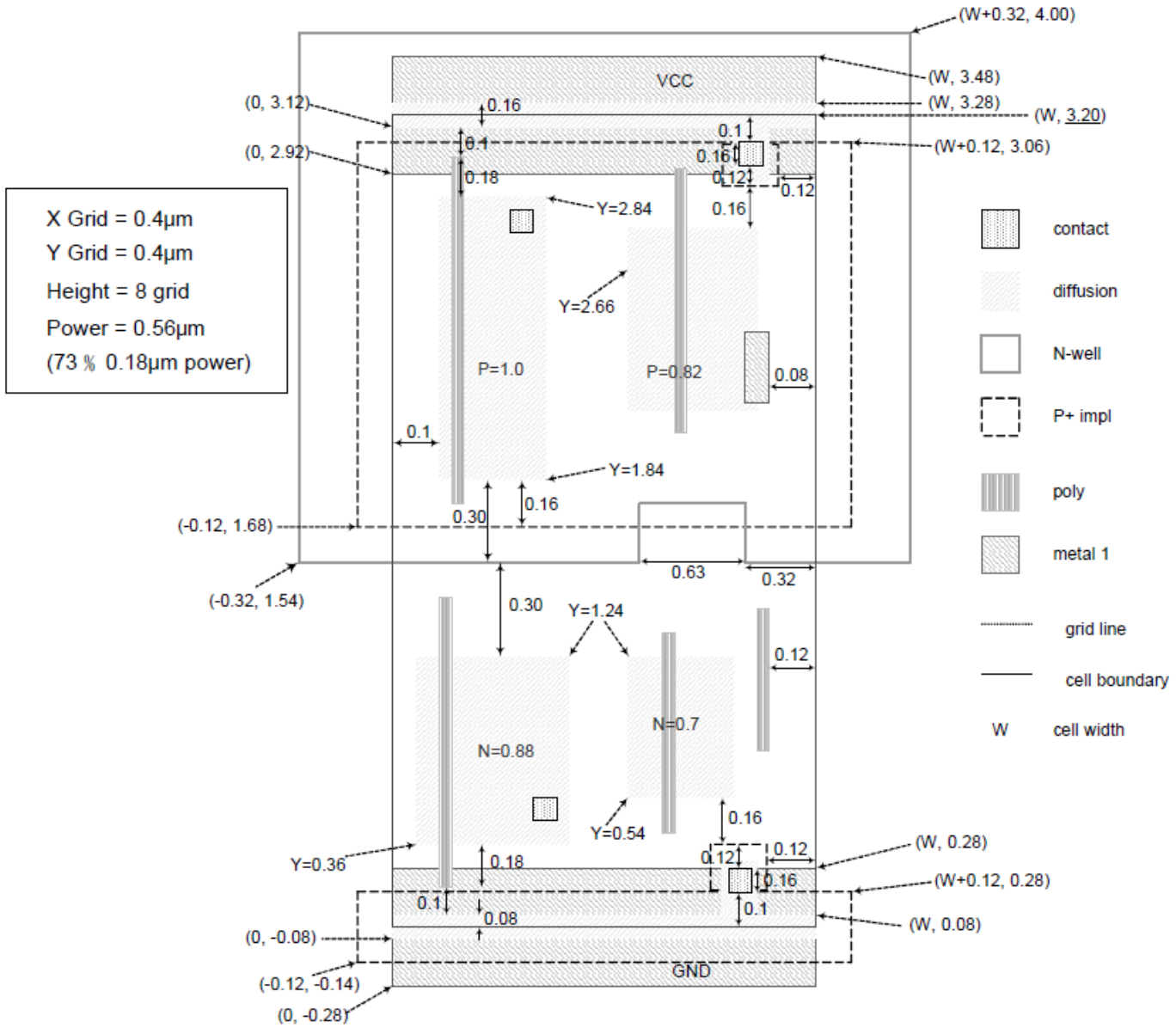


Table 2. Specifications of UMK65LSCSP10BBR_B

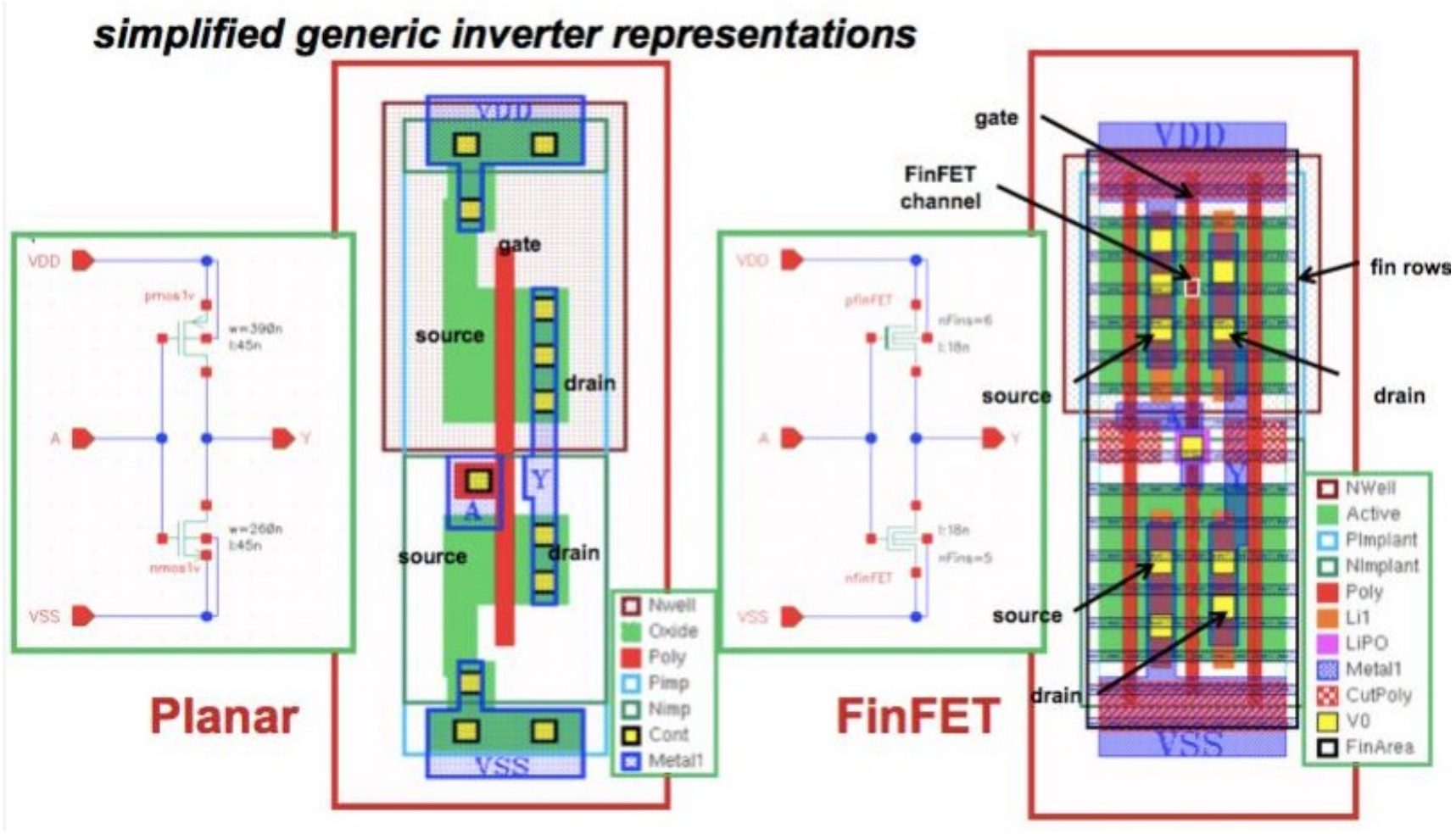
Characteristics	Specifications
Cell Height	1.8 um
Drawn Gate Length	0.06 um
Layers of Metals	7, 8, 9, 10
Layout Grid	0.005 um
Vertical Pin Grid	0.2 um
Horizontal Pin Grid	0.2 um
Power Rail Width	0.3 um



Design Rules for Cell



Planer to FinFET Layout Difference



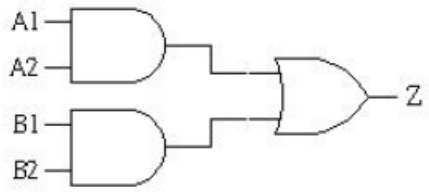
Standard Cell Library

The AO22 cell provides an OR gate with two AND gates' outputs as inputs.

Truth Table

A1	A2	B1	B2	Z
0	X	0	X	0
0	X	X	0	0
X	0	0	X	0
X	0	X	0	0
X	X	1	1	1
1	1	X	X	1

Symbol



Cell List

AO22M0NA ,AO22M1NA ,AO22M2N ,AO22M4NA ,AO22M6NA ,AO22M8NA ,AO22M12NA

AO22 Pin direction and Cap (pF)

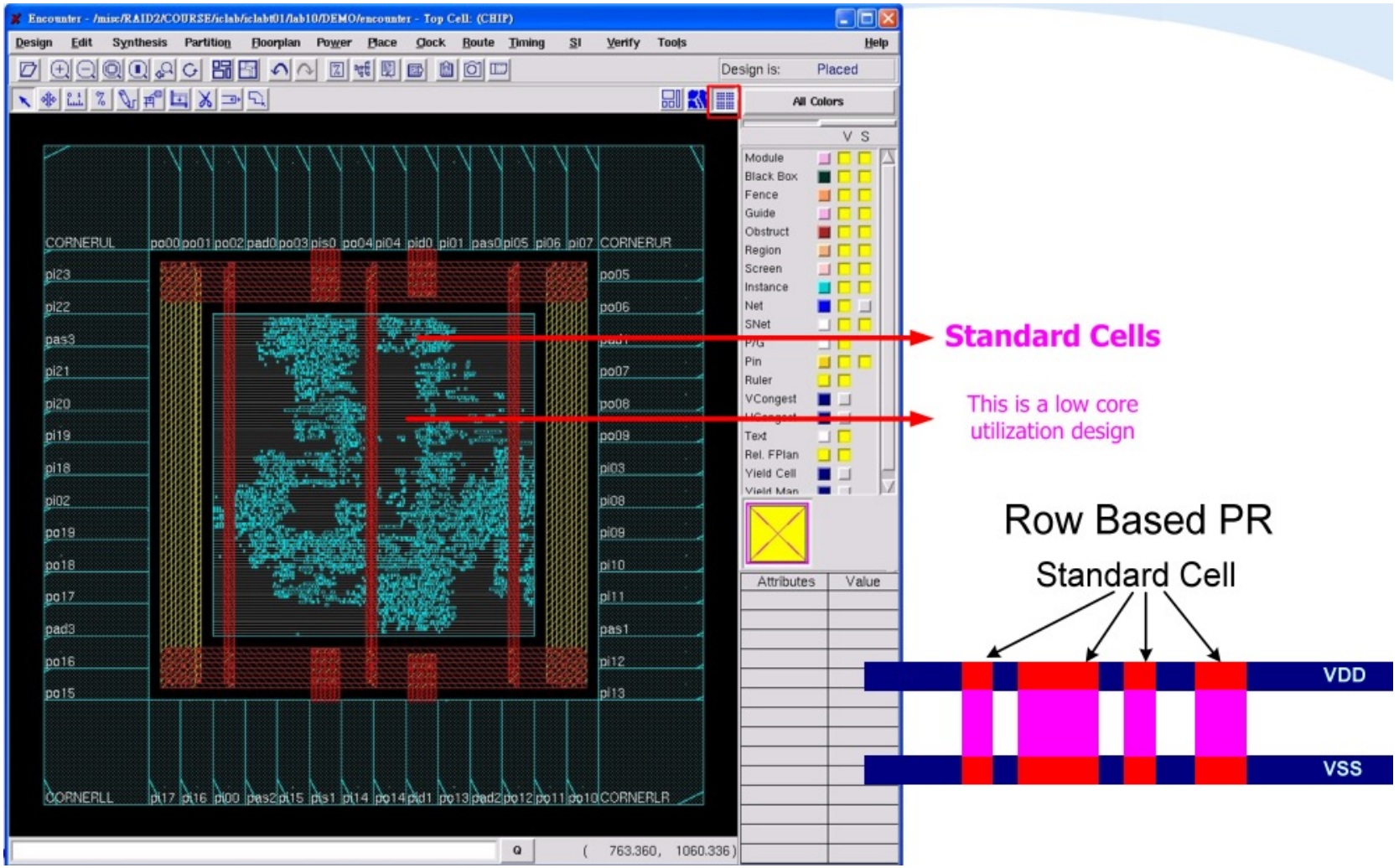
Pin	in/out	M0NA	M1NA	M2N	M4NA	M6NA	M8NA	M12NA
A1	input	0.00088	0.00087	0.00086	0.00131	0.00217	0.00264	0.00383
A2	input	0.00067	0.00067	0.00079	0.00122	0.00196	0.00243	0.00378
B1	input	0.00076	0.00076	0.00085	0.00131	0.00221	0.00271	0.00384
B2	input	0.00076	0.00075	0.00082	0.00129	0.00198	0.00246	0.00386
Z	output							

Power Dissipation (uW/MHz)

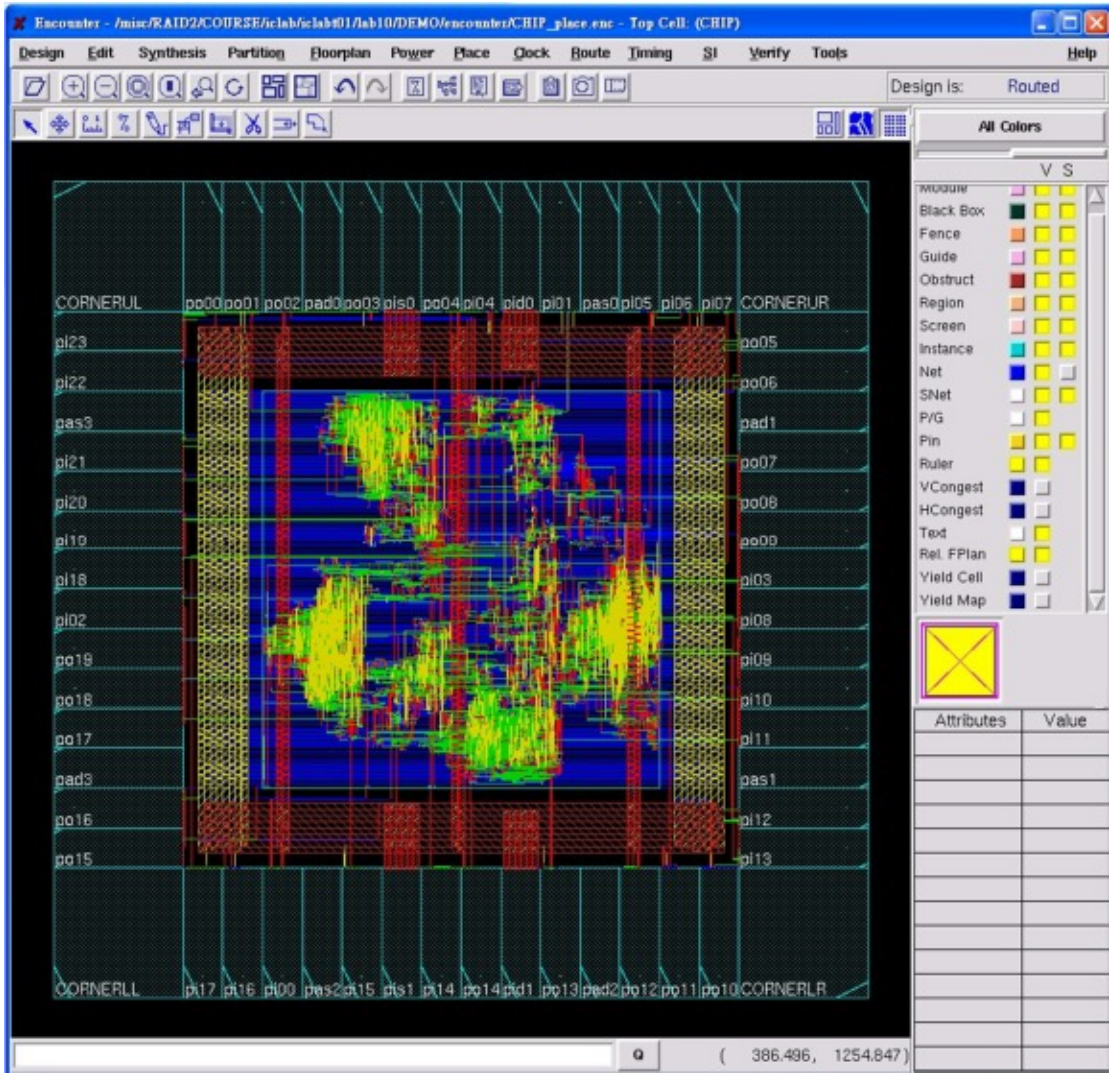
AO22M0NA at input slew= 0.03 ns, 25.0 degree C, 1.0V typical process

output load	0.0009 pF		0.0039 pF		0.0098 pF		0.0190 pF		0.0318 pF		0.0487 pF	
edge	rise	fall	rise	fall	rise	fall	rise	fall	rise	fall	rise	fall
A1->Z	0.0011	0.0024	0.0013	0.0024	0.0014	0.0024	0.0015	0.0024	0.0014	0.0024	0.0014	0.0024
A2->Z	0.0011	0.0026	0.0013	0.0026	0.0014	0.0026	0.0014	0.0026	0.0015	0.0026	0.0014	0.0026
B1->Z	0.0009	0.0019	0.0010	0.0019	0.0013	0.0020	0.0013	0.0020	0.0012	0.0019	0.0012	0.0020
B2->Z	0.0009	0.0022	0.0010	0.0022	0.0012	0.0022	0.0012	0.0022	0.0012	0.0022	0.0012	0.0022

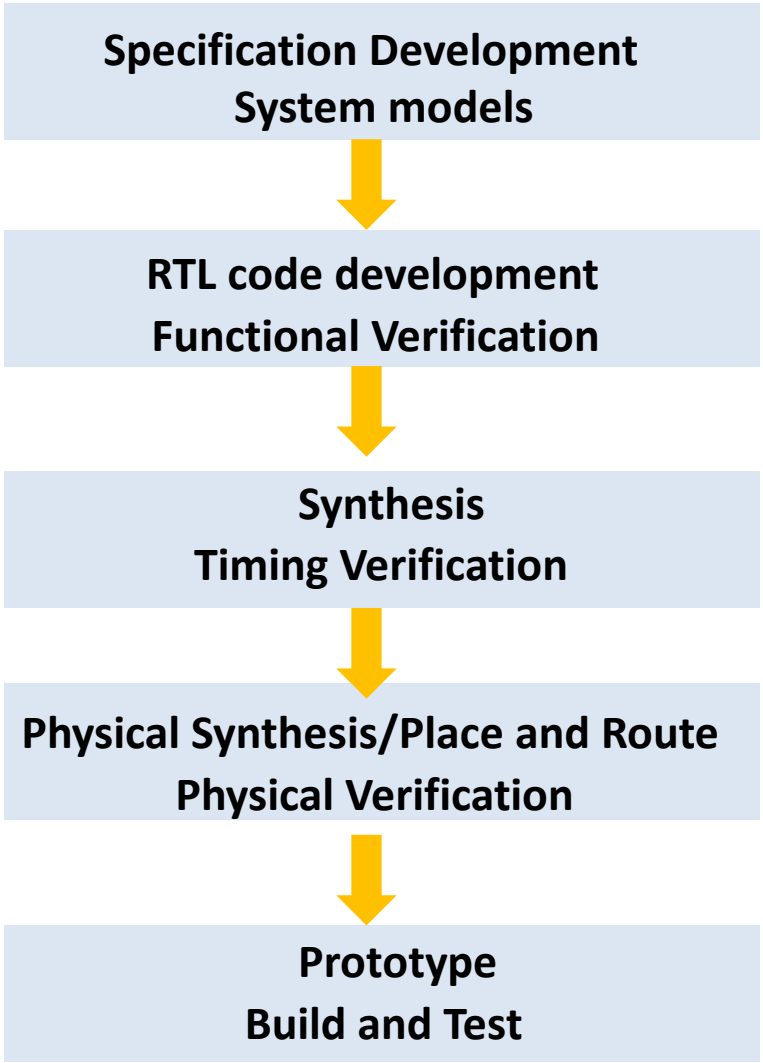
Standard Cell Placement



Wire Routing



Cell-based Design Flow



System Architecture

RTL

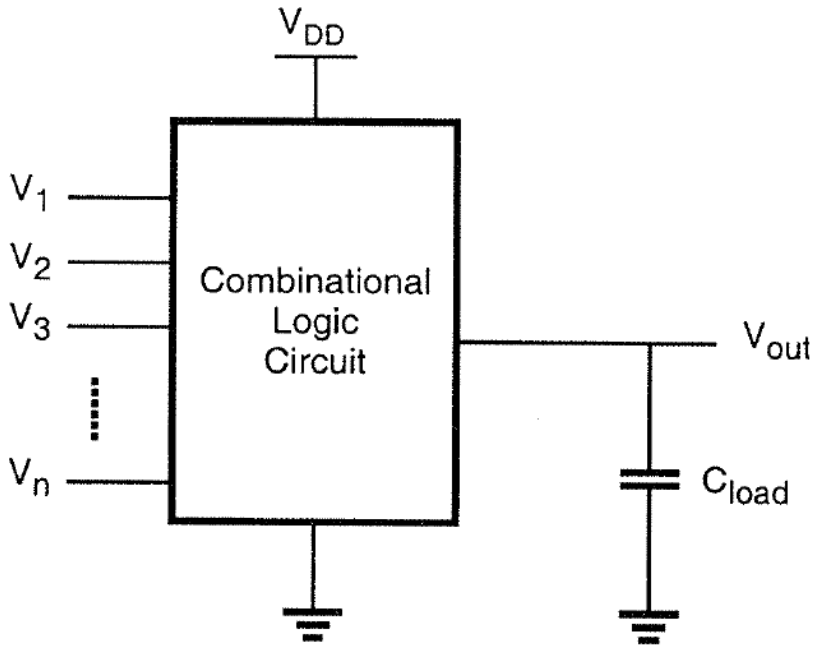
Synthesis

Physical Design

System Integration and Software Test

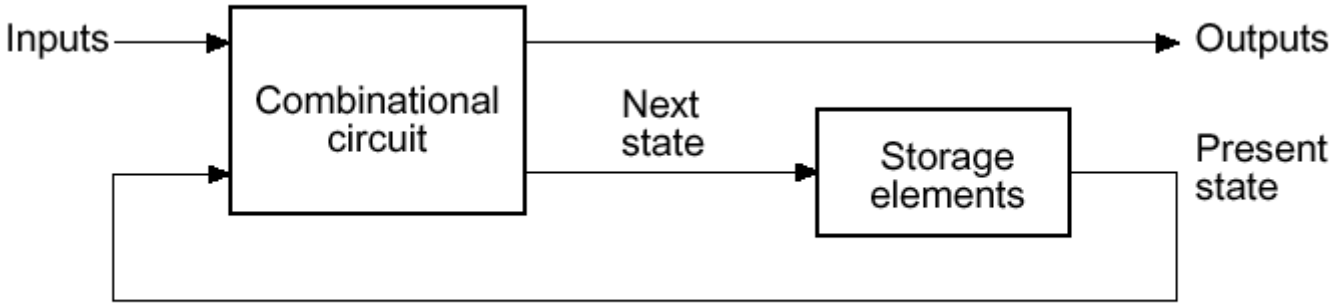
Combinational Logic

- Combinational Logic
  - Output depends only on current input
  - Has no memory



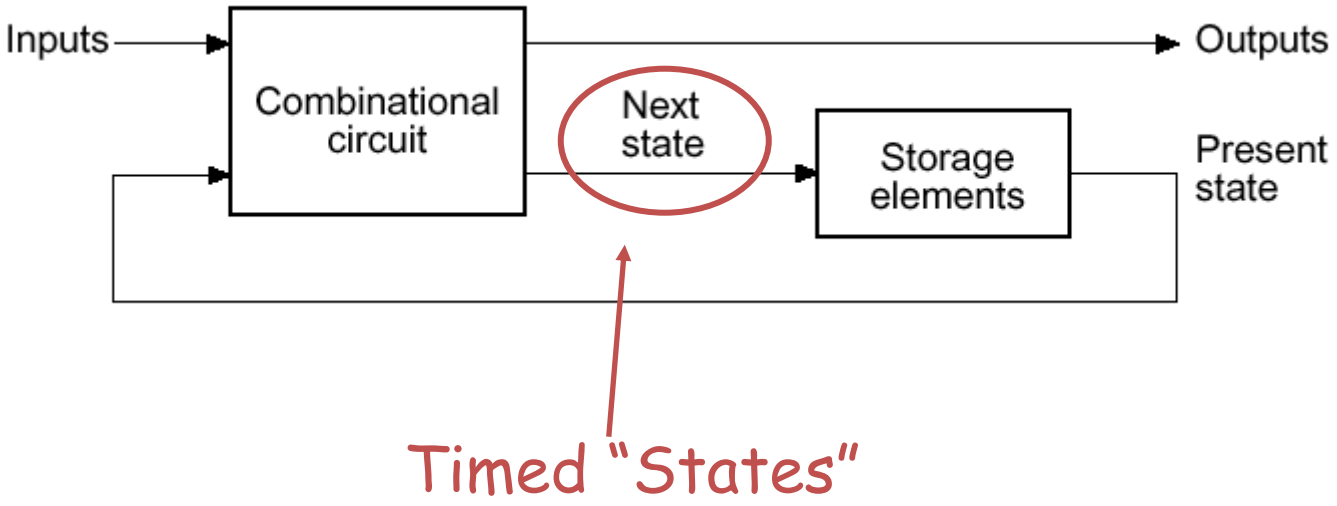
Sequential Logic

- Sequential Logic
  - Output depends not only on current input but also on past input values, e.g., design a counter
  - Need some type of memory to remember the past input values



Sequential Logic: Concept

- Sequential Logic circuits remember past inputs and past circuit state.
- Outputs from the system are "fed back" as new inputs
  - With gate delay and wire delay
- The storage elements are circuits that are capable of storing binary information: memory.



Logic Family

- **Static CMOS**
  - **Complementary CMOS logic**
  - Pass Transistor Logic
  - CVSL (Cascode voltage switch logic)
  - Ratioed circuits
    - Pseudo-nMOS Logic
- Dynamic Logic

CMOS Logic Styles

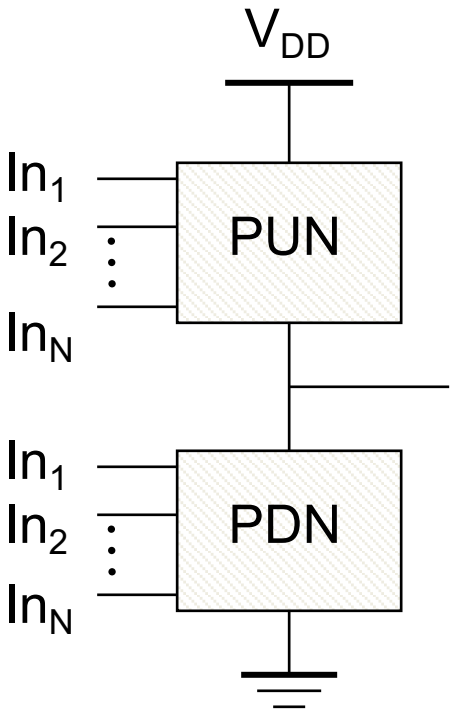
- CMOS tradeoffs :
  - Speed
  - Power (energy)
  - Area
- Design tradeoffs
  - Robustness, scalability
  - Design time
- Many styles: don't try to remember the names – remember the principles
- Changing the logic style – can it be done without breaking the synthesis flow?

CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either V_{DD} or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between V_{DD} and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

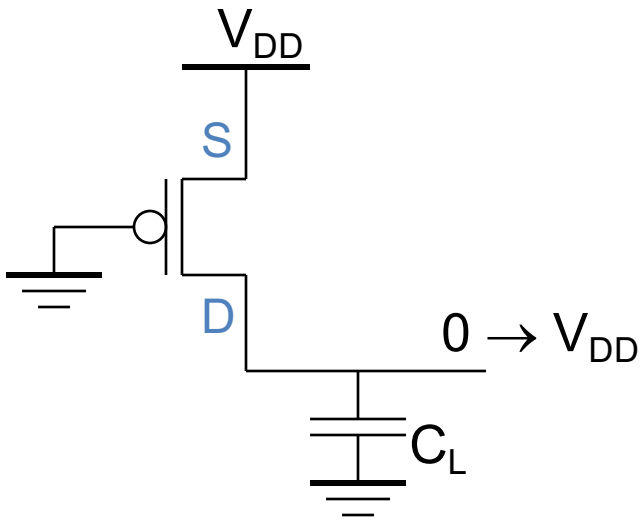
pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

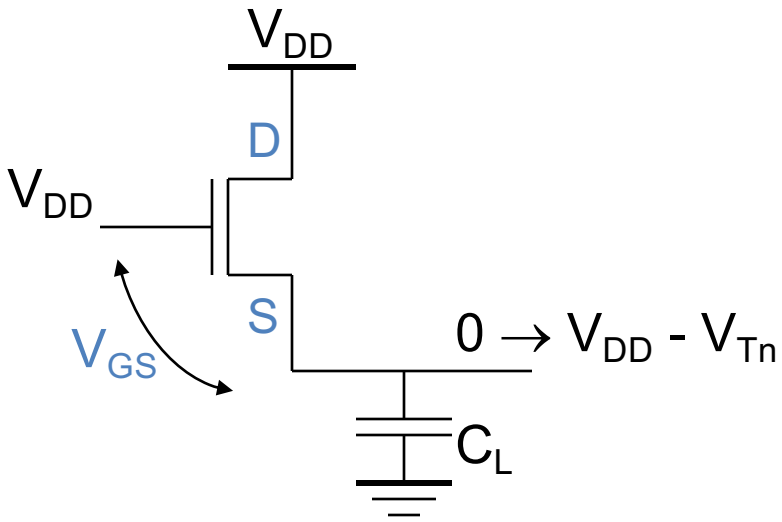
NMOS transistors only

PUN and PDN are dual logic networks

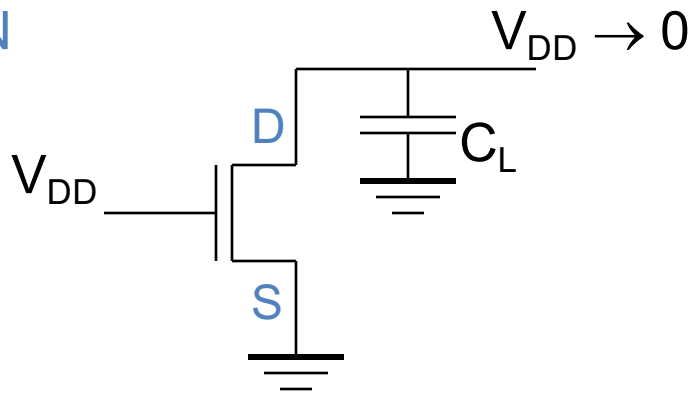
Threshold Drops

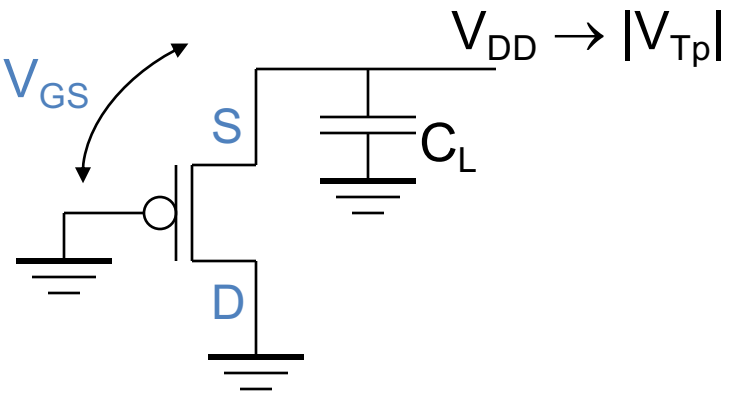
PUN





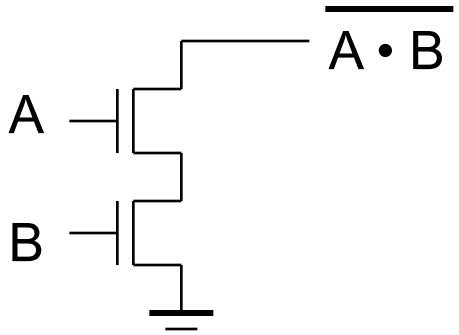
PDN



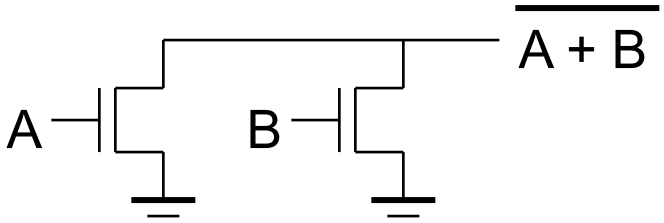


Construction of PDN

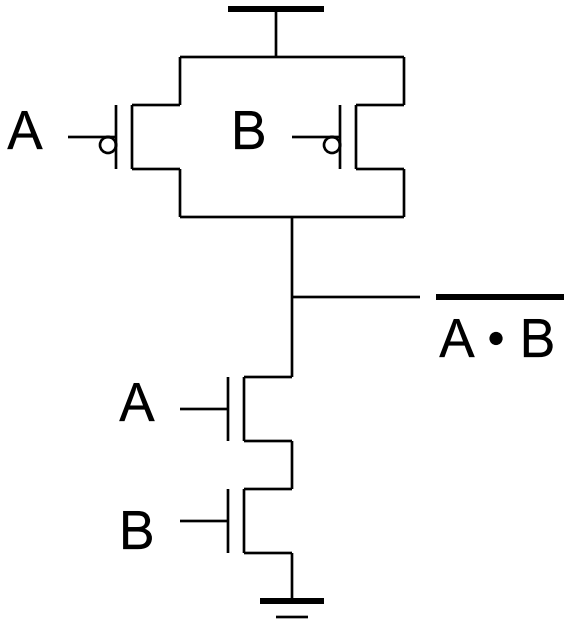
- NMOS devices in series implement a NAND function



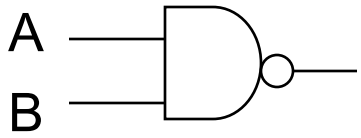
- NMOS devices in parallel implement a NOR function



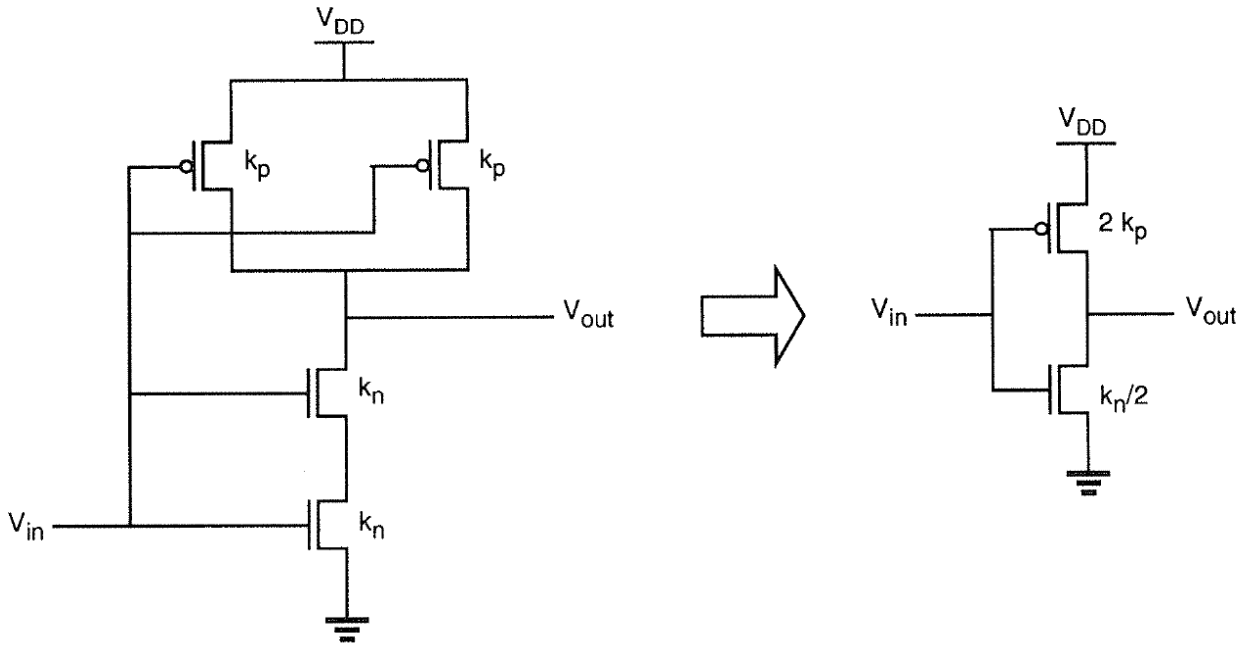
CMOS NAND



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



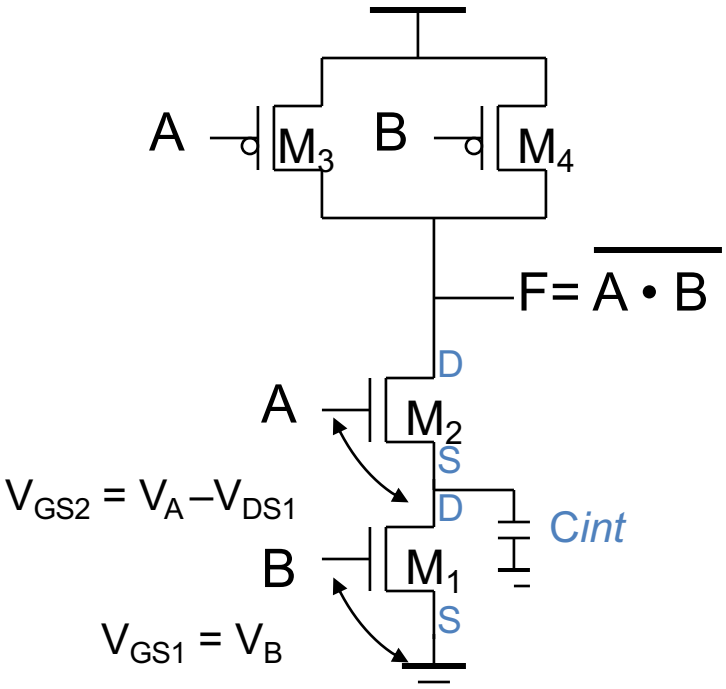
Inverter Equivalent of CMOS NAND2

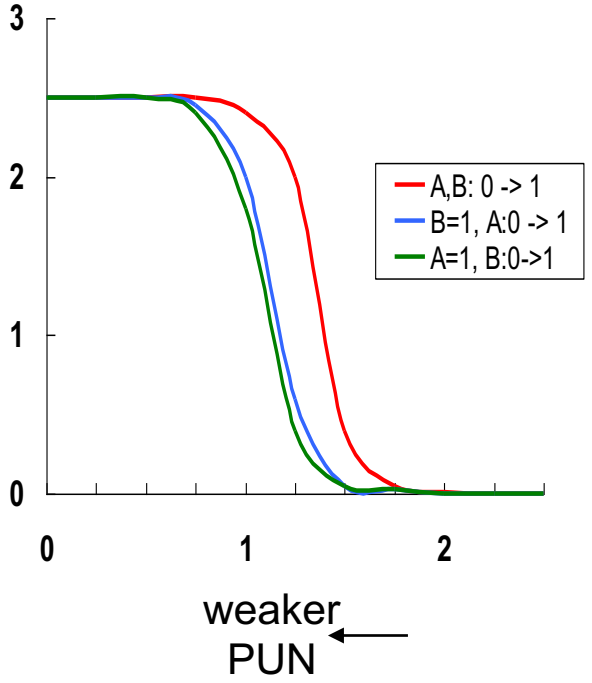


$(W/L)_{p,A} = (W/L)_{p,B}$. The switching threshold for this gate is then found as

$$V_{th}(\text{NAND2}) = \frac{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T,p}|)}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

Data-Dependent Transfer Curve





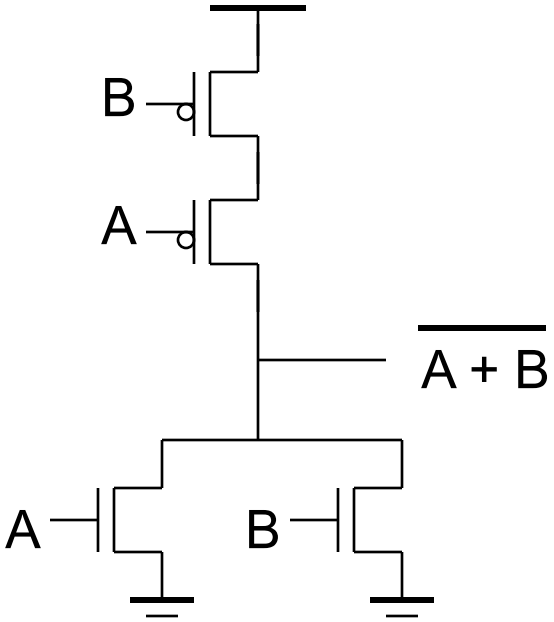
- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$V_{Tn1} = V_{Tn0}$

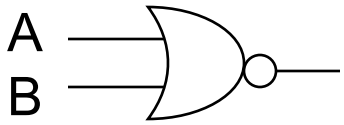
$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int})} - \sqrt{|2\phi_F|})$

since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C*int*

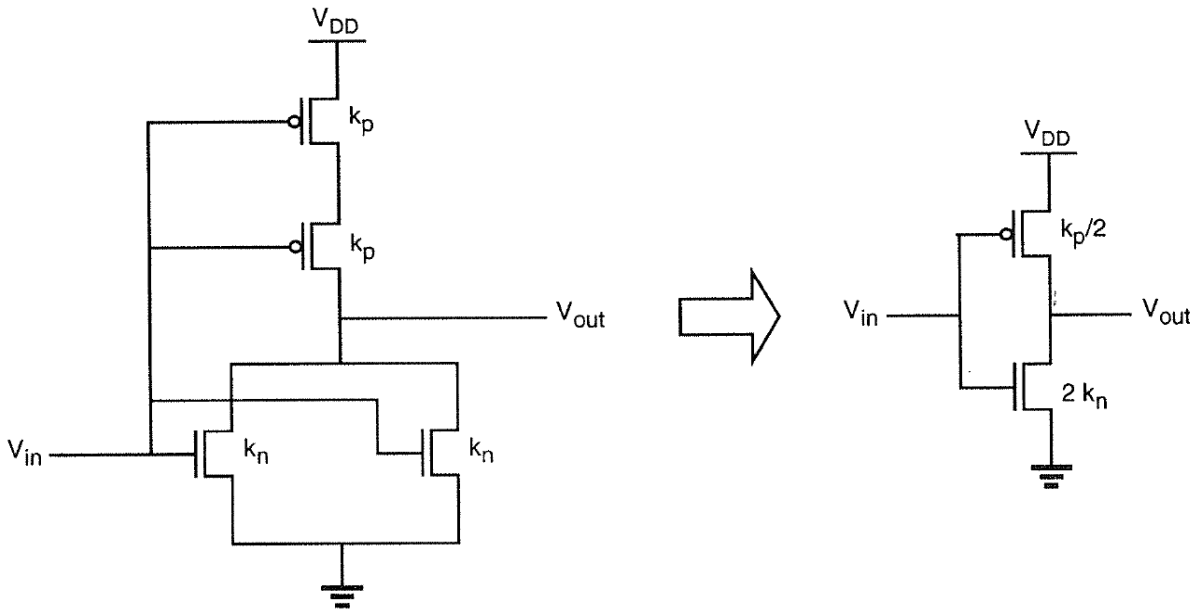
CMOS NOR



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

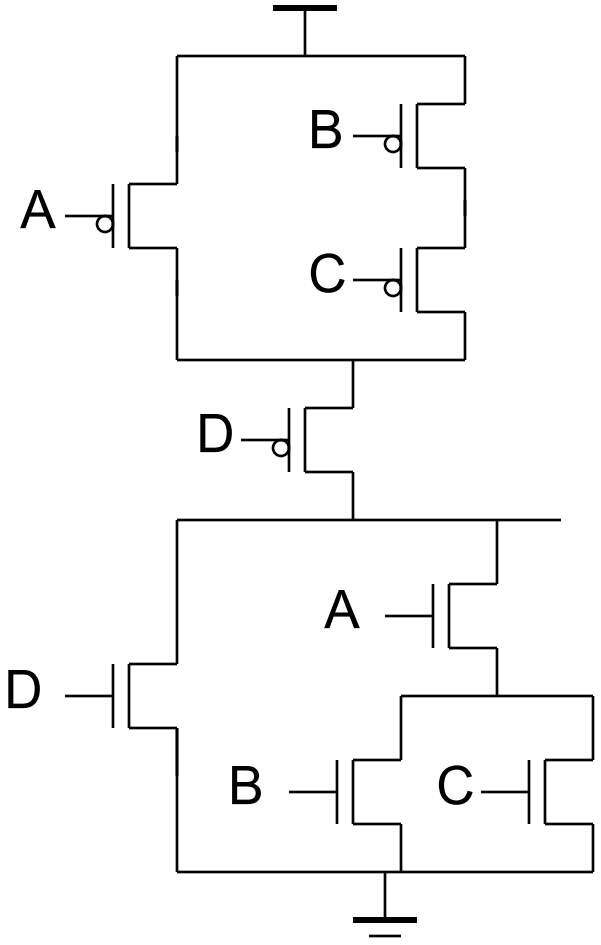


Inverter Equivalent of CMOS NOR2



$$V_{th}(\text{NOR2}) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{k_p}{4k_n}}}$$

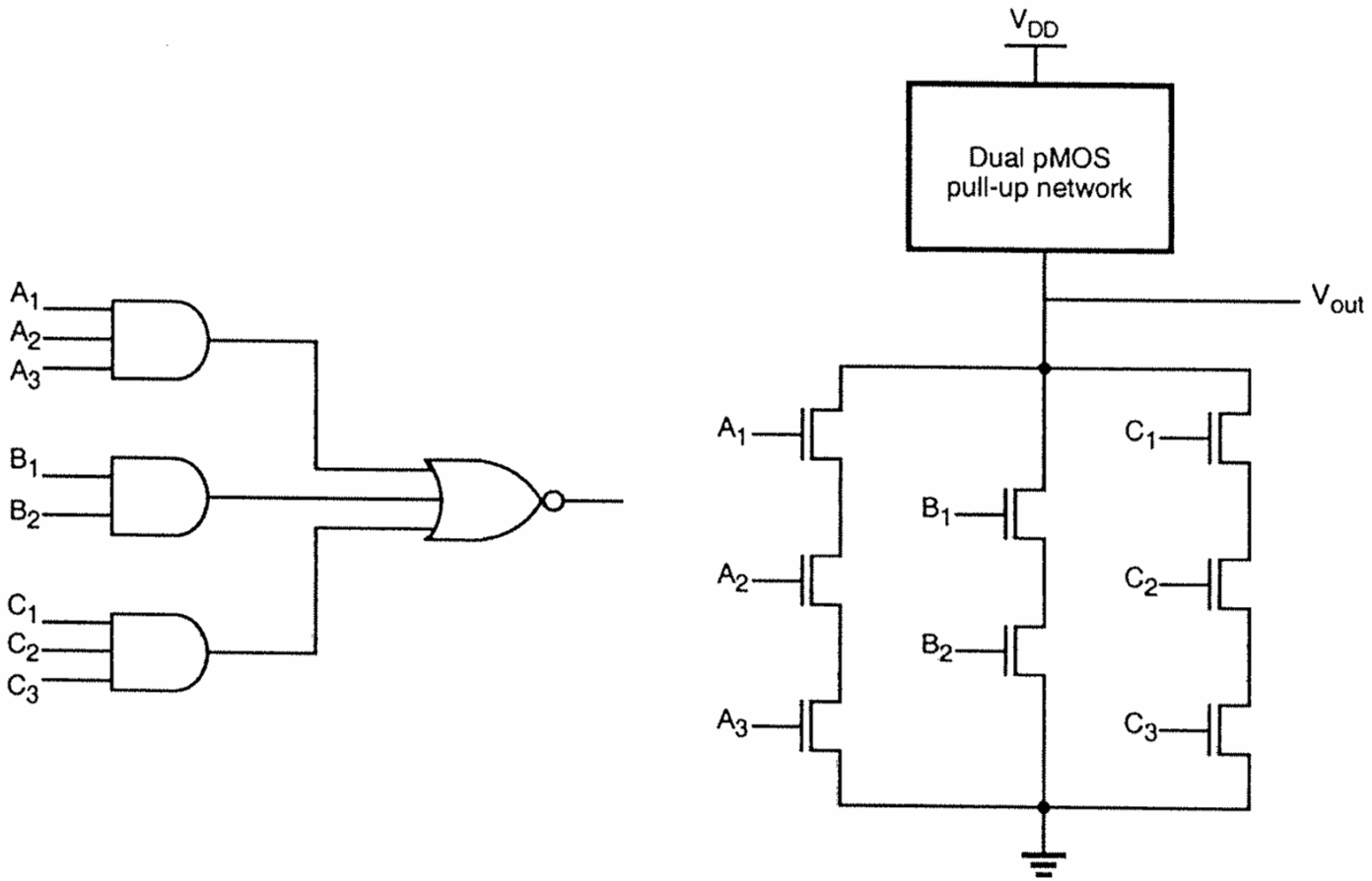
Complex CMOS Gate



$$OUT = \overline{(D + A \bullet (B + C))}$$

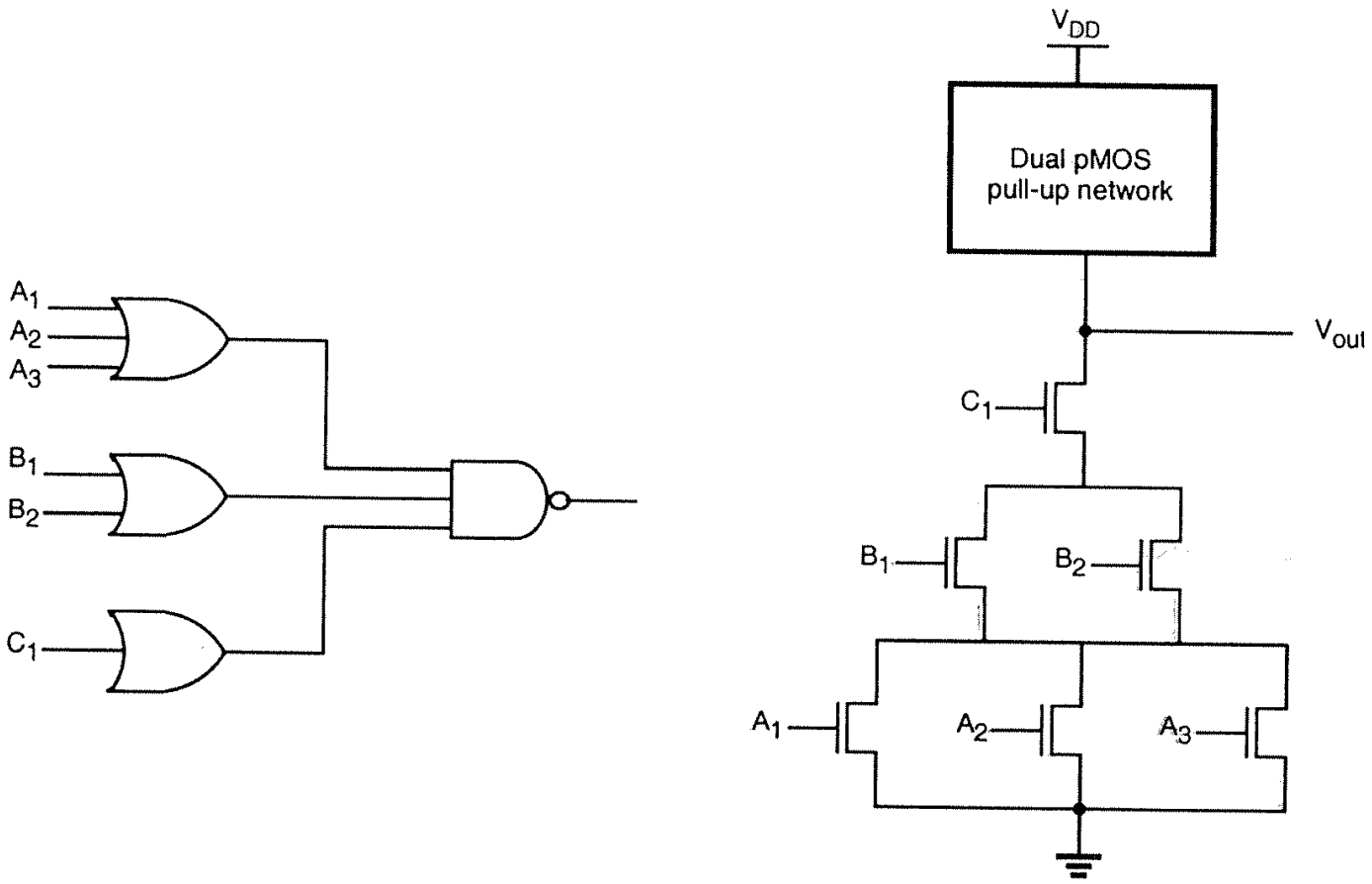
AND-OR-INVERTER (AOI) Gate

- An AND-OR-INVERTER (AOI) gate and corresponding pull-down net



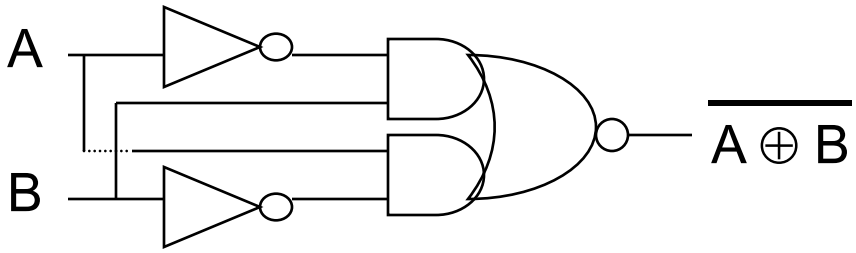
OR-AND-INVERTER (OAI) Gate

- An OR-AND-INVERTER (OAI) gate and corresponding pull-down net

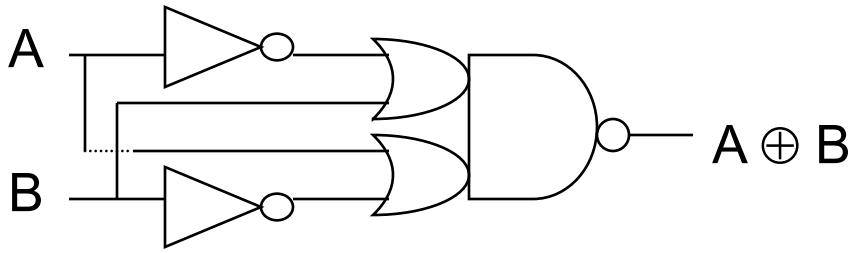


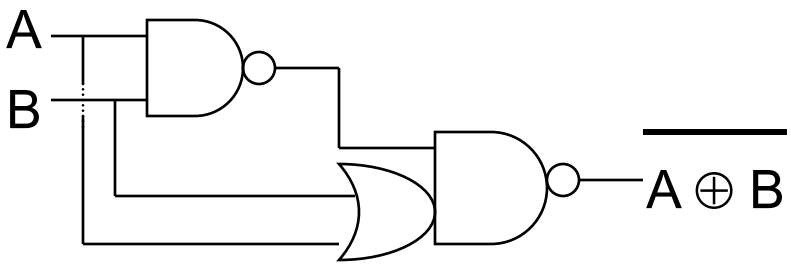
XNOR/XOR Gates

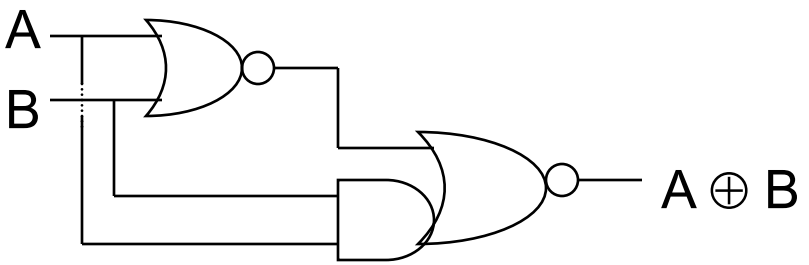
XNOR



XOR



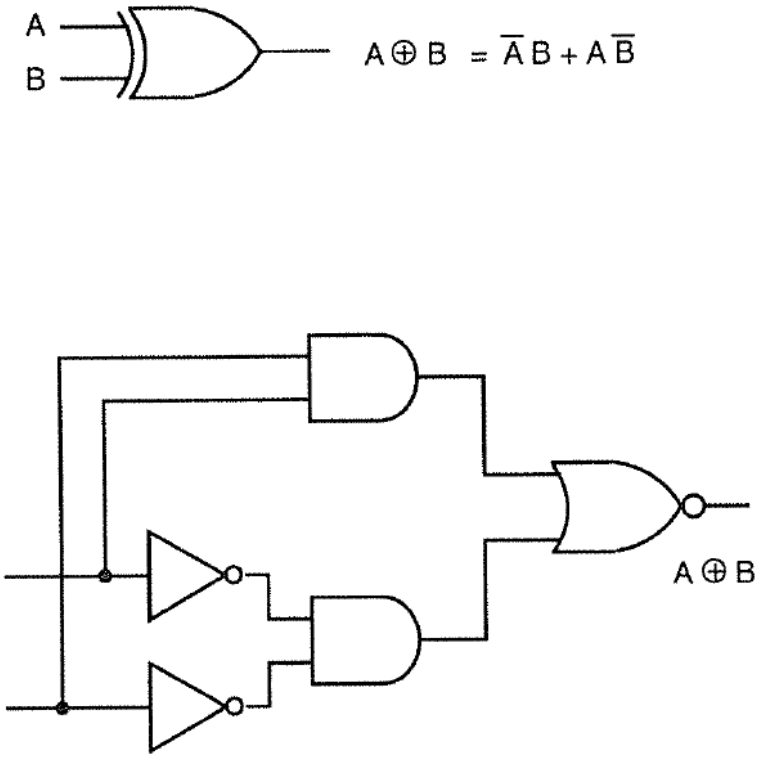


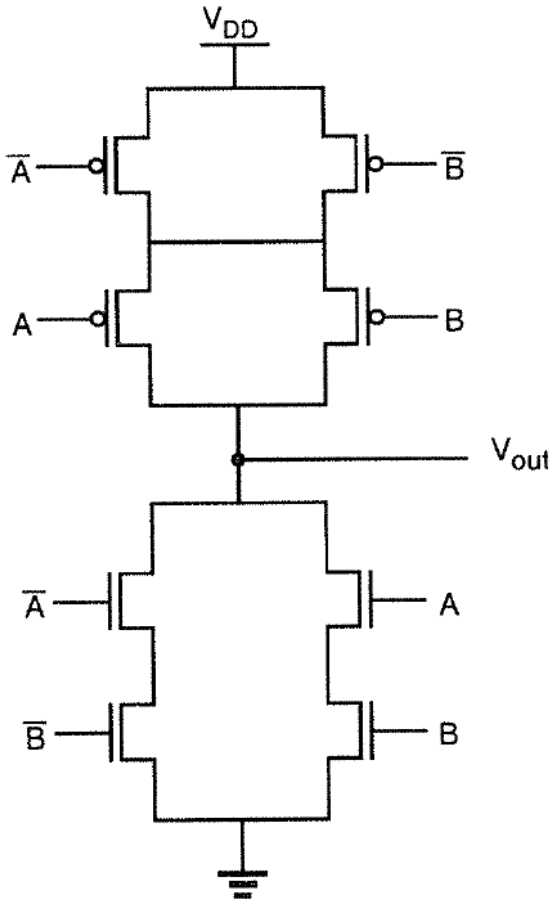


- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

XOR Gate Implementation

- Full-CMOS implementation of the XOR gate



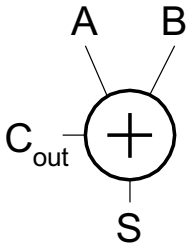


Single-Bit Addition

Half Adder

$$S = A \oplus B$$

$$C_{out} = A \bullet B$$

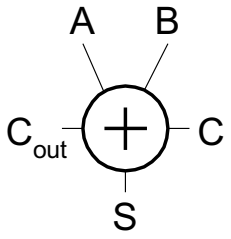


A	B	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Full Adder

$$S = A \oplus B \oplus C$$

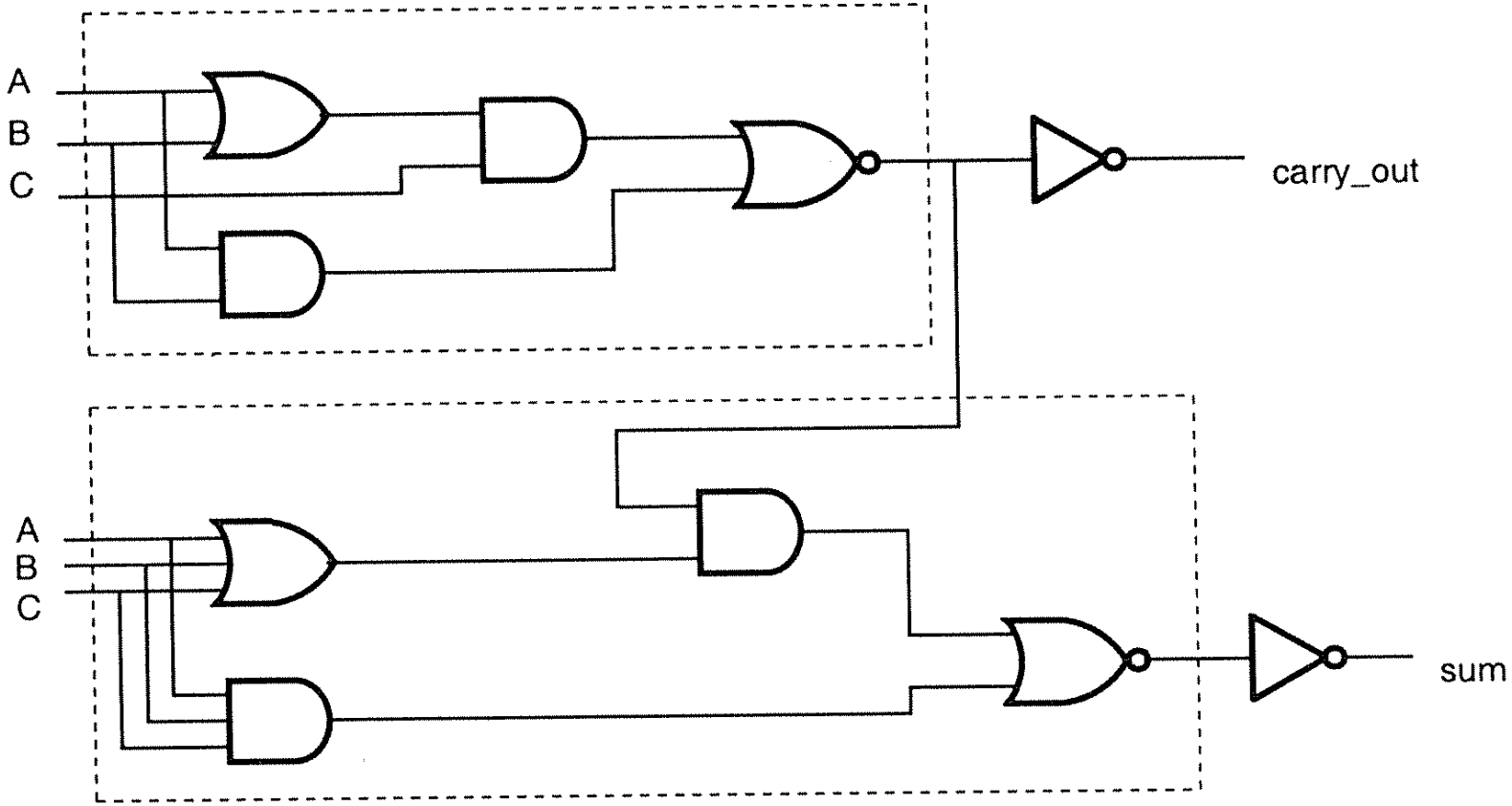
$$C_{out} = MAJ(A, B, C)$$



A	B	C	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

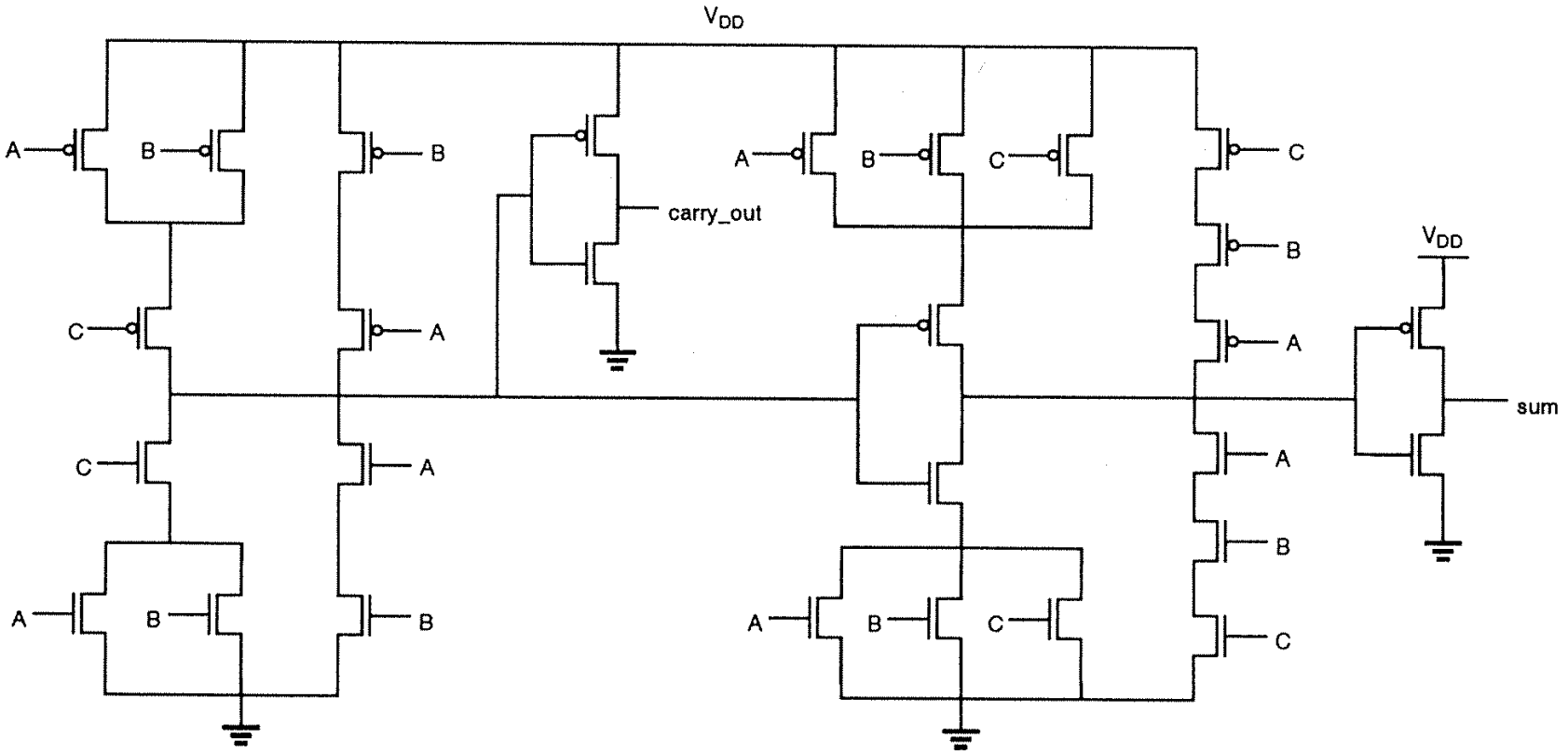
1-Bit Full Adder – Gate Level

- Gate-level schematic of the one-bit full-adder circuit



1-Bit Full Adder – Transistor Level

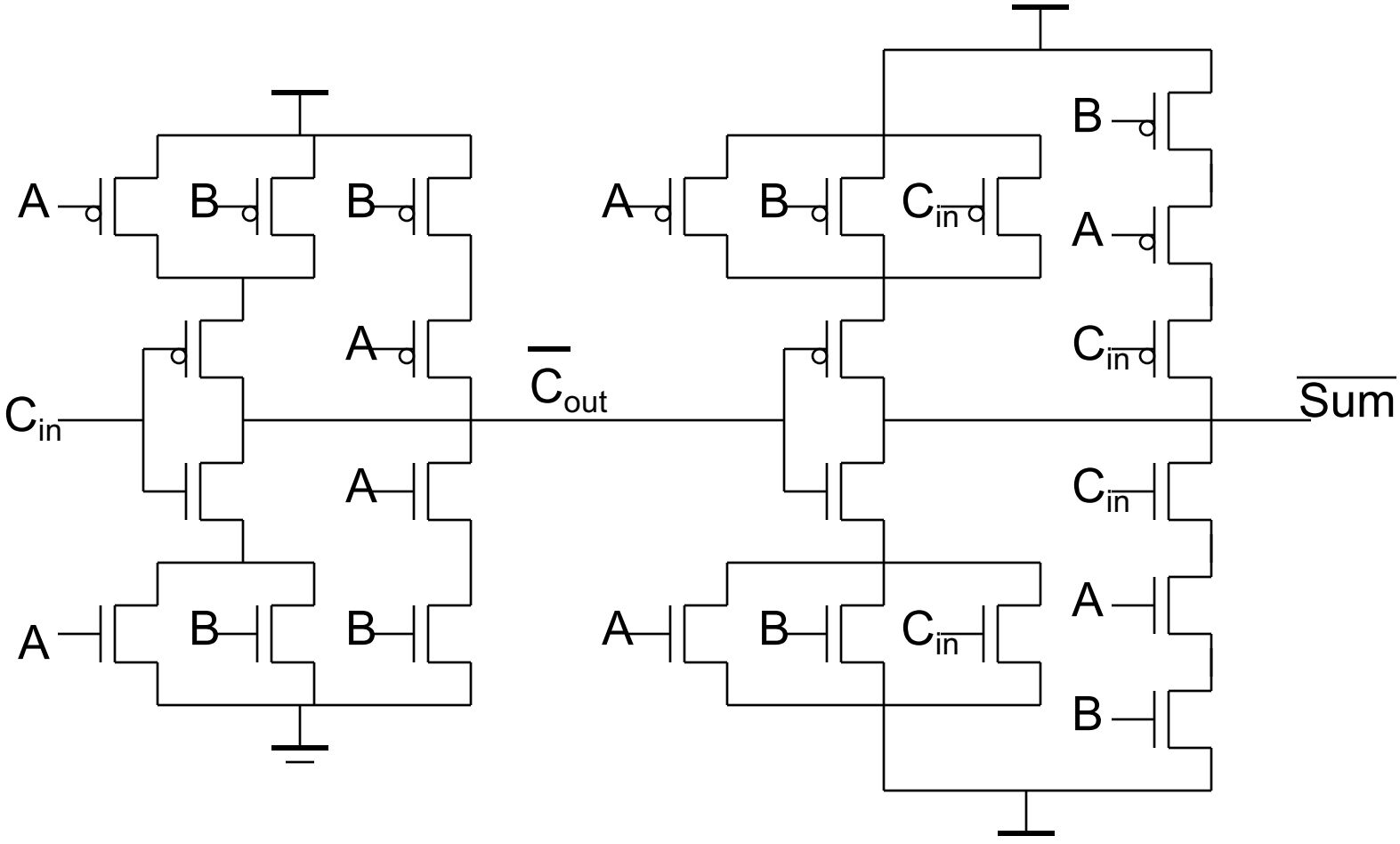
- Transistor-level schematic of the one-bit full adder circuit



Static CMOS Full Adder Circuit

$\overline{C}_{out} = \overline{C}_{in}\ \&\ (\overline{A} \mid \overline{B}) \mid (\overline{A}\ \&\ \overline{B})$

$\overline{Sum} = C_{out}\ \&\ (\overline{A} \mid \overline{B} \mid \overline{C}_{in}) \mid (\overline{A}\ \&\ \overline{B}\ \&\ \overline{C}_{in})$



$C_{out} = C_{in}\ \&\ (A \mid B) \mid (A\ \&\ B)$

$Sum = \overline{C}_{out}\ \&\ (A \mid B \mid C_{in}) \mid (A\ \&\ B\ \&\ C_{in})$