NYCU-EE IC LAB – Spring 2023

Final project Check List

Self-Verify APR Result

./02_check under 09_SUMBIT to download your Final_Project_iclabXXX.tar file back
Create a new directory, enter the directory and decompress the tar file.
Enter the decompressed directory.

1. Make sure your CHIP_iclabXXX.sdc is written correctly: period, waveform parameter, input delay and output delay. Waveform parameter, input delay and output delay should be half of the period.

2. Invoke innonus and restore CHIP_iclabXXX.inn
   (Remember to create a new folder in case you overwrite previous design)

3. Explore the core size and die size, also verify if the core to IO boundary should be larger than 100.

4. Verify the floorplan and powerplan constraints:
   a. Power ring: wire group, interleaving, and at least 4 pairs, width 9.
   b. Stripes: distance between 2 sets should be less than 200, and width 4.

5. SI Timing analysis with non-negative slacks, 0 DRVs, core filler added.

6. Verifying Geometry and Connectivity after adding core filler cells.

7. Latency cycles in post simulation should be the same as gate level simulation.

8. SRAMs must be inside core region.