ELEE 2330 – Digital systems – I

Homework-7 (Chapter 7)

For your Homework report, you should include in the upper right corner of the report, the Homework number, your *name in CAPITAL letters*, if you are *enrolled as ELEE/CMPE* etc. Don't forget to *staple your pages* in the upper left corner of your homework. Make sure your writing is in good form, clearly presented, and easily readable. Final answers shall be clearly outlined or circled, if possible. Points may be lost if your homework report doesn't comply with the above guidelines.

1. (a) What is main difference between a basic latch and a gated latch? Provide an example circuit for each.

1. (b) What is Setup time and Hold time for a given memory element? What is their significance?

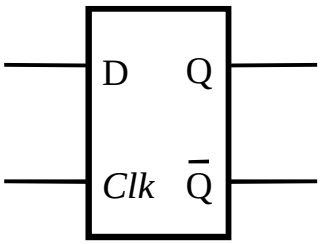
2. What is main difference between a level-sensitive latch and an edge-triggered flip-flop? Provide an example of their operation in terms of timing diagrams for each.

3. How can a JK flip-flop made to behave like a T flip-flop? How will the characteristic table for JK flip-flop look like when it is made to behave like T flip-flop?

4(a). Name the storage element shown below? _____.

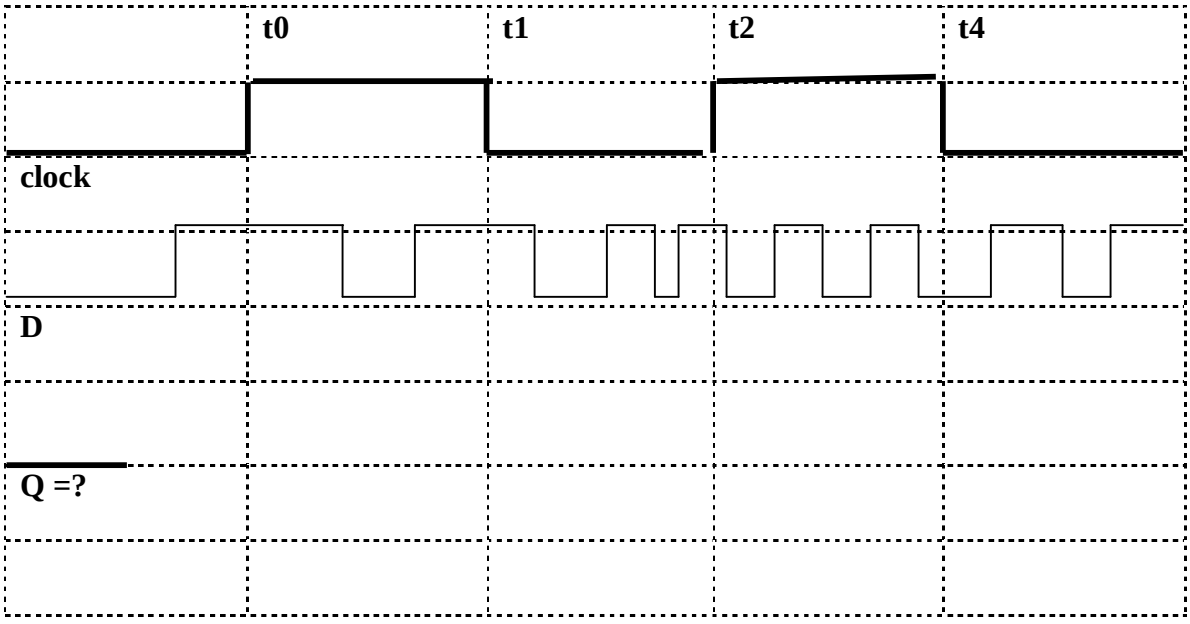
Clk	D	Q($t+1$)
0	x	Q(t)
1	0	0
1	1	1

Truth Table



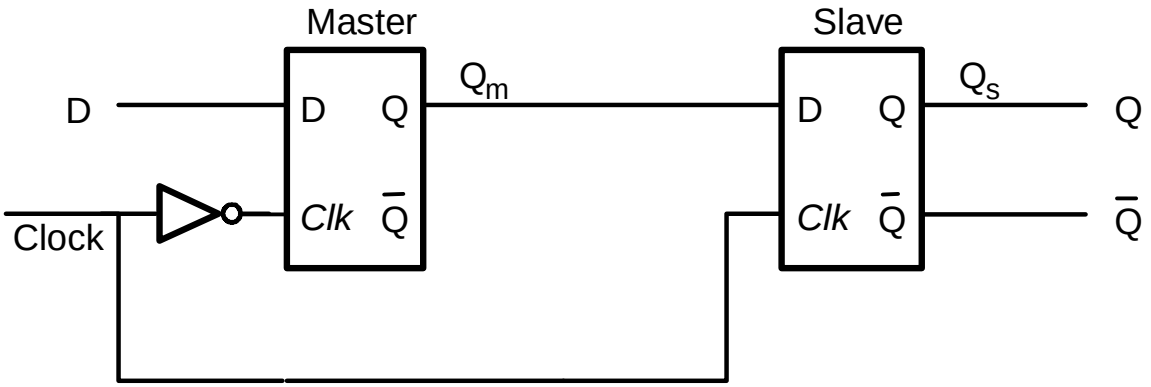
Graphical Symbol

4(b). For the storage elements shown above in 2(a), draw the output Q values in the timing diagram given below corresponding to the changing value of clock (clk) signal and the input data D.

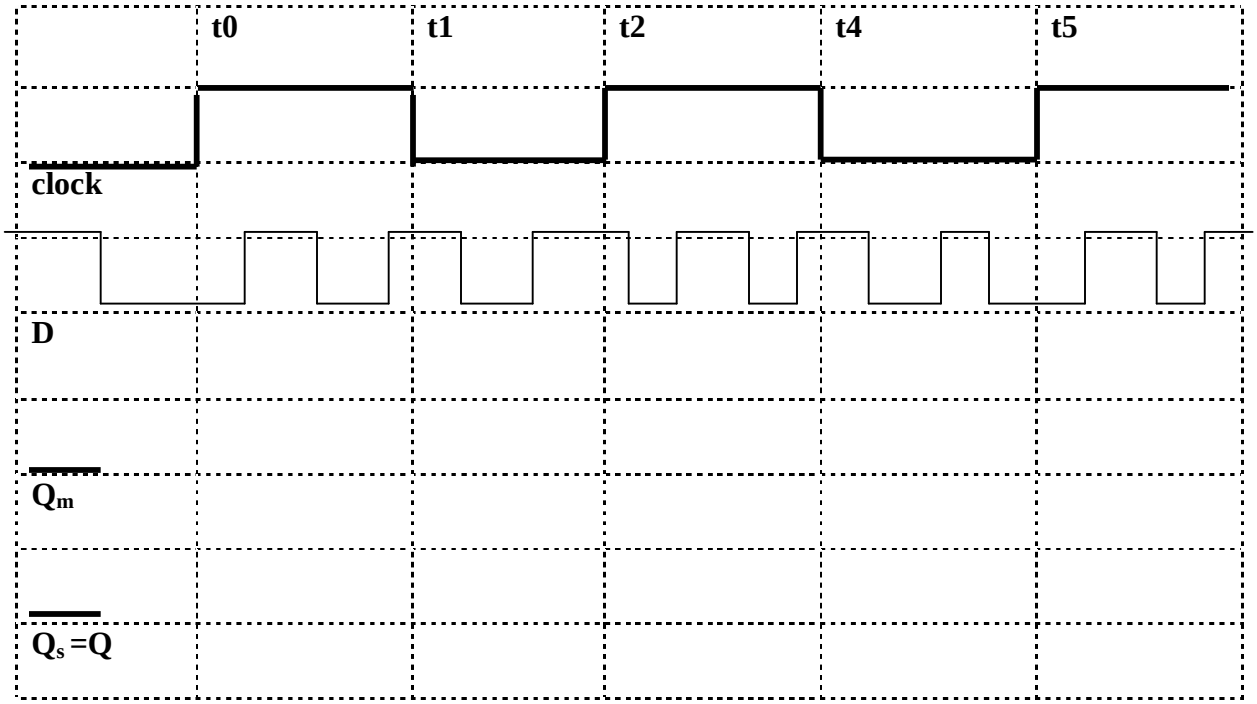


Timing Diagram

5a - For the Master-Slave D-latch configuration given below, complete the timing diagram -



5b - Draw intermediate output Q_m and final output $Q=Q_s$ values in the timing diagram below for each clock cycle shown -

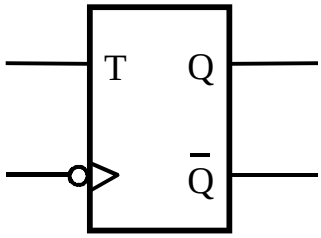


5c – Does this device as a whole behave like a positive-edge flip-flop or negative-edge flip-flop? Briefly explain why?

6(a). Name the storage element shown below? _____.

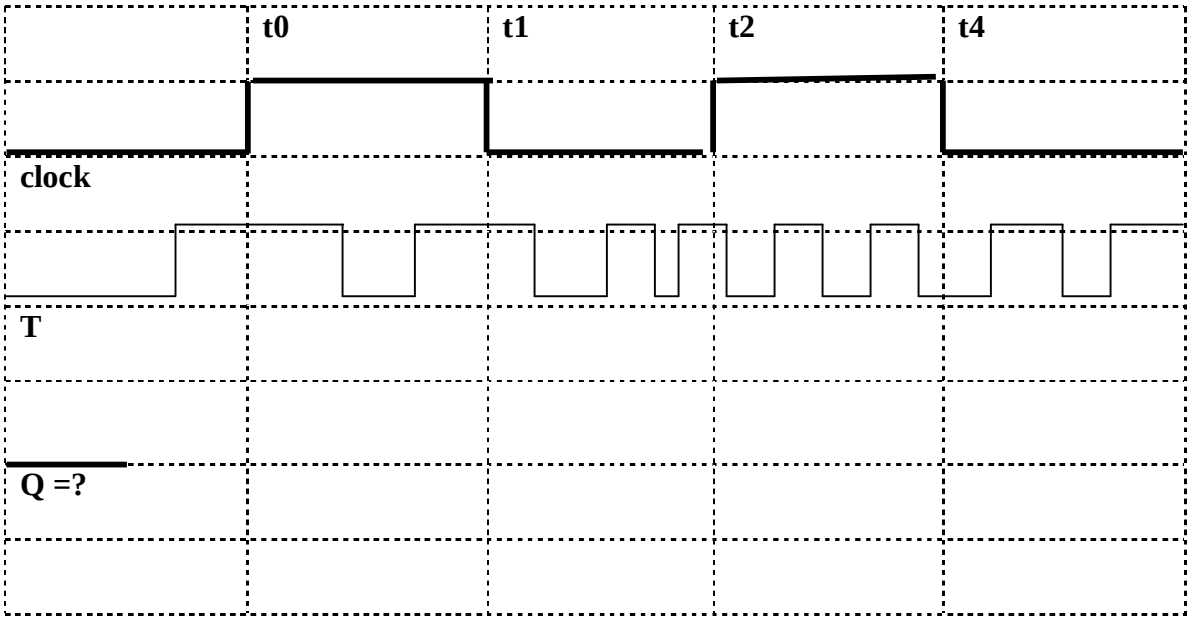
T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q}(t)$

Truth Table



Graphical Symbol

6(b). For the storage elements shown above in 2(a), draw the output Q values in the timing diagram given below corresponding to the changing value of clock (clk) signal and the input data D.



Timing Diagram

7. Following is a generalized circuit for a Johnson counter. Draw a 4-bit Johnson counter with 4 D-flip flops, with four outputs listed as Q0, Q1, Q2, Q3. Assume all outputs are initialized to zero by using the reset line. Draw a timing diagram for each outputs for 8 clock cycles, and provide the aggregate output of the counter in each clock cycle.