YIQIU SUN

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EDUCATION

University of Illinois, Urbana-Champaign — **Champaign, IL**
Ph.D in Computer Science — *Expected May 2026*
· Advisor: Saugata Ghose
· Research Interests: Processing-In-Memory, Programming Models for Novel Architectures, Hardware-Software Co-design

University of Michigan — **Ann Arbor, MI**
B.S.E in Computer Engineering — *May 2021*

Shanghai Jiao Tong University, UM-SJTU Joint Institute — **Shanghai, China**
Bachelor of Engineering in Electrical and Computer Engineering — *Aug. 2021*

PUBLICATIONS

T. J. Baker, **Y. Sun** and J. P. Hayes, "Benefits of Stochastic Computing in Hearing Aid Filterbank Design," 2021 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2021, pp. 1-5, doi: 10.1109/BioCAS49922.2021.9645021.

RESEARCH EXPERIENCE

MARIMBA: MAp-Reduce In-Memory-Based Acceleration — **Urbana, IL**
Advisor: Prof. Saugata Ghose — *Jan. 2022 - present*
· Explored the implementation of MapReduce framework on RACER, a cost-effective Processing-using-memory architecture
· Identified new design points for Processing-in-memory architectures by anaylzing the benefits and trade-offs of MapReduce with in-memory-based acceleration

Stochastic Circuits Implementation of Filter Banks Used in Hearing Aids — **Ann Arbor, MI**
Advisor: Prof. John P. Hayes — *May 2020 - Aug. 2021*
· Implemented a stochastic circuit version of filter bank used in hearing aids and used Synopsys to synthesis the circuits
· Minimized matching error while maintaining the advantage of stochastic circuits in area

Application of Deep Learning Algorithms on Transmuter — **Ann Arbor, MI**
Advisor: Prof. Trevor Mudge — *Jan. 2020 - Aug. 2020*
· Simulated RNN for the Transmuter architecture on gem5
· Optimized computer performance (GFLOPs) by 20% and total runtime (ms) by 50% through parallelism

PROJECT EXPERIENCE

Codelet-based Compiler Optimization Space Exploration — **Urbana, IL**
With Intel Corporation, Advisor: Prof. David Kuck — *Nov. 2021 - present*
· Generalized hardware saturation rules based on different types of codelets to enlarge optimization search space of Compiler
· Helped develop a tool to automate the whole process from codelet generation to experimental data analysis

Scheduling Algorithms and Optimizations for Lowering Python Package APIs to AI Engine Array — **Urbana, IL**
Advisor: Prof. Vikram Adve — *Oct. 2021 - Dec. 2021*
· Scheduled high-level NumPy logic onto AI engines and established specialized performance modeling for AI engines
· Designed a more exhaustive FFT design space than polyhedral model

Analyzing the Impact of Processing-in-Memory Devices on Scene Reconstruction — **Urbana, IL**
Advisor: Prof. Saugata Ghose — *Oct. 2022 - Dec. 2022*
· Evaluated two different depth fusion algorithms executing on a conventional CPU + memory system and a Hybrid Memory Cube with standard CPU cores
· Designed a custom hardware accelerator for depth fusion that can be built into the logic layer of a 3D-stacked memory

RISC-V SoC Microarchitecture Design & Optimization — **Shanghai, China**
SJTU Graduation Thesis, Advisor: Prof. Gang Zheng — *May 2021 - Aug. 2021*
· Implemented a 4-way Out-of-Order superscalar RISC-V processor and verified the synthesis results on Vivado
· Added approximate computing unit to the execution stage for domain-specific optimization

TUTORING EXPERIENCE

Undergraduate Mentor, UIUC — **Urbana, IL**
· Supervised student: Tianyun Zhang, CS+Economics 23' — *Jan. 2022 - Present*

Transfer Student Leader, University of Michigan — **Ann Arbor, MI**
· Organized event to help new incoming transfer students get accustomed to school life better — *August 2020 - May 2021*

Teaching Assistant, UM-SJTU Joint Institute — **Shanghai, China**
· Courses: Honor Mathematics (VV186), Electromagnetics (VE 230) — *Sep. 2019 - Dec.2019, May 2020 - August 2020*