Bug Report

Sequence of Operations done in order to catch the bug :

After reset

Write operation : addr=2 and data_in=0F

Write operation : addr=2 and data_in=0A

Read operation : addr=0

Bug in the Design:

The highlighted portion in the design is the bug. Here we are assigning the data_in value to the addr and due to which cache is always missing the cache_hit operation because the address is getting changed at the cache level.

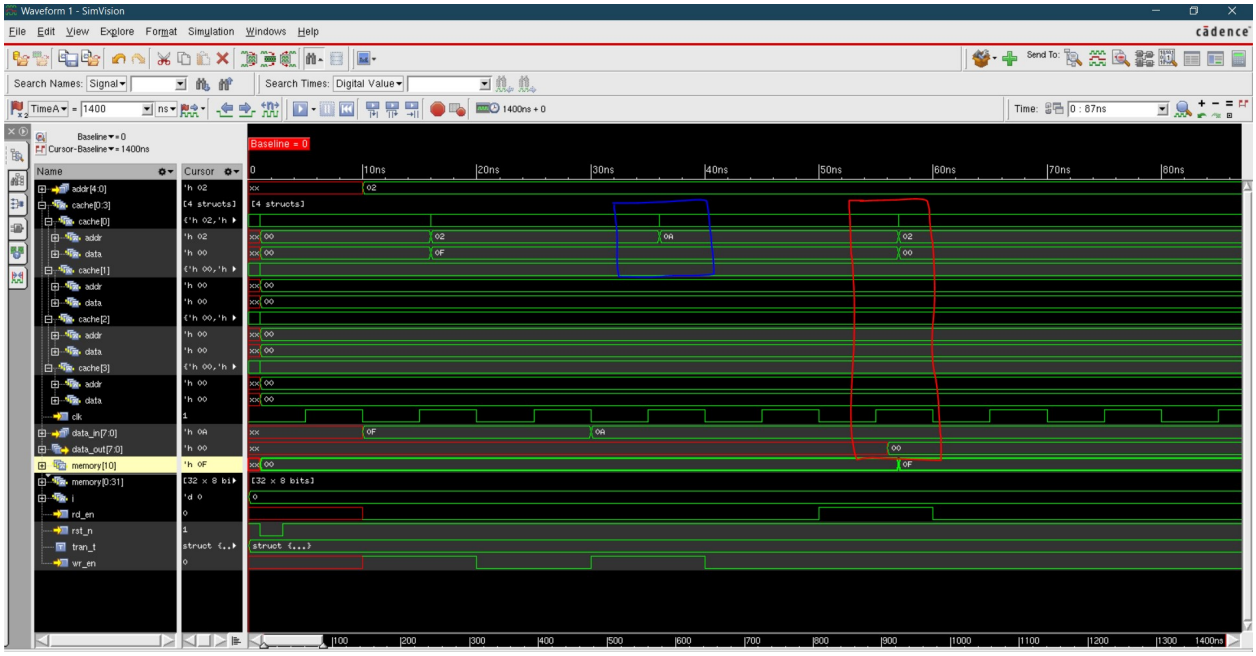
- The bug in the design lies at line number 50 in the cache_mem design file
- This scenario happens whenever there is Cache-Hit.
- The issue here is whenever the address of the cache and requested operation matches the design is writing the data_in to the addr field instead of the data field of the cache.
- Also the data field is 8bit wide and the addr field is 5bit wide, so this gives wrong information and even stores the wrong addr value in the cache.

```
always @(posedge clk or negedge rst_n) begin
  if (rst_n==0) begin
    for(int i=0; i<32; i++)
      memory[i] <= 8'b0;
    for (int i=0; i<4; i++) begin
      cache[i].addr <= 5'b0;
      cache[i].data <= 8'b0;
    end
  end
  else if ((wr_en==1) && (rd_en==0)) begin
    j = addr/8;
    if (cache[j].addr == addr)
      #1 cache[j].addr <= data_in;
    else begin
      memory[cache[j].addr]=cache[j].data;
     #1 cache[j].addr <= addr;
      cache[j].data <= data_in;
    end
  end
  else if ((wr_en==0) && (rd_en==1)) begin
    j = addr/8;
    #1 data_out <= memory[addr];
    if (cache[j].addr == addr)
      #1 data_out <= cache[j].data;
    else begin
      #1 data_out <= memory[addr];
      memory[cache[j].addr]=cache[j].data;
      cache[j].addr <= addr;
      cache[j].data <= memory[addr];
    end
  end
end

endmodule
```

Waveform Snippet:

- The blue highlighted portion shows that the data_in value of 0A is being written in the cache[0] as an addr due to the line number 50 operation in the design file, which is completely wrong.
- Now when we try to read the value at addr 02 it doesn't have the actual value of 0A and due to which the data_out is given false value of 00 (red highlighted portion in the waveform)



Bug Fix:

Issue: #1 cache[j].addr <= data_in;

Solution: #1 cache[j].data <= data_in;

Waveform Snippet with the solution: